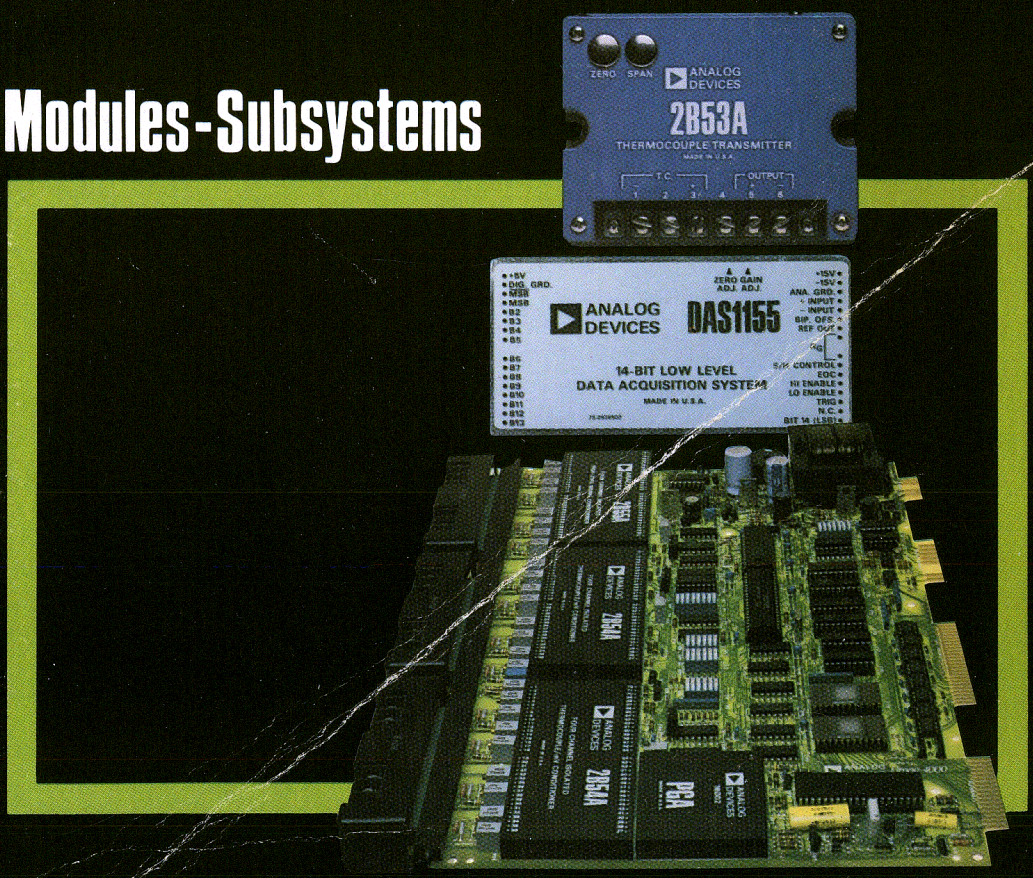
ANALOG DEVICES

Data-Acquisition Databook 1982

Modules-Subsystems



How to Find Product Data in this Databook

HOW TO FIND PRODUCT DATA IN THIS DATABOOK

The Databook contains Data Sheets for all products recommended for new designs, lists of Available Products not databookec here (data sheets upon request), and a Substitution Guide for products no longer available, plus a wealth of background information.

THERE ARE TWO VOLUMES

VOLUME I contains technical data on our *integrated circuits and hybrids* for data acquisition, plus abbreviated data on cert Volume II products that are well-suited to new designs and do not yet have integrated-circuit equivalents.

VOLUME II has all data-acquisition products manufactured in the form of *modules, cards, instruments, and discrete-assembl subsystems.*

DO YOU KNOW THE MODEL NUMBER?

If it's an Analog Devices model number, look it up in the alphanumeric Index (Section 2) to find the Volume, Section, an Page numbers.

If you're looking for a form-and-function-compatible version of a product originally brought to market by some other manufacturer (second source), add our "AD" prefix and look it up in the Index.

IF YOU DON'T KNOW THE MODEL NUMBER

There are two ways to find a device to perform your function:

1. **FIND YOUR FUNCTION IN THE LIST ON THE OPPOSITE PAGE**
   Use the "bleed tabs" to turn directly to the appropriate Section. You will find one or more functional Selection Guides the beginning of the Section. The Selection Guide will help you find the products that are closest to satisfying your nee and their Volume-Section-Page locations. Use it to compare all products in the category by salient criteria, no matter which Volume their technical data resides in.

2. **IF THE FUNCTION IS NOT LISTED BY A NAME THAT YOU RECOGNIZE**
   Find it in the diagram (opposite page) or in the Index (Section 2). The Index will help you find the Selection Guides fo products in that functional category. Then use the Selection Guide(s) to find the Volume-Section-Page locations of products that will come closest to satisfying your need.

A RELATED PRODUCT MAY BE WHAT YOU REALLY WANT

Text in each section often mentions related or complementary product categories having a greater or lesser degree of functic integration.

IF YOU CAN'T FIND IT HERE . . . ASK!

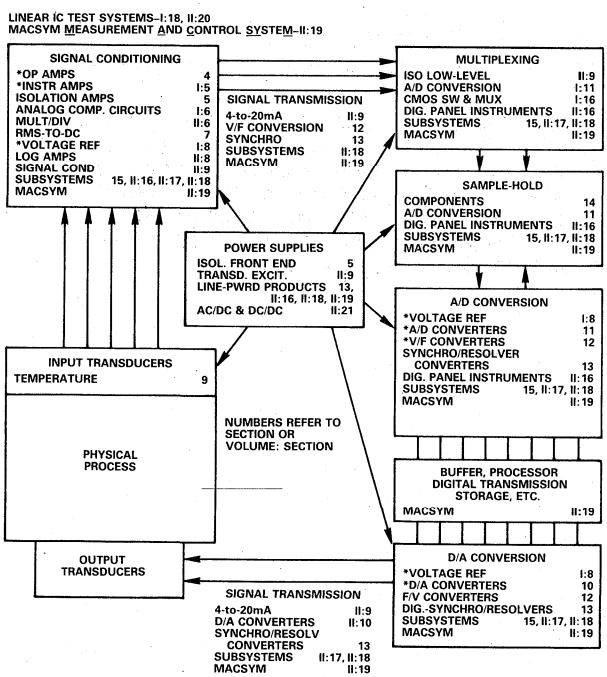
See Worldwide Service Directory in last pages of this Volume.

ANALOG DEVICES

DATA-ACQUISITION DATABOOK 1982

VOLUME II
MODULES-SUBSYSTEMS

PICTORIAL GUIDE TO PRODUCT CATEGORIES



*Automatic Test Instrumentation Available (I:18, II:20)

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DATA-ACQUISITION DATABOOK 1982

VOLUME II: MODULES-SUBSYSTEMS

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Specifications and prices shown in this Databook are subject to change without notice.

Products in this book may be covered by one or more of the following patents. Additional patents are pending. See individual data sheets for further information:

U.S.: 3,007,114, 3,278,736, 3,355,670, 3,441,913, 3,467,908, 3,500,218, 3,530,390, 3,533,002, 3,685,045, 3,729,660, 3,747,088, 3,793,563, 3,803,590, 3,842,412, 3,868,583, 3,872,466, 3,887,863, 3,890,611, 3,906,486, 3,909,908, 3,932,863, 3,940,760, 3,942,173, 3,946,324, 3,950,603, 3,961,326, 3,978,473, 3,979,688, 4,016,559, 4,020,486, 4,029,974, 4,034,366, 4,092,698, 4,123,698, 4,136,349, 4,141,004, 4,213,806, 4,250,445, 4,270,118, 4,268,759, 4,054,829, 4,286,225. U.K.: 1,310,591, 1,310,592, 1,364,233, 1,470,673, 1,470,674, 1,537,542, 1,531,931, 1,571,869, 1,590,136, 1,590,137. France: 70.10561, 71.28952, 74.25263, 76 08238. West Germany: 20 14 034, 21 39 560. Italy: 933,798. Canada: 1,025,558, 1,035,464, 984,015, 1,006,236, 1,054,248. Sweden: 7603320-8.

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General Introduction

Analog Devices designs, manufactures, and sells worldwide sophisticated electronic components and subsystems for use in precision measurement and control. More than six hundred standard products are produced in manufacturing facilities located throughout the world. These facilities encompass all relevant technologies, including bipolar, I^2L, CMOS, and hybrid integrated circuits–and assembled products in the form of potted modules, printed-circuit boards, and instrument packages.

State-of-the-art technologies have been utilized (and, in many cases, invented) to provide timely, reliable, easy-to-use advanced designs at realistic prices. More than fifteen years of successful applications experience and continuing vertical integration insure that these products are oriented to user needs. The continuing application of present state-of-the-art and the invention of future state-of-the-art processes strengthens the leadership position of Analog Devices in data-acquisition products.

MAJOR PROGRESS

Since the publication of our one-volume Databook, *Data Acquisition Components and Subsystems Catalog*, in 1980, more than 60 significant new products have been introduced. They are identified by bullets (•) in the Index and in the table of contents for each section of this Databook. The sheer mass of new products, the impressive volume of technical data on our large and rapidly growing line of precision integrated circuits, and the increasing diversity of our modular and subsystem product lines for precision data acquisition and control have led us to take the logical step of dividing the Databook into two Volumes, retaining within each the functional organization that our customers have found so useful.

MODULES-SUBSYSTEMS

The list of product-category "bleed tabs" opposite the "How to Find It" Guides on the inside front cover of this Volume is a functional summary of our modular and board-level component, subsystem, and instrument classes. The complete Index, starting on page 2-1, provides a detailed alphanumeric panorama of products and functions, irrespective of technology, appearing in either or both Volumes of this Databook.

Among the most significant of our new products, in terms of both user applications and advancement of the technology, are the monolithic 16-bit AD7581 CMOS D/A converter; the monolithic 8-channel 8-bit AD7581 CMOS data-acquisition system with data continuously available in 8 channels of on-board memory; the AD547 family of monolithic drift-trimmed high-performance FET-input op amps and its AD647 matched-dual version; the AD7528 monolithic dual D/A converter; the high-performance AD293/294 hybrid isolation amplifiers, based on an ingenious thick-film printed transformer and a significant advance in isolator circuit design; and the μMAC-4000 Intelligent Single-Board Data-Acquisition System and its high-performance plug-in analog signal conditioners–with available software for using popular micro- and minicomputers as host computers.

TECHNICAL SUPPORT

Analog Devices offers extensive technical literature, which discusses the technology and applications of products for precision measurement and control. Besides comprehensive data sheets, of which there are many outstanding examples in this book, we offer Application Notes, Application Guides, Technical Handbooks (at reasonable prices), and two serial publications: *Analog Productlog*, which provides brief information on new products being introduced, and *Analog Dialogue*, our technical journal, which provides-in-depth discussions of new developments in analog and digital circuit technology as applied to data-acquisition and control. We maintain a mailing list of engineers, scientists, and technicians with a serious interest in our products. In addition to data-book catalogs–such as this one–we also publish several short-form catalogs, including a *Short-Form Guide* to our entire product line. You will find our publications described on page 1-9 at the back of the book.

SALES OFFICES

Backing up our design and manufacturing capabilities and our extensive array of publications is a network of sales offices and representatives throughout the United States and most of the world. They are staffed by experienced sales and applications engineers, and many of them maintain a local stock of Analog Devices products. Our Worldwide Service Directory appears on pages 1-10 and 1-11 at the back of the book.

STANDARDS

Many products comply with MIL-STD-883B and/or other customer requirements. Analog Devices Semiconductor has complete capabilities for 100% screening of devices per Methods 5004 and 5005 of MIL-STD-883B; generic data is available on many of our products. Our CMOS facility in the Republic of Ireland has received plant approval from the European standardization authority; its quality-assurance procedures and capabilities have met the standards of CECC (CENELEC Electronic Components Committee), which are essentially compatible with what are known in the U.S.A. as MIL-M-38510 and MIL-STD-883B. A summary of our IC quality assurance procedures appears in Section 19 of Volume I.

PRODUCTS NOT CATALOGUED HERE

On page 1-3, at the back of this book, you will find a table listing the sections (bleed tabs) to be found in the other Volume of the Databook. In the pages that follow it, you will find Selection Guides listing salient characteristics of products in categories that are to be found exclusively in that volume.

For maximum usefulness to designers of new equipment, without unwieldy size, we have limited the contents of the Databook to products most likely to be used for the design of new circuits and systems. If the data sheet for a product you are interested in is not in either Volume turn to page 1-7, at the back of this book, where you will find a list of older products for which data sheets are available upon request. On page 1-8 you will find a guide to substitutions for products no longer available.

PRICES

At Analog Devices, we recognize that accurate, up-to-date prices of our products are an important consideration in making a choice among the many available product families. However, since prices are subject to change, current price lists and/or quotations are available upon request from our sales offices.

(this section continues at the back of the book)

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Alphanumerically by Product
Alphabetically by Function

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Ordering Guide

INTRODUCTION

This Ordering Guide should make it easy to order Analog Devices products, whether you're buying one IC op amp, a multi-option subsystem, or 1000 each of 15 different items. It will help you:

1. Find the correct part number for the options you want.
2. Get a price quotation and place an order with us.
3. Know our warranty for components and subsystems.

For answers to further questions, call the nearest sales office (listed at the back of the book) or our main office in Norwood, Mass. U.S.A. (617-329-4700).

MODEL NUMBERING

Many of the data sheets in the Databook have an Ordering Guide. Use it to specify the correct part number for the exact combination of options you want. Part numbering systems for ICs and hybrids will be found in Volume I, Section 3. If there is any question, call us.

ORDERING FROM ANALOG DEVICES

When placing an order, please provide specific information regarding model type, number, option designations, quantity, ship-to and bill-to address. Prices quoted are list; they do not include applicable taxes, customs, or shipping charges. All shipments are F.O.B. factory. Please specify if air shipment is required.

Place your orders with our local sales office or representative, or directly with Norwood. Orders and requests for quotations may be telephoned, sent via TWX or TELEX, or mailed. Orders will be acknowledged when received; billing and delivery information is included.

Payments for new accounts, where open-account credit has not yet been established, will be C.O.D. or prepaid. On all orders under fifty dollars ($50.00), a five-dollar ($5.00) processing charge is required.

When prepaid, orders should include $2.50 additional for packaging and postage (and a 5% sales tax on the price of the goods if you are ordering for delivery to a destination in Massachusetts).

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All Analog Devices, Inc., products are warranted against defects in workmanship and materials under normal use and service for one year from the date of their shipment by Analog Devices, Inc., except that components obtained from others are warranted only to the extent of the original manufacturers' warranties, if any, except for component test systems, which have a 180-day warranty, and μMAC and MACSYM systems, which have a 90-day warranty. This warranty does not extend to any products which have been subjected to misuse, neglect, accident, or improper installation or application, or which have been repaired or altered by others. Analog Devices' sole liability and the Purchaser's sole remedy under this warranty is limited to repairing or replacing defective products. (The repair or replacement of defective products does not extend the warranty period. This warranty does not apply to components which are normally consumed in operation or which have a normal life inherently shorter than one year.) Analog Devices, Inc., shall not be liable for consequential damages under any circumstances.

THE FOREGOING WARRANTY AND REMEDY ARE IN LIEU OF ALL OTHER REMEDIES AND ALL OTHER WARRANTIES, WRITTEN OR ORAL, STATUTORY, EXPRESS, OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

Operational Amplifiers

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	J-FET				•	•			•	•
	Dual J-FET						•	•		
Multi-Device Technology	Hybrid		•	•	•					
	Module									
High Open Loop Gain	≥100dB					•	•			
	≥140dB									
High CMR	>100dB									
Low Offset Voltage	≤5mV	•		•		•	•	•	•	•
	≤1mV					•	•	•	•	
	≤50μV									
Low Offset V, vs. Temp	≤5μV/°C					•	•	•	•	
	≤1μV/°C									
	≤0.6μV/°C									
Low Bias Current	≤50pA		•	•	•	•	•	•	•	
	≤5pA									
	≤0.5pA									
Fast Settling	≤1μs to 0.1%							•	•	
	≤5μs to 0.01%									
Wideband (Unity Gain)	≥2MHz							•	•	•
	≥10MHz									
High Slew Rate	≥10V/μs							•	•	•
	≥30V/μs									
	≥100V/μs									
	≥1000V/μs									
Low Noise (0.1 to 10Hz) 2μV p-p						•	•	•	•	•
High Voltage Out	≥100V									
High Current Out	≥20mA									
Low Power	≤75mW	•				•	•	•	•	•
Second Source		•								•
Temperature Range 0 to +70°C		•	•	•	•	•	•	•	•	•
-25°C to +85°C										•
-55°C to +125°C		•	•	•	•	•	•	•	•	•
Dice Availability					•	•	•	•	•	
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		HIGH ACCURACY												
		LOW V_{OS} DRIFT												
		LOW BIAS CURRENT												
		FET INPUT												
		AD504	AD510	AD OP-07	AD517	234	235[1]	261[1]	AD545	AD547	AD647	52	AD515	171
Monolithic Technology	Bipolar Input	•	•	•	•									
	J-FET									•	•			
	Dual J-FET													
Multi-Device Technology	Hybrid								•				•	
	Module					•	•	•				•		•
High Open Loop Gain	⩾100dB	•	•	•	•	•	•	•		•	•	•		•
	⩾140dB					•	•	•						
High CMR	>100dB	•	•	•	•			•				•		•
Low Offset Voltage	⩽5mV	•	•	•	•	•	•	•	•			•	•	•
	⩽1mV					•	•	•		•	•	•		•
	⩽50μV			•	•	•	•	•						
Low Offset V, vs. Temp	⩽5μV/°C	•	•	•	•	•	•	•	•	•	•	•		
	⩽1μV/°C					•	•	•		•	•	•		
	⩽0.6μV/°C	•	•	•		•	•	•						
Low Bias Current	⩽50pA						•		•	•	•	•	•	•
	⩽5pA								•			•	•	
	⩽0.5pA												•	
Fast Settling	⩽1μs to 0.1%													
	⩽5μs to 0.01%					•								
Wideband (Unity Gain)	⩾2MHz					•								•
	⩾10MHz													
High Slew Rate	⩾10V/μs													•
	⩾30V/μs					•								
	⩾100V/μs													
	⩾1000V/μs													
Low Noise (0.1 to 10Hz) 2μV p-p		•	•	•	•	•		•		•	•	•		
High Voltage Out	⩾100V													•
High Current Out	⩾20mA													
Low Power	⩽75mW								•	•	•		•	
Second Source				•										
Temperature Range 0 to +70°C		•	•	•	•		•	•	•	•	•	•	•	•
-25°C to +85°C														
-55°C to +125°C		•	•	•	•					•	•			
Dice Availability				•	•					•				
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[1] Chopper Stabilized

		FAST/WIDEBAND												
						FET INPUT							UNITY GAIN BUFFER	
		AD507	AD509	AD518	48	AD380	AD381	AD382	AD3554	50, 51	HOS-050	ADLH0032	ADLH0033	HOS-100
Monolithic Technology	Bipolar Input J-FET Dual J-FET	•	•	•										
Multi-Device Technology	Hybrid Module				•	•	•	•	•	•	•	•	•	•
High Open Loop Gain	⩾100dB ⩾140dB	•			•		•	•	•		•			
High CMR	>100dB													
Low Offset Voltage	⩽5mV ⩽1mV ⩽50μV	•	•		•	•	•	•	•	•		•	•	
Low Offset V, vs. Temp	⩽5μV/°C ⩽1μV/°C ⩽0.6μV/°C						•	•						
Low Bias Current	⩽50pA ⩽5pA ⩽0.5pA				•		•	•	•			•	•	
Fast Settling	⩽1μs to 0.1% ⩽5μs to 0.01%	•	•	•	•	•	•	•	•	•	•	•	•	•
Wideband (Unity Gain)	⩾2MHz ⩾10MHz	•	•	•	•	•	•	•	•	•	•	•	•	•
High Slew Rate	⩾10V/μs ⩾30V/μs ⩾100V/μs ⩾1000V/μs	•	•	•	•	•	•	•	•	•	•	•	•	•
Low Noise (0.1 to 10Hz) 2μV p-p							•	•						
High Voltage Out High Current Out Low Power	⩾100V ⩾20mA ⩽75mW	•			•	•		•	•	•	•		•	•
Second Source		•	•						•			•	•	
Temperature Range 0 to +70°C -25°C to +85°C -55°C to +125°C		• • •	• • •	• • •	•	• • •	• • •	• • •	• • •	• • •	• •	• • •	• • •	• • •
Dice Availability				•										
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Orientation
Operational Amplifiers

The amplifiers listed in the two volumes of this catalog are intended to provide cost-effective solutions to the bulk of op-amp requirements in precision measurement and control, as well as to more-general requirements in electronic circuits. The technical data included in these books* cover the properties of some 36 op-amp families, comprising more than 100 distinct types. Some are general purpose, others provide near-optimum performance for specific classes of applications.

They differ in a variety of ways, for example, circuit technology, circuit architecture, input properties, output properties, operating temperature range, degree of isolation, and in terms of the many performance specifications. Some are high-performance modules, most are monolithic ICs (including precision dual devices), some are hybrid ICs.

The technical data in this volume embrace exceptionally high-performance (low-drift and high-speed) operational amplifiers, in the form of small encapsulated modules. As the Selection Guide indicates, there is also a universe of technical data, to be found in Volume I, on a wide range of monolithic and hybrid operational amplifiers—including devices screened to the requirements of MIL-STD-883B and chips for hybrid assembly.

BACKGROUND

The operational amplifier is today the most-widely used analog subassembly. It is safe to say that its *basic* properties and applications are sufficiently understood by most circuit designers and builders. However, the basis for choice, the subtleties of using op amps in circuits for best results (especially in precision measurement and control), and the varieties of possible applications are less clearly understood by op amp users, in varying degrees.

In these few pages, we shall address the question of making a proper choice of op amp type for an application, in relation to the extensive array of device properties presented in the data sheets that follow.

For those users requiring basic tutorial material, and detailed information on getting the most out of op amps, we have provided on page 4–16 a bibliography that should make available up to 99% of information need now and then, with "fanout" to the vast body of literature that — with some redundancy — will provide the remainder. It should come as no surprise to successful users of Analog Devices op amps that a number of the references are to the applications sections of data sheets included in Volume I or Volume II of this catalog.

SELECTION PRINCIPLES

In selecting the right device for a specific application, you should have clearly in mind your design objectives and a firm understanding of what published specifications mean. Beyond this, you should detail the significant variables that are pertinent to your application. The purpose of this section is to put these many decision factors into perspective to help you make the most meaningful buying decisions.

To properly choose an operational amplifier for any given set of requirements, the designer must have:

1. *A complete definition of the design objectives.* Signal levels, accuracy desired, bandwidth requirements, circuit impedance, environmental conditions and other factors must be well defined before selection can be effectively undertaken.

2. *Firm understanding of what the manufacturer means by the numbers published for the parameters.* Frequently, any two manufacturers may have comparable published specifications, which may have been arrived at using differing measurement techniques. This creates a pitfall in op amp selection. To avoid these difficulties, the designer must know what the published specifications mean and how these parameters are measured and then must be able to interpret these published specifications in terms meaningful to the design requirements.

There are three fundamental aspects to the rational selection of an operational amplifier for a given application: (1) establishing the circuit architecture, (2) defining the performance levels, and (3) choosing the amplifier(s).

1. To obtain a circuit building block to implement a defined functional job, the principal choices are either to purchase a committed functional device or to design a circuit employing op amps to perform the function. For example, to obtain a difference between two voltages, one may either purchase an instrumentation or isolation amplifier, or design a suitable subtraction circuit using op amps. If a committed functional building block, with appropriate specs and price, is not available, the circuit designer must start by developing schematic diagrams of circuits that will perform the function simply using "ideal" operational amplifiers. Many commonly used circuits can be found in textbooks, "cookbooks", and linear circuit books, as well as in application notes and data sheets.

2. Recognizing that the choice of an op amp depends on both the overall circuit requirements and the characteristics of available op amps, the designer should interpret the desired overall performance in terms of the parameters of op amps, and establish acceptable ranges of parameters, and their variation with time, temperature, supply voltage, etc. Examples of the key parameters are the input offset voltage, input bias and offset currents, and the high-frequency performance and transient behavior of the op-amp block (and its effect on the closed-loop circuit) for large and small signals. It will be helpful to develop an application checklist, which includes such considerations as the character of the input signals and their impedance, the output load, the desired accuracy — static and dynamic — and the environmental conditions.

3. The designer must then relate acceptable performance of the op-amp building block to the specifications and prices of available devices from preferred suppliers, bearing in mind a

*In addition to the products listed in the Selection Guide, which are recommended for new designs, a number of older products are still available; data sheets are available upon request.

firm understanding of the way in which manufacturers define their specifications, and how definitions can differ in a way that may be misleading. A set of definitions used by Analog Devices follows the next section.

APPLICATION CHECKLIST

By way of an application checklist, the designer will need to account for the following:

Character of the application: The character of the application (inverter, follower, differential amplifier, etc.) will often influence the choice of amplifier.

Chopper stabilized amplifiers, for example, have not often been generally applicable where differential inputs are required.

Accurate description of the input signal: It is extremely important that the input signal be thoroughly characterized. Is the input a voltage source or a current source? Range of amplitude? Source impedance? Time/frequency characteristics?

Environmental conditions: What is the maximum range of temperature, time, and supply voltage over which the circuits must operate (to the required accuracy) without readjustment?

Accuracy desired: The accuracy requirement determines the extent to which the foregoing considerations are critical, and ultimately points the way to a device (or series of devices) which are acceptable. Accuracy must, of course, be defined in terms meaningful to the application with regard to bandwidth, dc offset, and other parameters.

SELECTION PROCESS

In general, the objective of amplifier selection should be to choose the least expensive device which will meet the physical, electrical, and environmental requirements imposed by the application. This suggests that a "General Purpose" amplifier will be the best choice in all applications where the desired performance requirements can be met. Where this is not possible, it is generally because of limitations encountered in two areas – bandwidth requirements, and/or offset and drift parameters.

To make it easier to relate bandwidth requirements with the drift and offset characteristics, a capsule view of bandwidth considerations precedes the DC discussions below. The reader is then returned to an expanded discussion of gain-bandwidth considerations.

Gain Bandwidth Considerations, A Capsule View

Although all selection criteria must be met simultaneously, determination of the bandwidth requirements is a logical starting point because:

A) If DC information is not of interest, a suitable blocking capacitor can be connected at the amplifier input and all of the "drift" specifications may usually be ignored, and

B) Where high frequency (>10MHz) characteristics are of primary importance, the choice will be limited to those amplifiers designated "Wide Bandwidth/Fast Settling."

Where DC information is required and where frequency requirements are relatively modest (full power response below 100kHz, unity gain of less than 1.5MHz) other criteria will probably influence the final choice. It is important, however, to choose an amplifier with which an adequate value of loop gain is assured (at the maximum frequency of interest) to obtain the desired accuracy. Loop gain is the excess of open loop gain over closed loop gain, and is responsible for the diminishing error due to fluctuations in the open loop gain due to time, temperature, etc. For example, if the closed-loop gain is 1000, the open-loop gain must be at least 100,000 to yield an error of no more than 1%, and 1,000,000 to yield an error no greater than 0.1%. Where undistorted response is required, the specifications for full linear response and slewing rate should be chosen such that they are not exceeded at the highest frequency of operation.

Offset and Drift Considerations

In the majority of op-amp applications, final selection is determined by the DC offset and drift characteristics. To undertake amplifier selection in these cases, it is necessary to translate the requirements listed earlier as follows. (It is assumed that bandwidth requirements and temperature range have been established at this point.)

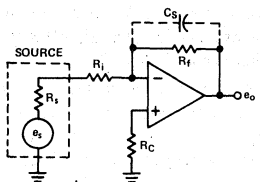
1. *What input impedance must the circuit present to the signal source?* This depends primarily on the source impedance, R_S, and the amount of loading error which is acceptable. Most amplifier circuits are designed around either the inverting or noninverting circuit of Figure 1. The choice is often made between the two to accommodate the impedance requirement. Input impedance for the inverting circuit is approximately equal to the summing impedance, R_i and the upper limit on the magnitude of R_i is determined by the allowable drift error because of input bias current as discussed below. The noninverting circuit offers inherently higher input impedance than the inverting circuit (due to "bootstrapping" feedback) and in this case input impedance is approximately equal to the common mode impedance of the amplifier R_{cm}.

2. *How much drift error can be tolerated?* The question is related to the input signal level, e_s, and the required accuracy For example, to amplify or otherwise manipulate a DC input signal of one volt with an accuracy of 0.1%, the offset drift error, V_d, must be one millivolt or less. (This assumes that other sources of error such as input loading, noise and gain error have already been allowed for.) By the same reasoning, the allowable drift error for a 1 volt signal and 0.01% accuracy would be 100μV.

When this has been defined, the allowable limits of offset

voltage (e_{os}), bias current (i_b), and difference current can be calculated by the equations of Figure 1. These equations relate offset voltage (e_{os}), bias current (i_b), difference current (i_d) and the external circuit impedances to the drift error, V_d, for both the inverting and the noninverting circuits. From these equations it can be seen how the input impedance requirements of the foregoing paragraphs are related to the drift error.

For example, in the case of the inverting circuit, a referred offset error voltage, $i_b R_i = e_{out}\left(\frac{R_i}{R_f}\right)$, is generated by the bias current flowing through the feedback impedance. This error increases for increasing R_i. Since R_i also sets the input impedance, there is a conflict between high input impedance and low offset errors. Likewise, for a given offset error, higher values for R_i can be used with an amplifier which has lower bias current.



$$e_o = -\frac{R_f}{R_i}\left[e_s + e_{os}\left(\frac{R_f + R_i}{R_f}\right) + I_b R_i\right]$$

For $R_C = 0$ and $R_s \ll R_i$

Signal | Input Drift Error = V_d

$$e_o = -\frac{R_f}{R_i}\left[e_s + e_{os}\frac{R_f + R_i}{R_f} + i_d R_i\right]$$

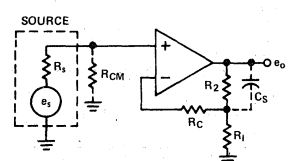
For $R_C = R_i R_f/(R_i + R_f)$ and $R_s \ll R_i$

Signal | Input Drift Error = V_d

Input Impedance $R_{IN} \approx R_i$

$$\% \text{ Drift Error} = \frac{100 V_d}{e_s}$$

Figure 1A. Inverting Configuration



$$e_o = \frac{R_2 + R_i}{R_i}\left[e_s + e_{os} + i_b R_s\right] \text{ for } R_C = 0$$

Signal | Drift Error = V_d

$$e_o = \frac{R_2 + R_i}{R_i}\left[e_s + e_{os} + i_d R_s\right] \text{ for } R_C = R_s - \frac{R_i R_2}{R_i + R_2}$$

Signal | Drift Error = V_d

Input Impedance $R_{IN} \approx R_{CM}$

$$\% \text{ Drift Error} = \frac{100 V_d}{e_s}$$

Figure 1B. Noninverting Configuration

Where it will otherwise function properly, the noninverting circuit generally makes a better choice for high input impedance circuits. Also, for the same source and input impedance requirement, a given amplifier will generate lower offset errors for the noninverting circuit than for the inverting circuit. This is so because the bias current flows only through R_s for the noninverter and this will always be less than the input impedance, R_i, of the inverter. Input impedance of the noninverter (approximately R_{CM}) is typically 10^7 ohms even for the least expensive bipolar amplifiers and up to 10^{11} ohms for FET types.

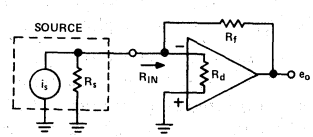
Unfortunately, however, the noninverting configuration cannot always be used since it is not convenient to use for many circuit functions such as integration or summation. A further limitation occurs in high accuracy applications, where common mode errors may rule out this circuit configuration.

Initial offset can usually be zeroed at room temperature so that only the maximum temperature excursion (ΔT) from +25°C need be considered. For example, over the range of -25°C to +85°C, the maximum temperature excursion (ΔT) from +25°C would be 60°C. As a practical matter, offset errors due to supply voltage and time drift can generally be neglected since errors due to temperature drift are usually much greater.

Current Amplifier Considerations

Before leaving the subject of offset errors, we shall discuss briefly the current amplifier configuration which is shown in Figure 2A. The obvious approach to measuring current is to develop a voltage drop across a load resistor, R_f, and to measure this potential with a high impedance amplifier as shown in Figure 2B.

This approach has several disadvantages as compared to the circuit of Figure 2A. First the noninverting amplifier introduces common mode errors which do not occur for Figure 2A. Second, an ideal current meter would have zero impedance whereas, R_f in Figure 2B may become very large since this resistor determines the sensitivity of the measurement. Third, the changes of input impedance, R_{cm}, for the noninverting amplifier with temperature will cause variable loading on R_f and hence a change in sensitivity.



$$e_o = -R_f\left[i_s + e_{os}\left(\frac{R_f + R_s}{R_s R_f}\right) + i_b\right]$$

Signal | Drift error = $I\epsilon$

Input Impedance $R_{IN} = \left(\frac{R_f R_d}{R_f + R_d}\right)\left(\frac{1}{1 + A\beta}\right)$

where $1/\beta = 1 + \frac{R_f (R_s + R_d)}{R_s R_d}$ % Drift Error = $\frac{100\, I\epsilon}{i_s}$

Figure 2A. Current Amplifier

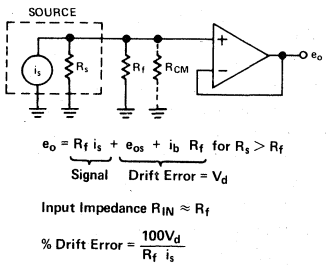


Figure 2B. Voltage Amplifier with Sampling Resistor

The current amplifier of Figure 2A circumvents all of these difficulties and approaches an ideal current meter; that is, there is essentially no voltage drop across the measuring circuit, since with enough open loop gain, A, the input impedance R_{IN} becomes very small.

In selecting a current amplifier, the most important consideration is current noise, and bias current drift. Measuring accuracy is largely the ratio of current noise and drift to signal current, i_s. To obtain the drift of error current I_ϵ referred to the input, use the following expression.

$$\Delta I_\epsilon = \left[\frac{\Delta e_{os}}{\Delta T}\left(\frac{R_f + R_s}{R_f R_s}\right) + \frac{\Delta i_B}{\Delta T}\right]\Delta T$$

Now, to make a proper selection you must pick an amplifier with an error current, I_ϵ, over the operating temperature which is small compared to the signal current, i_s. Do not overlook current noise which may be more important than current drift in many applications.

Gain Bandwidth Considerations, Expanded Discussion

From the previous discussion, it is apparent that most general purpose operational amplifiers will usually give adequate performance for the DC and audio frequency range applications. However, to obtain unity gain bandwidth above 2MHz, full power response above 20kHz and slewing rate above 6V/μsec, in general, requires special design techniques. All amplifiers with wideband, fast response characteristics have been listed in the wide bandwidth group to simplify the selection for higher frequency applications.

One factor often overlooked is that stray capacitance and impedance levels of the external feedback circuit can be the major limitation in high frequency applications. For example, in Figure 1A, if R_f were one megohm, and stray capacitance, C_S, were one picofarad then the closed loop bandwidth would be limited to 160kHz ($1/(2\pi R_F C_S)$) regardless of how fast the amplifier is. Moreover, output slewing rate will be limited by how fast C_S can be charged which in turn is related to signal level, e_s, and input impedance, R_i, by $de_o/dt = -e_s/R_iC_s$. For these reasons it is usually not possible to obtain both fast response and high input impedance for an inverting circuit since both R_i and R_f must be large to obtain high input impedance.

Another advantage of the noninverting circuit (Figure 1B) is that input impedance, being determined by potentiometric feedback, does not depend on the impedance levels for R_1 and R_2. Therefore, a low impedance can be used for R_2 so that stray capacitance of C_S will not limit the circuit's bandwidth. In this case the minimum value for R_2 is constrained only by the output current rating of the amplifier. Again the trade-off between the frequency response and input impedance of the inverting and noninverting circuits must be evaluated in light of the common mode rejection error introduced by the noninverter.

For greater emphasis wideband applications can be separated into two categories – steady state and transient. Since the amplifier requirements for the two are somewhat different, these categories will be discussed separately.

A. Steady State Applications

Steady state applications involve amplifying or otherwise manipulating *continuous* sinusoidal, complex or random waveforms. In these applications the significant issues in choosing an amplifier are as follows:

1. *Is DC coupling required?* If DC information is of no consequence, then the offset drift errors are not usually important and a capacitor can be used if necessary to block the output DC offset. Your only concern here is that DC offset at the output does not become so large, as might be the case with a high gain stage, that the output is saturated or the dynamic swing for AC signals is limited. One way to circumvent the latter problem is to use feedback to limit the gain at DC as shown in Figure 3. The gain of these circuits can be small at DC but large at high frequencies.

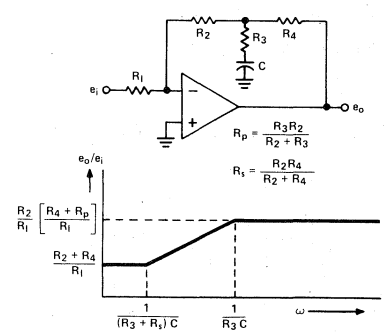


Figure 3. DC Feedback Minimizes Output Offset for AC Applications

2. *What closed loop gain and bandwidth are required?* Closed loop gain, G, is dictated by the application. To a first approximation the intersection of the open and closed loop gain curves in Figure 4 gives the closed loop bandwidth, f_{c1}(–3dB). For high gain, wideband requirements, it may be necessary, or more economical, to use two amplifiers in cascade, each at lower gain.

3. *What loop gain is required or alternatively what gain stability, output impedance and/or linearity are necessary?* The available loop gain at a particular frequency or over a range of frequencies is very often more important than closed loop bandwidth in selecting an amplifier. Loop gain as illustrated in Figure 4, is defined as the difference, in dB, or as the ratio, arithmetically, of the open to closed loop gain ($A\beta$ = A/G). You will find in most of the equations defining the closed loop characteristic of a feedback amplifier that the loop gain ($A\beta$) is the determining factor in performance. Some of the more notable examples of this point are as follows:

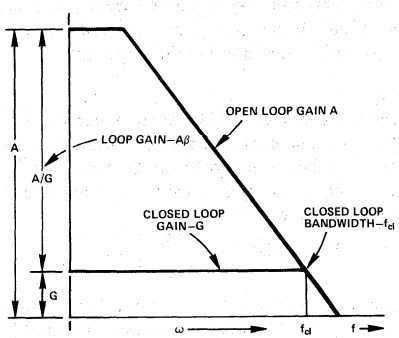


Figure 4. Closed Loop Bandwidth and Loop Gain

a. Closed loop gain stability = $\Delta G/G$
$\Delta G/G = (\Delta A/A)\ [1/(1 + A\beta)]$ where $\Delta A/A$ is the open loop gain stability, usually about 1%/°C.

b. Closed loop output impedance = $Z_{ocl} = Z_o/(1 + A\beta)$, where Z_o is the open loop output impedance, often 200 to 5000 ohms.

c. Closed loop nonlinearity = $L_{cl} = L_{ol}/(1 + A\beta)$, where L_{ol} is the open loop linearity, usually less than 5%.

Loop gain of 100, or 40dB, is adequate for most applications and this is readily achievable at DC and low frequencies. But note that loop gain decreases with increasing frequency which makes it difficult to obtain large loop gains at high frequencies. For this reason it may be necessary to use a 10MHz unity gain amplifier in order to obtain adequate feedback over a 10kHz bandwidth.

4. *What full power response and/or slew rate are required?* You should examine your expected output waveform and select an amplifier whose slewing rate exceeds the maximum rate of change of output signal. For a sinusoidal waveform with a peak voltage output equal to the rated amplifier output the frequency should not exceed f_p, the full power response of the amplifier. As the output signal voltage is reduced below the rated output voltage, the usable maximum frequency can be extended proportionately. If you do not observe these restrictions you will get distortion and unexpected DC offsets at the output of the amplifier.

For some monolithic amplifier designs available today their frequency response is not a simple 6dB roll-off; the response may be shaped with external RC components for improved performance, using a *compensation* terminal provided. Using feedforward or phase lag compensation networks, gain-bandwidth product and/or full power response may be shaped to meet varying design requirements. Most internally compensated op amps offer a stable 6dB per octave roll-off with specified unity gain-bandwidth and slew rate thereby limiting maximum speed and response to those published specifications.

B. Transient Applications

In applications such as A/D and D/A converters and pulse amplifiers, the *transient response* of the wideband amplifier is generally more important than the *gain bandwidth* characteristic described above. Slewing rate, overload recovery and settling time are the specifications which determine the transient response.

When applying the high frequency amplifier, it is important to understand how amplifier performance is affected by component selection as well as impedance levels used around the amplifier.

Settling Time

Settling time is defined as the time elapsed from the application of a perfect step input to the time when the amplifier output has entered and remained within a specified error band symmetrical about the final value (Figure 5). Settling time therefore includes the time required for the amplifier to slew from the initial value, recover from slew rate limited overload, and settle to a given error in the linear range.

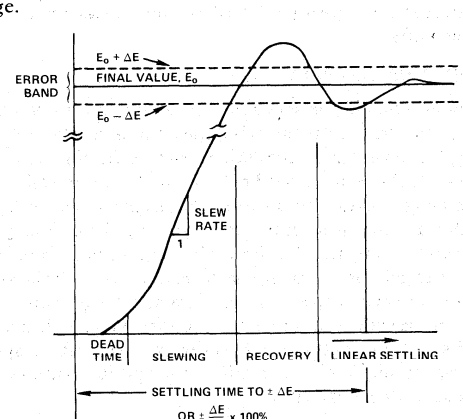


Figure 5. Typical Settling Time Characteristics

The time and frequency response of a linear, bilateral network or amplifier are related by well known mathematics. For example, the step response for a well behaved, ideally linear, 6dB/octave amplifier with a closed loop bandwidth of ω_{cl} is shown in Figure 6.

However, since settling time is determined by a combination of amplifier characteristics (both linear and nonlinear) and because it is a closed loop parameter, it cannot be readily predicted from the open loop specifications such as slew rate, small signal bandwidth, etc.

Analog Devices specifies settling time for the condition of unity gain, relatively low impedance levels, and no capacitive loading. A full-scale step input is used to determine settling time and the step is generally unipolar – i.e.: from zero to plus or minus full scale. The settling time indicated is generally the longest time resulting from a step of either polarity and is given as a percentage of the full scale step transition.

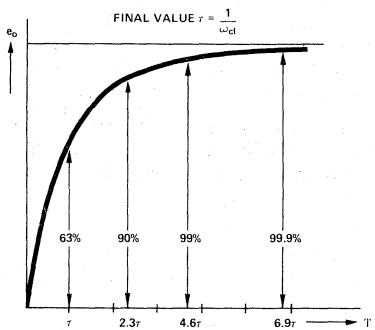


Figure 6. Step Response for Linear 6dB/Octave Amplifier

Settling time is a nonlinear function. It varies with the input signal level and it is greatly affected by impedances external to the amplifier.

ERRORS DUE TO NOISE

A major criterion in the selection of an amplifier for low level signals is the amplifier input noise, since this is usually the limiting factor on system resolution. In the general case, amplifier noise can be characterized by a voltage source in series with the summing junction and a current source in parallel with the summing junction. Whenever high source impedance is encountered, current noise flowing through the source impedance will appear as an additional voltage noise, combining with the amplifier voltage noise. The root-square sum of these (uncorrelated) noise sources will then be amplified along with the desired signal. For this reason, selection of a particular amplifier must consider both the amplifier noise performance as well as the source impedance.

Consideration must also be given to noise sources other than the amplifier whenever determining total system noise. RF noise may be fed into an amplifier through any connecting wire, including power supply and output leads. A quiet power supply (nonswitching), adequate shielding, and low-pass filters on all incoming leads will usually prevent noise pick-up.

Thermal noise is generated in any conductor or resistor as a result of thermal agitation of the electrons. This noise voltage source, sometimes referred to as "Johnson Noise", is generated in the resistive component of any impedance and has a value:

$e_n = \sqrt{4KTBR}$

where e_n = the rms value of the noise voltage

K = Boltzmann's Constant (1.38×10^{-23} joules/kelvin)

T = absolute temperature of the resistance, kelvin

B = the bandwidth in which the noise is measured

Since noise is related to the bandwidth over which the measurement is made, no noise specification is meaningful unless the bandwidth for the specification is given. Although the Thermal Noise equation may appear unwieldy for practical noise calculations, all that is required to enable rapid approximations is to apply a few simple rules of thumb.

Rules of Thumb

(1) Remember that a 100kΩ resistor generates 40nV rms in a 1Hz bandwidth. The noise voltages generated by other values of resistances in other bandwidths can be calculated by remembering that the noise is proportional to the square root of the resistance and the bandwidth; i.e.

$$e_n \text{ (rms)} = (40nV/\sqrt{Hz})\left(\sqrt{\frac{R}{100k\Omega}\ (BW)}\right)$$

(2) To convert the rms noise to a p-p value, a conversion factor of 6.6μV p-p/μV rms is applied for less than 0.1% probability of noise peaks exceeding calculated limits.

(3) The total rms noise contribution due to several uncorrelated random noise sources is determined by the square root of the sum of the squares (RSS):

$$e_t = \sqrt{e_a^2 + e_b^2 + e_c^2 + \ldots e_n^2}$$

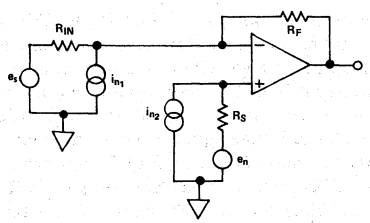
If any noise source is less than a third of another, it may be neglected. The resulting error will be approximately 5%.

(4) Restricting the bandwidth of a system to the minimum usable and using the lowest impedances possible are ways to reduce noise.

DESIGN EXAMPLE

Figure 7A illustrates a typical circuit with noise calculations shown for each noise source. The total of the noise sources is obtained by adding each of the individual sources in RSS fashion.

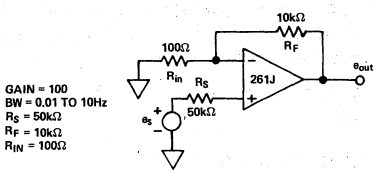
Figure 7B illustrates how the Rules of Thumb may be applied in a practical case to approximate the total output noise. In this example, model 261J, the lowest noise non-inverting chopper type amplifier is being used with a 50kΩ source impedance. The two major noise sources, in addition to the 261J input voltage noise of 1μV p-p, are the Johnson noise (58μV p-p) and current noise (100μV p-p).



COMPONENT	CAUSE	OUTPUT CONTRIBUTION
R_{IN}	Johnson Noise	$\sqrt{4KTBR_{IN}}\ (R_F/R_{IN})$
R_S	Johnson Noise	$\sqrt{4KTBR_S}\ (R_F/R_{IN}+1)$
R_F	Johnson Noise	$\sqrt{4KTBR_F}$
i_{n_1}	Amp. Current Noise	$i_{n_1} R_F$
i_{n_2}	Amp. Current Noise	$(i_{n_2} R_S)\ (R_F/R_{IN}+1)$
e_n	Amp. Voltage Noise	$e_n\ (R_F/R_{IN}+1)$

$$\text{TOTAL NOISE} = \sqrt{(e_{R_{IN}} G)^2 + [e_{R_S}(G+1)]^2 + e^2 R_F + [(i_{n_1} R_F)^2] + [(i_{n_2} R_S)(G+1)]^2 + [e_n (G+1)]^2}$$

Figure 7A. Noise Components



1) RESISTOR NOISE: $R_F \rightarrow 13nV/\sqrt{Hz}$
$R_{IN} \rightarrow (1.3nV/\sqrt{Hz})\ 100$
$R_S \rightarrow (28nV/\sqrt{Hz})\ 101 = 2.8\mu V/\sqrt{Hz}$
TOTAL RESISTOR NOISE IN 10Hz BW =
$(2.8\mu V/\sqrt{Hz})\ (\sqrt{10Hz})$ 6.6μV p-p/μV rms = 58μV p-p

2) AMPLIFIER CURRENT NOISE: (20pA p-p) (50k) (101) = 100μV p-p
(20pA p-p) (10k) = 0.2μV p-p

3) AMPLIFIER VOLTAGE NOISE: (1μV p-p) (101) = 100μV p-p

TOTAL OUTPUT NOISE = $\sqrt{(100)^2 + (100)^2 + (58)^2} \approx 150\mu V$ p-p

Figure 7B. Design Example

THE SELECTION GUIDE

To assist the designer in rapidly distinguishing among the many types available from Analog Devices, and to narrow the field of further study to just a few types, the Selection Guide takes the form of a "bullet chart". One axis comprises a list of key op-amp characteristics—including manufacturing technology—and specification ranges; the other is the complete set of op-amp families catalogued in both volumes. For any specification level that can be satisfied by members of a given device family, a bullet (•) is placed at the appropriate intersection.

Once the required performance has been established, the Selection Guide is used to find the family, or families, coming closest to the requirements—or to determine quickly whether a particular family is suitable. The exact volume, section, and page location of each type is included in the table, so that the detailed technical and application data can be consulted with a minimum of effort.

An effort has been made to group the amplifiers by their most salient application areas, i.e., General Purpose (low cost), High Accuracy, and Fast/Wideband, and by appropriate subclasses within those major classes.

THE AMPLIFIERS IN THIS SECTION IN BRIEF

High-Accuracy Low-Drift Differential-Input Modules. "Chopperless" low-drift designs with differential FET inputs, optimized for voltage offset and drift, bias current, dc open-loop gain, and CMR, should be considered for high-accuracy instrumentation, low-level transducer bridge circuits, precision voltage comparators, and for impedance buffer designs. The best overall performer in this group in high-impedance applications is the model 52K, which combines low offset and drift (0.5mV and 1μV/°C) with 3pA bias current.

High-Accuracy Modules Using Chopper Techniques. The amplifiers in this class are widely accepted as the best choice when it is essential to maintain low voltage offsets and bias currents with time and temperature or whenever external offset adjustments are not practical in the application. Using carrier modulation techniques, these designs achieve drifts to 0.1μV/°C and long-term stability to ½μV/mo. Typical applications include error-summing amplifiers for servo loops, precision regulators, and input amplifiers for laboratory-grade metering instruments and test equipment.

Two forms of amplifier are available. The *noninverting chopper-amplifier* (261 family) is a high gain feedback amplifier, containing a MOSFET chopper, optimized for follower-with-gain applications. The chopper converts the difference between the dc or low-frequency input voltage, at high impedance, and the feedback voltage to a high-frequency square-wave, amplifies it with no drift, and demodulates and filters the result to produce an output waveform that is an amplified version of the input. The closed-loop gain is determined by the attenuation ratio of the feedback resistor-pair.

The initial offset is ±25μV max (trimmable to zero), with average drift-vs.-temperature of 0.1μV/°C max (model 261K). Bias current is respectable, at 300pA max, with a tempco of 10pA/°C max, to minimize errors with high-impedance sources.

Maximum noise voltage is 0.4μV peak-to-peak, from 0.01 to 1.0Hz, and 1.0μV, from 0.01 to 10Hz. Small-signal bandwidth, established by an external compensating capacitor that is chosen as a function of gain, is 100Hz.

Inverting chopper-stabilized amplifiers (234/235 family) employ narrow-band chopper amplifiers to measure the summing-point voltage of the main amplifier (which should be at a null), chop, amplify, filter, and feed to the positive input of the main amplifier an amplified correction signal. Thus, the offset voltage and drift of the main amplifier (including the effects of input bias current) are reduced by the gain of the chopper amplifier, without a corresponding reduction of bandwidth.

Chopper and chopper-stabilized amplifiers should be considered when long-term stability must be maintained with time and temperature, and wherever maintenance-free operation of instruments and remote circuits is essential. Typical applications include amplification of microvolt-level signals, precision integration, and analog computing.

Wide Bandwidth, Fast-Settling Modules. High-speed op amps are characterized by high slewing rates, fast settling time, and wide bandwidth. Fast settling time is especially important in applications with rapidly changing or switched analog data, in buffers, d/a converters, and multiplexer circuitry; wide small-signal bandwidth is important in preamplification and in handling low-level wideband ac signals; high slewing rate is associated with fast settling time and is also important in handling ac signals having large magnitudes with minimal distortion, since the large-signal bandwidth is closely related to the slewing rate.

The products in this category with outstanding specifications are models 50J/K and 48J/K. Model 50's max slewing rate is 500V/μs inverting, 400V/μs noninverting, and small-signal unity-gain bandwidth is 70MHz; full-power bandwidth is 8MHz, min. In addition, these devices will deliver ±100mA of output current at ±10V, an important factor in video and line-driver circuitry, and in driving capacitive loads. For example, the current required to sustain 500V/μs in a 100pF load is I = C dV/dt = 50mA. Model 48J/K is optimized for settling time: 500ns maximum to 0.01%, inverting or noninverting, with output of ±20mA at ±10V.

Differential FET-Input High-Out Modules. This beefy group includes models 50, 51, and 171. Models 50 and 51 will furnish up to ±100mA at ±10V out. In addition both are excellent wideband amplifiers. Besides the applications suggested for them in the wide-bandwidth category, they are useful for such applications as current booster/buffer for op amps dealing with low-level signals—either outside the loop or inside the loop. They are protected against short circuits.

For extended-temperature-range operation, model 51A/B operates from -25°C to +85°C.

The model 171 has a large output voltage swing, ±140V at ±10mA, when used with ±150V supplies. However, it need not operate symmetrically; any combination of power-supply voltages between the limits of 15 to +300V for the positive side and -15 to -300V for the negative side is acceptable (including single-supply operation), provided that the total voltage across the amplifier is within the range of 30 to 300V. The output will swing to within 10V of the V_S^+ and V_S^- supply rails. The output and both inputs are protected against short circuits to common or to either supply. Model 171K has an open-loop gain of 10^6 min, offset of 1mV, drift of 15μV/°C max, bias current of 20pA max, CMR of 100dB min, unity-gain small-signal bandwidth of 3MHz, and slewing rate of 10V/μs. Typical applications include high compliance-voltage current source, high-voltage follower-with-gain, high-voltage integrator, differential amplifier for high-common-mode-voltage bridge applications, and high-voltage reference supply.

Isolated Operational Amplifier Module. Model 277 (see Section 5) combines a high-performance uncommitted operational-amplifier input stage with a precision, isolated output stage, an isolated dual ±15V power supply, and transformer-coupled isolation circuitry, to form a versatile isolation amplifier. It is rated to withstand input/output common-mode voltage of 3500V rms max (60Hz, 1 minute), and peak continuous ac or dc of ±2500V max, and has input-output CMR of 160dB min at dc and 120dB min at 60Hz, with leakage current of 1μA @ CMV of 115V rms, 60Hz ($Z_L = 10^{12}\Omega||16pF$).

The input-stage performance makes many op-amp applications feasible: ±1μV/°C max offset tempco (trimmed, model 277K), bias current of ±20nA max, open-loop gain of 106dB min. In addition, isolated power output of ±15mA max at ±15V, referred to input common, is available for auxiliary front-end circuitry. The output stage has gain of 1V/V, nonlinearity of 0.05% max, 1.5kHz full-power bandwidth, and 50μV/°C offset tempco.

Typical applications for the 277 include general isolated op-amp circuitry, programmable-gain isolated amplifier, isolated power source and amplifier for bridge measurements, instrumentation amplifier, instrumentation-grade process-signal isolator, and current-shunt measurements.

The extended-temperature-range equivalent of models 277J/K is model 277A.

DEFINITIONS OF SPECIFICATIONS

Absolute Maximum Differential Voltage
Under most operating conditions, feedback maintains the error voltage between inputs to nearly zero volts. However, in some applications, such as voltage comparators, the voltage between the inputs can become large. This specification defines the maximum voltage which can be applied between inputs without causing permanent damage to the amplifier.

Common-Mode Rejection
An ideal operational amplifier responds only to the difference voltage between inputs ($e^+ - e^-$) and produces no output for a *common-mode voltage*, that is, when both inputs are at the same potential. However, due to slightly different gains between the plus and minus inputs, or variations in offset voltage as a function of common-mode level, common-mode input voltages are not eliminated at the output. If the output error voltage, due to a known magnitude of common-mode voltage, is referred to the input (dividing by the closed-loop gain), it reflects the equivalent *common-mode error voltage* (CME) between the inputs. Common-mode rejection ratio (CMRR) is defined as the ratio of common-mode voltage to the resulting common-mode error voltage. Common-mode rejection is often expressed logarithmically: CMR (in dB) = 20 $\log_{10}$ (CMRR).

The precise specification of CMR is complicated by the fact that the common-mode voltage error can be a highly nonlinear function of common-mode voltage and also varies with temperature. As a consequence, CMR data published by Analog Devices are average figures, assuming an end-point measure-

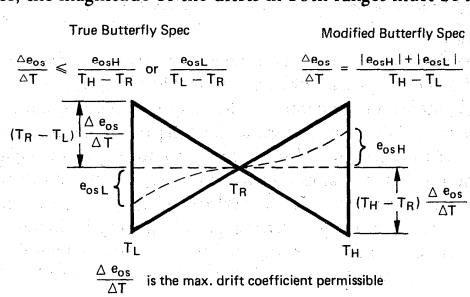
ment over the common-mode range specified. The incremental CMR about small values of common-mode voltage may be greater than the average CMR specified (on the other hand, the incremental CMR may be less in the neightborhood of large CMV). Published CMR specifications for op amps pertain to very low-frequency voltages, unless specified otherwise; CMR decreased with increasing frequency.

Common-Mode Voltage, Maximum
For differential-input amplifiers, the voltage at both inputs can swing about ground (power-supply common) level. *Common-mode voltage* is defined as any voltage (above or below ground) that could be observed at both inputs. The maximum common-mode voltage is defined as that voltage which will produce less than a specified value of common-mode error. This establishes the maximum input voltage for the voltage-follower connection.

Drift vs. Supply
Offset voltage, bias current, and difference current vary as supply voltage is varied. Usually, dc errors due to this effect are negligible compared to drift with temperature. No inference may be drawn from this low-frequency specification concerning the effects of rapid variation of voltage at the supply terminals.

Drift vs. Temperature
Offset voltage, bias current, and difference current all change, or "drift", from their initial values with temperature. This is by far the most important source of error in most precision applications. The temperature coefficients (tempcos) of those parameters are all defined as the average slope over a specified temperature range. Drift can be a nonlinear function of temperature (though it is often quite linear over limited temperature ranges); the slopes generally are greater at the extremes of temperature than around normal ambient (+25°C), which generally means that for small temperature excursions in the vicinity of +25°C, the specification is conservative.

Analog Devices precision operational amplifiers are specified by three- (or more-) point measurements, at 25°C and at the high and low extremes of the range (T_H, T_L), with the amplifier adjusted to zero at room temperature. The sum of the magnitudes of the drifts in the two ranges must be less than the specified drift rate (μV/°C or nA/°C) multiplied by the total temperature range (modified "butterfly"), or, in some cases, the magnitude of the drifts in both ranges must be less than the specified drift rate multiplied by the respective temperature ranges ("true butterfly").



The lowest-cost second-source IC amplifiers are specified only in terms of the maximum value of the parameter (e.g., offset voltage) over temperature in the specified range.

Drift vs. Time
Offset voltage, bias current, and difference current change with time as components age. It is important to realize that drift with time is random, and rarely – if ever – accumulates linearly for healthy devices. For example, voltage drift for a chopper-stabilized amplifier might be quoted at 1μV/day, whereas cumulative drift over 30 days might not exceed 5μV, or 15μV in a year (e.g., model 235). A convenient rule of thumb for extrapolation is to divide the drift for a stated interval by the square root of its ratio to any other interval of interest.

Full-Power Response
The large-signal and small-signal response characteristics of operational amplifiers differ substantially. An amplifier's output will not respond to large signal changes as fast as the small-signal bandwidth characteristics would predict, primarily because of slew-rate limiting in the output stages. Full-power response is specified in two ways: full linear response and full peak response. Full linear response is specified in terms of the maximum frequency, at unity closed-loop gain, for which a sinusoidal input signal will produce full output at rated load without exceeding a pre-determined distortion level. There is no industry-wide accepted value for the distortion level which determines the full-linear-response limitation, but we use 3% as a maximum acceptable limit for modules.

In many applications, the distortion caused by exceeding the full linear response can be comfortably ignored, but a more-serious effect (often overlooked) is an effect equivalent to a dc offset voltage that can be generated when full linear response is exceeded, due to rectification of the asymmetrical feedback waveform or overloading of the input stage by large distortion signals at the summing junction.

Another frequency response that is often of interest is the maximum frequency at which full output swing may be obtained, irrespective of distortion. This is termed "full peak response" and can often be found in a plot of output voltage swing vs. frequency.

Initial Bias Current
Bias current is defined as the current required at either input from an infinite source impedance to drive the output to zero (assuming zero common-mode voltage). For differential amplifiers, bias current is present at both the negative and the positive input. All Analog Devices specifications pertain to the *larger* of the two, *not the average.* For single-ended amplifiers (i.e., chopper types), bias current refers to the current at the input terminal.

Analog Devices specifies initial bias current, I_b, as the bias current at either input, specified at +25°C ambient with the input junctions *at normal operating temperature* (some manufacturers specify initial bias current at power turn-on. Such

specifications may be misleading. For example, in FET-input amplifiers, bias current is doubled for each 10°C increase; since junction temperatures may warm up to 20°C or more above ambient, the "initial bias current" spec used by some manufacturers may be met only during a brief interval after the power is burned on, and I_b may be quadrupled under ordinary operation conditions.)

Initial Difference Current

Difference current is defined as the difference between the bias currents at the two inputs. The input circuitry of differential amplifiers is generally symmetrical, so that bias currents at both inputs tend to be equal and tend to track with changes in temperature and supply voltage. Therefore, difference current is often about 0.1 times the bias current at either input, assuming that initial bias current has not been compensated at the input terminals. For amplifiers in which bias currents track, it is often possible to reduce voltage errors due to bias current and its variations by the use of equal resistance loads at both inputs.

Input Impedance

Differential input impedance is defined as the impedance between the two input terminals at +25°C, assuming that the error voltage is nulled or very near zero volts. To a first approximation, dynamic impedance can be represented by a capacitor in parallel with a resistor.

Common-mode impedance, expressed as a resistance in parallel with a capacitance, is defined as the impedance between each input and power-supply common, specified at +25°C. For most circuits, common-mode impedance on the negative input has little significance, except for the capacitance which it adds at the summing junction (one exception is electrometer circuitry). However, common-mode impedance on the plus input sets the upper limit on closed-loop input impedance for the non-inverting configuration. Common-mode impedance is a nonlinear function of both temperature and common-mode voltage. For FET-input amplifiers, common-mode resistance is reduced by a factor of two for each 10° of temperature rise. As a function of common-mode voltage, the resistive component is defined as the average resistance for a common-mode change from zero to the maximum common-mode voltage. Incremental resistance may be less than the specified average value, especially at full-scale for some FET-input amplifiers.

Input Offset Voltage

Offset voltage is defined as the voltage required at the input from zero source impedance to drive the output to zero; its magnitude is measured by closing the loop (using low values of resistance) to establish a large fixed gain, measuring the amplified error at the output, and dividing the measured value by the gain.

The initial offset voltage is specified at +25°C and rated supply voltage. In most amplifiers, provisions are made to adjust initial offset to zero with an external trim potentiometer.

Input Noise

Input voltage- and current-noise characteristics can be specified and analyzed in much the same way as offset-voltage and bias-current characteristics. In fact, long-term drift can be considered as noise which occurs at very low frequencies. The primary difference is that, when evaluating noise performance, bandwidth must be considered. Also rms noise from different sources is summed by root-sum-of-squares, rather than linear, addition. Depending on the amplifier design, noise may have differing characteristics as a function of frequency, being dominated by "1/f noise", resistor noise, or junction noise, at various frequencies.

For this reason, several noise specifications are given. Low-frequency noise in the band 0.01 to 1Hz (or 0.1 to 10Hz) is specified as peak-to-peak, with a 3.3σ uncertainty, signifying that 99.9% of the observed peak-to-peak excursions will fall within the specified limits. Wideband noise is specified as rms. For some types, spectral-density plots or "spot noise", at specific frequencies, in $\mu V/\sqrt{Hz}$ or $pA/\sqrt{Hz}$, are provided.

Open-Loop Gain

Open-loop gain is defined as the ratio of a change of output voltage to the voltage applied between the amplifier inputs to produce the change. Gain is specified at dc. In many applications, the frequency dependence of gain is important; for this reason, the typical open-loop gain as a function of frequency is published for each amplifier type. See also *unity gain small-signal response.*

Overload Recovery

Overload recovery is defined as the time required for the output voltage to recover to the rated output voltage from a saturated condition caused by a 50% overdrive. Published specifications apply for low impedances and contain the assumption that overload recovery is not degraded by stray capacitance in the feedback network.

Rated Output

Rated output *voltage* is the minimum peak output voltage which can be obtained at rated current or a specified value of resistive load before clipping or out-of-spec nonlinearity occurs. Rated output *current* is the minimum guaranteed value of current supplied at the rated output voltage (or other specified voltage). Load impedances less than the specified (or implied) value can be used, but the maximum output voltage will decrease, distortion may increase, and the open-loop gain will be reduced. (All models are short-circuit protected to ground, and many are safe against shorts to the supplies.)

Settling Time

Settling time is defined as the time elapsed from the application of a perfect step input to the time when the amplifier output has entered and remained within a specified error band symmetrical about the final value. Settling time, therefore, includes the time required for the signal to propagate through the amplifier, for the amplifier to slew from the initial value, recover from slew-rate-limited overload (if it occurs), and settle to a given error in the linear range. It may also include a "long tail" due to the time required to reach thermal equilibrium, or the settling time of compensation circuits. Settling

time is usually specified for the condition of unity gain, relatively low impedance levels, and no (or a specified value of) capacitive loading, and any specified compensation. A full-scale unipolar step input is used, and both polarities are tested.

Although settling time can generally be grossly inferred from the other amplifier specifications (an amplifier that has extra-wide small-signal bandwidth, extra-fast slewing, and excellent full-power response may reasonably – but not always – be expected to have fast settling), the settling time cannot usually be rationally predicted from the other dynamic specifications.

Slewing Rate

The slewing rate of an amplifier, usually in volts per microsecond (V/μs), defines the maximum rate of change of output voltage for a large input step change.

Unity-Gain Small-Signal Response

Unity-gain small-signal response is the frequency at which the open-loop gain falls to 1V/V, or 0dB under a specified compensation condition. "Small signal" indicates that, in general, it is not possible to obtain large output voltage swing at high frequencies because of distortion due to slew-rate limiting or signal rectification. For amplifiers with symmetrical response for signals applied to either input, the dynamic behavior will be consistent for both inverting and non-inverting configurations. However, if feedforward compensation is used, fast response will be available only on the negative input, restricting fast applications of the device to the inverting mode.

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ARTICLES AND APPLICATION NOTES (Available Upon Request; ask for specific issue of Analog Dialogue)

"Analog Signal Handling for High Speed and Accuracy" by A. P. Brokaw, ANALOG DIALOGUE 11-2

"Current Inverter with Wide Dynamic Range" by Barrie Gilbert, ANALOG DIALOGUE 9-1, 1975

"How to Select Operational Amplifiers", Application Note Section 21 of Volume I

"An IC-Amplifier User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change," by A. P. Brokaw, Application Note Section 21 of Volume I

"Laser-Trimming on the Wafer, A Powerful New Tool for IC's" by R. Wagner, ANALOG DIALOGUE 9-3, 1975

"Noise and Operational Amplifier Circuits" by L. Smith and D. Sheingold, ANALOG DIALOGUE 3-1, 1969

"Op Amps as Electrometers," ANALOG DIALOGUE 5-2, 1971

"Settling Time of Operational Amplifiers" by R. Demrow, ANALOG DIALOGUE 4-1, 1970

"Simple Rules for Choosing Resistance Values in Adder-Subtractor Circuits" by D. Sheingold, ANALOG DIALOGUE 10-1, 1976

"Specifying and Measuring a Low-Noise FET-Input IC Op Amp" by Bill Maxwell, ANALOG DIALOGUE 8-2, 1974

"How to Test Operational Amplifier Parameters", Application Note Section 21 of Volume I

USEFUL TUTORIAL MATERIAL IN DATA SHEETS

Electrometer Circuitry, see AD515 and Models 310/311

High-Speed Amplifiers, see AD518 and Models 50/51

Low-Drift Differential Op Amp Performance, see AD504

Low-Level Applications of Chopper-Stabilized Amplifiers:
Inverting, see Models 234, 235
Non-Inverting, see Model 261

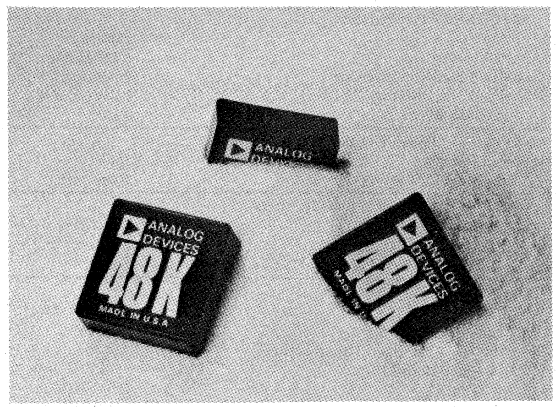
ANALOG DEVICES

Fast Settling Differential FET Op Amp

MODEL 48

FEATURES
- Fast Settling: 500ns max to 0.01%
- Fast Slew Rate: 125V/μs
- Wide Bandwidth: 15MHz
- High Common Mode Rejection: 83dB min
- High Gain: A_0 = 100,000 min
- Low Drift: 15μV/°C max

APPLICATIONS
- Stable Unity Gain Buffer to 15MHz
- Sample Hold Circuits
- Ultra Fast Current Source
- High Speed Integrator



GENERAL DESCRIPTION

The model 48 is an ultra fast, FET input differential op amp that should be considered where settling time, slew rate, bandwidth and good thermal stability are critical requirements. Characterized by a -6dB/octave rolloff to frequencies exceeding 15MHz, the model 48's dynamic response consists of a guaranteed slew rate of 110V/μs and settles to 0.01% in 500ns, max. For dc performance, the model 48 has open loop gain of 100,000 min, and common mode rejection at a full ±10V of 15,000 min (83dB). Maximum offset drifts of 50μV/°C (48J) and 15μV/°C (48K) complete the performance profile, proving this amplifier to be an excellent choice for both high speed analog and digital applications.

Packaged in a small 1 1/8" X 1 1/8" X 0.4" case, the model 48 requires little space, runs cool (9mA of quiescent current) and is competitively priced in unit quantities.

FAST SETTLING APPLICATIONS

A/D and D/A converters, multiplexers and other sampling circuits require fast settling output amplifiers. Since system conversion speed is most often dictated by the settling time of the amplifier, model 48, with a guaranteed 500ns settling time to 0.01%, makes it an excellent choice.

D/A CURRENT TO VOLTAGE CONVERTER

Current to voltage converters for D/A applications place severe requirements on the op amp's slew rate, open loop gain and offset drift. Model 48 meets these requirements with smooth settling to 0.01% in 500ns, open loop gain of 100,000 and offset drift of 15μV/°C (48K).

SETTLING TIME VS SIGNAL LEVEL

Shown in Figure 1 is a graph of settling time for various step inputs and the test circuit used to obtain this data. Settling time varies in a nonlinear fashion with input level, error band, and polarity of input step. The worst case settling is that which is specified at ±10V.

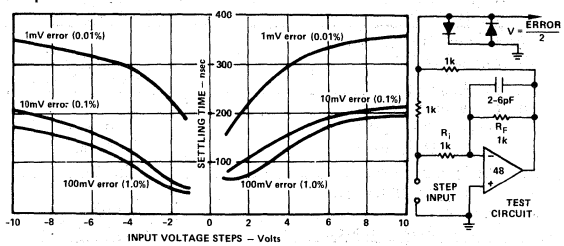


Figure 1. Settling Time for Various Input Steps

SETTLING TIME VS R_F AND C_L

Settling time of an amplifier is also influenced by the value of the gain resistors selected and the amount of capacitive loading. Model 48 is stable even when driving cap loads, C_L, up to 1000pF, but to obtain optimum settling time this value of capacitance should be held as low as possible. The effects of C_L and R_F on settling time are shown in Table 1.

TABLE 1. 0.1% SETTLING TIME VS R_F, C_L

$R_F = R_i$ (Ω)	t_s (nsec)	Cap Load (pF)
1k	350	6
10k	420	6
50k	560	6
2k	320	100
2k	420	200
2k	1100	500

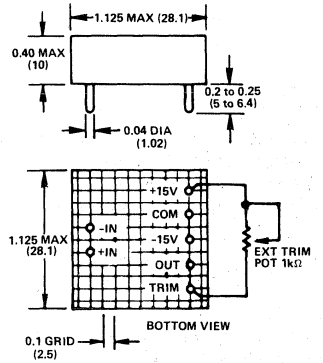
SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

MODEL	48J (K)
OPEN LOOP GAIN	
DC Load 500 ohms	100,000 min
RATED OUTPUT[1]	
Voltage, 500 ohm Load	±10V min
Current	±20mA min
Maximum Load Capacitance	1000pF
FREQUENCY RESPONSE	
Unity Gain	15MHz
Full Power	1.5MHz min
Slew Rate, Non-Inverting	90V/μs min
Slew Rate, Inverting	110V/μs min
Overload Recovery	0.5μs
SETTLING TIME, UNITY GAIN, 0.01%	
Non-Inverting	500ns max
Inverting, $R_f = R_i = 2k\Omega$	500ns max
SETTLING TIME, UNITY GAIN, 0.1%	
Inverting, $Z_f = 1k\Omega \| 3.3pF$	300ns max
Inverting, $Z_f = 1k\Omega \| 3.3pF$	250ns
Noninverting, $Z_f = 1k\Omega \| 3.3pF$	250ns
INPUT OFFSET VOLTAGE	
Initial @ +25°C	Adjust to Zero
Trim Potentiometer	1k ohm
With 499 ohm Fixed Trim Resistor	±2mV
vs. Temp (0 to +70°C)	±50μV/°C max (±15μV/°C max)
vs. Time	250μV/month
vs. Supply	±15μV/%
INPUT BIAS CURRENT	
Initial @ +25°C	-50pA max (-25pA max)
At +85°C	2nA (1nA)
INPUT IMPEDANCE	
Differential	$10^{11}\Omega \| 3.5pF$
Common Mode	$10^{11}\Omega \| 3.5pF$
INPUT NOISE	
Voltage, 0.01 to 1Hz	2μV p-p
5Hz to 50kHz	3μV rms
Current, 0.01 to 1Hz	0.1pA p-p
INPUT VOLTAGE RANGE	
Differential	±15V
Common Mode, 1% Error	±11V
COMMON MODE REJECTION	
±10V dc	15,000 min
±10V dc	30,000
POWER SUPPLY[2]	
Voltage, Rated Specifications	±15V
Operating	±(12 to 18)V
Current, Quiescent	9mA
TEMPERATURE RANGE	
Rated Performance	0 to +70°C
Operating	-25°C to +85°C
Storage	-55°C to +125°C
MECHANICAL	
Weight	15 grams
Trimpot	1kΩ
Mating Socket	AC1010

[1] Short circuit protected to ground.
[2] Recommend ADI model 904, ±15V @ 50mA.
Specifications subject to change without notice.

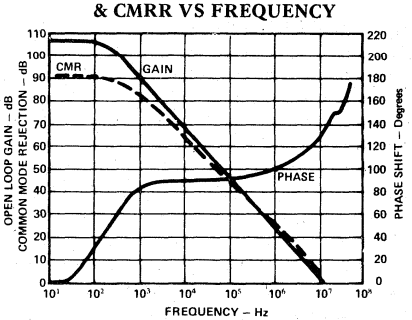
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



Mating Socket AC1010

OPEN LOOP GAIN, PHASE & CMRR VS FREQUENCY



KEY SPECS FOR ADI FAST SETTLING FET OP AMPS

Model	48J	46J	44J	45J	
Settling to 0.01% (max)	500	300	1000	1000	ns
Slew Rate	125	1000	75	75	V/μs
Bandwidth	15	40	10	10	MHz
Output @ 10V	20	100	20	20	mA
Drift	50	75	50	50	μV/°C
CMR min @ 10V	83	72	80	74	dB
Gain (min)	100k	25k	100k	50k	

CONSIDERATIONS FOR HIGH SPEED APPLICATIONS

Components: Use gain resistors of 2kΩ or less to reduce effects of stray capacitance. Use metal film resistors for low capacitance and inductance.

Wiring: Run separate signal and power grounds terminating at a common point at the power supply common (preferably). Keep all leads as short as possible to reduce noise pickup and inductive effects.

Fast Settling, Wideband, 100mA Output, FET Amplifiers

MODELS 50 & 51

FEATURES

Fast Settling: 200ns max, 0.05% (50J/K)
100ns max, 0.1% (50J/K)
100mA Output: dc to 8MHz (50J/K)
dc to 6MHz (51A/B)
All Hermetically Sealed Semiconductors (51A/B)
-55°C to +125°C Temperature Range (51A/B)
100MHz Gain Bandwidth (50J/K)

APPLICATIONS

A to D Input Amplifier
D to A Current Converter
Video Pulse Amplifier
CRT Deflection Amplifier
Wideband Current Booster



GENERAL DESCRIPTION

Models 50 and 51 are ultra fast, wideband differential FET amplifiers, designed for applications requiring fast settling time with high output current in closed loop gain configurations of 2 or greater. Model 50 offers guaranteed settling time of 100ns maximum to ±0.1% accuracy and 200ns maximum to ±0.05% accuracy. Model 51 features all hermetically sealed semiconductors for greater reliability and wide operating temperature range (-55°C to +125°C) with guaranteed settling times of 140ns maximum to ±0.1% and 250ns maximum to ±0.05%.

Model 50 is available in two input voltage drift selections. Model 50J is ±50μV/°C max, model 50K is ±15μV/°C max. Other outstanding features of models 50J/K are 100MHz gain bandwidth product, slew rate of 500V/μs and output current of ±100mA from dc to 8MHz.

Model 51 is also available in two input voltage drift selections; model 51A is ±50μV/°C max, model 51B is ±20μV/°C max. Models 51A/B offer 80MHz gain bandwidth product, slew rate of 400V/μs and ±100mA output current from dc to 6MHz. Both models 50 and 51 offer significant improvement over previous designs with lower input voltage noise (6μV rms, 5Hz to 2MHz bandwidth), particularly important in display system D/A converter applications.

FAST SETTLING APPLICATIONS

D/A converters require fast settling output amplifiers since conversion speed is often dictated by the settling time of the amplifier. Models 50 and 51 offer fast settling time performance at closed loop gains from 2 to 6. This characteristic is extremely important for D/A applications requiring fast current to voltage conversion from less than ideal current sources.

The circuit shown in Figure 1 is that of a typical current to voltage converter. The output of the D/A converter is often considered an ideal current source ($R_{out} = \infty$) which is converted to a voltage by the amplifier's feedback resistor. Although it may appear that in this application the amplifier is being operated in a closed loop gain of 1, a closer look at the D/A's specifications may show an output impedance of 800 to 2500 ohms. For this condition, the amplifier is operated in a closed loop gain of 2 to 6. This is then the range of gains over which settling time is important.

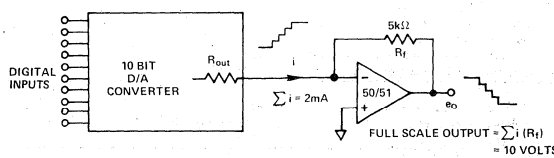


Figure 1. High Speed Current to Voltage Buffer

High speed amplifiers typically suffer significant degradation in settling time when operated in closed loop gains greater than unity. Model 50, with 100MHz gain bandwidth and model 51 with 80MHz gain bandwidth achieve fast settling time since they are far from the point of bandwidth limitations. For example, at a gain of 4, model 50 has a bandwidth of 20MHz, which represents a time constant of 8ns. For 0.1% settling, the bandwidth limitation is 6.9 time constants or approximately 55ns.

For detailed information, contact factory.

SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

MODEL	50J	50K	51A	51B
OPEN LOOP GAIN				
DC, Load = 100 ohm	88dB min	*	94dB min	**
DC, Load = 2k ohm	94dB min	*	97dB min	**
RATED OUTPUT[1]				
Voltage, $R_L \geq 100\Omega$	±10V min	*	*	*
Current	±100mA min	*	*	*
Impedance, Open Loop dc	200Ω	*	*	*
Load Capacitance, max				
Inverting	100pF max	*	*	*
Noninverting	50pF max	*	*	*
FREQUENCY RESPONSE				
Small Signal, Unity Gain	70MHz	*	56MHz	**
Small Signal, -3dB, Unity Gain	100MHz	*	80MHz	**
Full Power	8MHz min	*	6MHz min	**
Slew Rate, Noninverting	400V/μs, min	*	300V/μs, min	**
Slew Rate, Inverting	500V/μs, min	*	400V/μs, min	**
Overload Recovery	200ns	*	*	*
SETTLING TIME				
Inverting, Gain = 2				
±0.1%, ±10 Volt Step	100ns max	*	140ns max	**
±0.05%, ±10 Volt Step	200ns max	*	250ns max	**
Noninverting, Gain = 2				
±0.1%, ±10 Volt Step	150ns max	*	200ns max	**
±0.05%, ±10 Volt Step	300ns max	*	400ns max	**
INPUT OFFSET VOLTAGE				
Initial, @ +25°C	Adjust to Zero	*	*	*
Trim Potentiometer	1kΩ	*	*	*
With 499Ω Fixed Resistor	±3mV	*	*	*
vs. Temperature	±50μV/°C max	±15μV/°C max	±50μV/°C max	±20μV/°C max
vs. Supply Voltage	±15μV/%	*	*	*
vs. Time	±500μV/month	*	*	*
Warm up Drift, 20 Minutes	±2mV	*	*	*
INPUT BIAS CURRENT				
Initial, @ +25°C	0, 0-2nA max	*	*	*
vs. Temperature	Double/+10°C	*	*	*
vs. Supply Voltage	10pA/%	*	*	*
INPUT DIFFERENCE CURRENT				
Initial, @ +25°C	±100pA	*	*	*
vs. Temperature	Double/+10°C	*	*	*
INPUT IMPEDANCE				
Differential	$10^{10}\Omega \| 3.5pF$	*	*	*
Common Mode	$10^{10}\Omega \| 3.5pF$	*	*	*
INPUT NOISE				
Voltage, 0.1Hz to 10Hz	5μV, p-p	*	*	*
5Hz to 2MHz	6μV, rms	*	*	*
Current, 0.1Hz to 10Hz	1pA, p-p	*	*	*
INPUT VOLTAGE RANGE				
Common Mode Voltage	±10V min	*	*	*
Max Safe Differential Voltage	$\pm V_S$	*	*	*
Common Mode Rejection, CMV = ±10V	60dB, min	*	*	*
Common Mode Rejection, CMV = ±5V	70dB, min	*	*	*
POWER SUPPLY				
Voltage, Rated Performance[2]	±15V dc	*	*	*
Voltage, Operating	±(12 to 18)V dc	*	*	*
Current, Quiescent	±40mA	*	*	*
TEMPERATURE RANGE				
Rated Specifications	0 to +70°C	*	-25°C to +85°C	**
Operating[3]	-25°C to +85°C	*	-55°C to +125°C	**
Storage	-55°C to +125°C	*	*	*
MECHANICAL				
Case Size, mm	1.8" x 1.2" x 0.6"	*	*	*
Weight, grams	31	*	*	*
Mating Socket	AC1034	*	*	*

*Specifications same as Model 50J.

**Specifications same as Model 51A.

[1] Short circuit protected to ground.

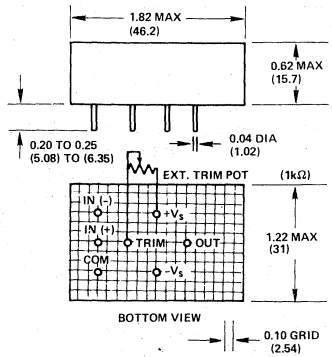
[2] Recommended power supply ADI Model 920, ±15V @ 200mA.

[3] Model 51A and 51B have an operating temperature range of -55°C to +100°C when operating in the differential mode.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



MATING SOCKET AC1034

UNITY GAIN APPLICATIONS

Models 50 and 51 have been optimized for fast settling inverting applications, such as current to voltage conversion at the output of D/A converters. In these configurations the high speed amplifier is usually operating in a noise gain of about 5. (Noise Gain = 1 + R_f/R_{out} of D/A). They have also been designed as fast non-inverting amplifiers and offer excellent performance at noise gains of 2 or higher. For unity gain applications the circuits shown in Figure 2 and Figure 3 are recommended.

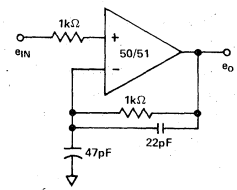


Figure 2. Recommended Circuit for Unity Gain Noninverting Buffer

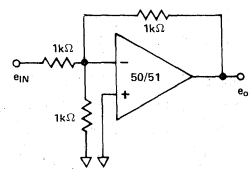


Figure 3. Recommended Circuit for Unity Gain Inverter

ANALOG DEVICES

Low Noise, Low Drift Precision FET Amplifier

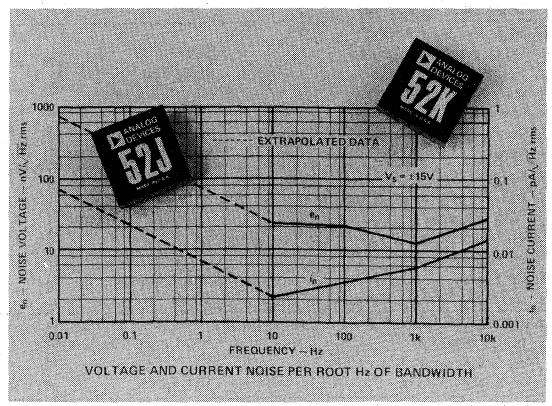
MODEL 52

FEATURES

Guaranteed Low Noise 1.5μV p-p max (0.01 to 1Hz)
Low Voltage Drift: 1μV/°C max (52K)
Low Bias Current: 3pA, max
High CMR: 100dB, min
High Voltage Gain: 120dB, min
Wide Power Supply Range: ±9V to ±18V
Excellent Long Term Stability: 5μV/month
Fast Thermal Response

APPLICATIONS

Low Level Instrumentation Preamp
High Impedance Precision Buffer
Long Term Integrator
Current to Voltage Converter
Precision Voltage Regulator
Preamp for 16-Bit Resolution V/F Converters



VOLTAGE AND CURRENT NOISE PER ROOT Hz OF BANDWIDTH

GENERAL DESCRIPTION

Model 52, a low noise, high accuracy FET input operational amplifier was designed for handling microvolt signals from high impedance (>100kΩ) sources. It features guaranteed low voltage noise (1.5μV p-p max, 0.01 to 1Hz bandwidth) with low input offset voltage drift (3μV/°C max, 52J; 1μV/°C max 52K). Unlike most available low drift amplifiers, model 52 voltage drift is unaffected by trimming the initial offset voltage (0.5mV max). The low input bias current (3pA max) is held constant over the entire ±10V common mode voltage range. High voltage gain (120dB, min) and high CMR (100dB, min) complete the performance profile. Model 52 is an excellent choice for high accuracy, high resolution linear signal processing applications.

By incorporating a new low noise N-channel monolithic FET input stage, thermal stability, voltage noise and differential signal performance are improved to a level previously obtainable only in the best bipolar amplifier designs. Model 52 is an excellent choice to replace chopper stabilized amplifiers where significant sources of error are introduced from zero beating, "chopper spikes" and ground loop currents.

The guaranteed accuracy performance of model 52 suggests critical applications such as low noise, low drift "front-end" preamplifiers for A to D converters and DVM's. For high impedance buffering applications, model 52 offers low input bias current, high linear common mode rejection, complete protection from input transients (offset voltage and bias current will not degrade due to reverse breakdown) and freedom from latch up when the common mode voltage range is exceeded. Model 52 is supplied in a reliable, compact epoxy module package. Output is protected from shorts to ground and/or supply voltage and is capable of driving up to 0.01μF load capacitance.

IMPROVED OFFSET VOLTAGE STABILITY

Model 52 has been designed for the lowest possible input voltage drift over the 0 to +70°C temperature range. In most operational amplifier designs, trimming is accomplished by unbalancing the current in the input stage. This trimming technique introduces an additional 2 to 12μV/°C for each millivolt of E_{OS} that is nulled. To provide performance consistent with low offset voltage drift, model 52 incorporates a three-point trim (see connection diagram) whereby a compensating voltage is introduced without unbalancing the input stage currents. By virtue of this trim scheme, there is no degradation in T.C. when E_{OS} is nulled and the specified performance is achieved.

IMPROVED NOISE PERFORMANCE

Input noise limits signal resolution in low level signal processing applications. The FET input stage of model 52 reduces noise current significantly from that of bipolar amplifiers, permitting high source impedance applications. Model 52 also offers voltage noise levels appreciably below that of other FET amplifiers. To illustrate the excellent low noise performance of model 52, Figure 1 shows typical input voltage noise in a 0.01 to 1Hz bandwidth. Noise is typically less than 1μV p-p and is free of noise spikes.

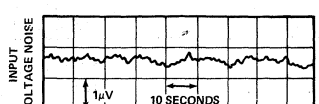


Figure 1. Voltage Noise 0.01 to 1Hz Bandwidth

For detailed information, contact factory.

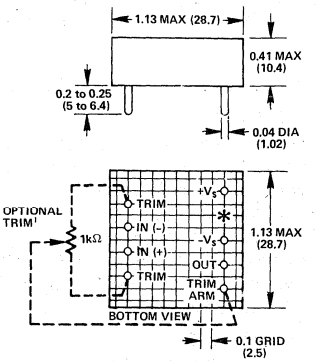
SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

MODEL	52J	52K
OPEN LOOP GAIN		
DC 2kΩ Load	120dB min (130dB typ)	*
RATED OUTPUT[1]		
Voltage, 2kΩ Load	±10V min	*
Current	±5mA min	*
Maximum Load Capacitance	0.01μF	*
Impedance, Open Loop	75Ω	*
FREQUENCY RESPONSE		
Unity Gain, Small Signal	500kHz	*
Full Power	4kHz min	*
Slew Rate	0.25V/μs min	*
Overload Recovery	130μs	*
Settling Time, ±0.1%, ±10V Step	100μs	*
Settling Time, ±0.01%, ±10V Step	150μs	*
INPUT OFFSET VOLTAGE		
Initial[2], @ +25°C	±500μV max	*
With External Trim Potentiometer	Adjustable to Zero	*
vs. Temperature (0 to +70°C)	±3μV/°C max	±1μV/°C max
vs. Supply Voltage	±2μV/%	*
vs. Time	±5μV/Month	*
Warm-Up Drift, 5 Minutes	±5μV	*
INPUT BIAS CURRENT		
Initial, @ +25°C	-3pA max (-1pA typ)	*
vs. Temperature (0 to +70°C)	x2/+10°C	*
vs. Supply Voltage	±0.01pA/%	*
INPUT DIFFERENCE CURRENT		
Initial, @ +25°C	±1pA	*
vs. Temperature (0 to +70°C)	x2/+10°C	*
INPUT IMPEDANCE		
Differential	10^{12}Ω||3.5pF	*
Common Mode	10^{12}Ω||3.5pF	*
INPUT NOISE		
Voltage, 0.01Hz to 1Hz	1.5μV p-p max (1μV p-p typ)	*
10Hz to 10kHz	3μV rms max (2μV rms typ)	*
f = 1Hz	70nV/√Hz rms	*
f = 10Hz	25nV/√Hz rms	*
f = 100Hz	20nV/√Hz rms	*
f = 1kHz	13nV/√Hz rms	*
Current, 0.01Hz to 1Hz	0.1pA p-p	*
f = 1Hz	7fA/√Hz rms	*
f = 10Hz	2.5fA/√Hz rms	*
f = 100Hz	3.5fA/√Hz rms	*
f = 1kHz	6fA/√Hz rms	*
INPUT VOLTAGE RANGE		
Common Mode Voltage	±10V min	*
Common Mode Rejection, CMV = ±10V	100dB min (106dB typ)	*
Max Safe Differential Voltage	$\pm V_S$	*
POWER SUPPLY[3]		
Voltage, Rated Performance	±15V	*
Voltage, Operating	±(9 to 18)V	*
Current, Quiescent	±5mA	*
TEMPERATURE RANGE		
Rated Performance	0 to +70°C	*
Operating	-25°C to +85°C	*
Storage	-55°C to +125°C	*
MECHANICAL		
Case Size	1.12" x 1.12" x 0.4"	*
Weight	16g	*
Mating Socket	AC1008	*

*Specifications same as model 52J.
[1] Protected for short circuit to ground.
[2] With no external trim potentiometer connected.
[3] Recommended power supply, ADI model 904, ±15V @ 50mA output.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

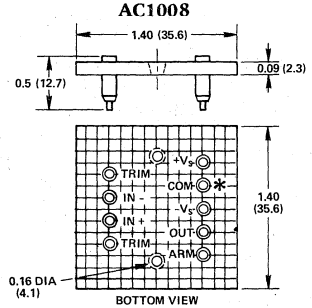
Dimensions shown in inches and (mm).



[1] Optional 1kΩ external trim pot. Input offset voltage may be adjusted to zero with trim pot connected as shown. With trim pins left open, input offset voltage will be ±0.5mV, maximum.

*Common Supply connection not required.

MATING SOCKET AC1008



*No connection required on Model 52.

FREQUENCY RESPONSE

From the plot of Open Loop Voltage Gain and Phase Shift (see Figure 2) versus Frequency, it can be seen that model 52 is stable for all closed loop gains. Even at the crossover frequency of 500kHz, model 52 has a phase margin of 75°.

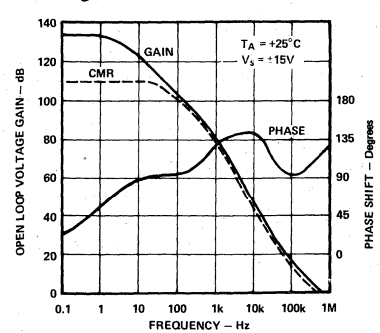


Figure 2. Open Loop Frequency Response and CMR

ANALOG DEVICES

High Voltage Differential FET Amplifier

MODEL 171

FEATURES
High Output Voltage: ±140V
High CMR: 100dB min
Operates With a Wide Range of Power Supplies
High CMV: ±(|V_S| - 10V)

APPLICATIONS
High Voltage Compliance Current Source
High Voltage Follower With Gain
High Voltage Integrator
Diff. Amp for High CMV Bridge Applications
Reference Power Supply



GENERAL DESCRIPTION

Model 171 is a high performance FET input op amp designed for operation over a wide range of supply voltages. This module features an output range of ±15V to ±140V at 10mA, a minimum CMRR of 100dB and a high common mode voltage rating of ±(V_S - 10V) min. DC offset is less than ±1mV, and maximum drift of either ±50 or ±15μV/°C is available in the J or K versions. Bias current is less than 50pA (171J) or 20pA (171K), doubling per +10°C increase of temperature. The model 171 also features small signal bandwidth of 3MHz for unity gain, full-power bandwidth of 15kHz, and slew rate of 10V/μs. These operating characteristics make model 171 an excellent choice for high voltage buffer applications, followers with gain, off-ground signal measurements and reference power supplies.

Excellent power supply rejection of 7μV/V enables model 171 to be powered by inexpensive, low regulation supplies, without sacrificing any of the 171's inherent high performance. The supplies also need not be symmetrical. Any combination of power supply voltages between the limits of 15 to +300V for the positive side and 15 to -300V for negative side is acceptable provided the total voltage across the amplifier is within the range of 30 to 300V.

Model 171's output is completely short circuit protected by the use of a current limit scheme. This type of protection provides a short circuit output that is only slightly greater than the rated output current for normal operation. With this design the module and external circuitry are protected, internal heat dissipation and the associated high temperature rise are limited, and added reliability is built in.

POWER SUPPLY VOLTAGES

Model 171 offers the flexibility of operating with an extensive range and combination of power supply voltages. Figure 1 shows a chart of permissible combinations of supply voltages for the 171. The model 171 maintains its normal operating characteristics when using asymmetrical power supply configurations.

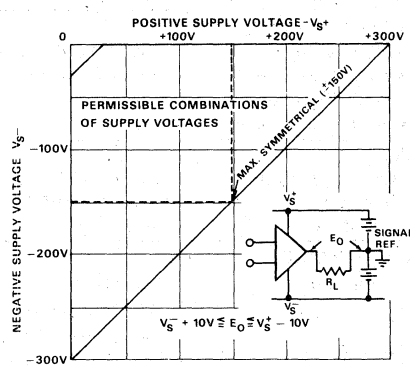


Figure 1. Power Supply Voltage Combinations

For detailed information, contact factory.

SPECIFICATIONS (typical @ +25°C and ±125V unless otherwise noted)

MODEL	171J	171K
OPEN LOOP GAIN	10^6 min	*
RATED OUTPUT		
Voltage	$\pm(\|V_S\|-10V)$ min	*
Current	±10mA min	*
Maximum Load Capacitance	1000pF	*
FREQUENCY RESPONSE		
Unity Gain, Small Signal	3MHz	*
Slewing Rate	10V/μs min	*
Full Power	15kHz min	*
Settling Time to ±0.1%, ±10V Step	25μs	*
Overload Recovery	5μs	*
INPUT OFFSET VOLTAGE		
Initial Offset, +25°C[1]	±1mV	*
Avg. vs. Temp (0 to +70°C)	±50μV/°C max	±15μV/°C max
vs. Supply Voltage	±7μV/V	*
vs. Time	±250μV/mo	*
INPUT BIAS CURRENT		
Initial Bias, +25°C	-50pA max	-20pA max
vs. Temp (0 to +70°C)	x 2/10°C	*
Difference Current	±10pA	±5pA
INPUT IMPEDANCE		
Differential	$10^{11}\,\Omega\|\|3.5$pF	*
Common Mode	$10^{11}\,\Omega\|\|3.5$pF	*
INPUT NOISE		
Voltage, 0.01 to 1.0Hz	4μV p-p	*
10Hz to 10kHz	2.5μV rms	*
5Hz to 50kHz	6μV rms	*
INPUT VOLTAGE RANGE		
Common Mode Voltage	$\pm(\|V_S\|-10V)$ min	*
Common Mode Rejection	100dB min	*
Common Mode Rejection	114dB	*
Max Safe Differential Voltage	$\pm V_S$	*
POWER SUPPLY		
Voltage, Rated Specification	±25 to ±150V dc	*
Voltage, Operating	±15 to ±150V dc	*
Current, Quiescent	±6mA typ	*
TEMPERATURE RANGE		
Rated Specification	0 to +70°C	*
Operating	-25°C to +85°C	*
Storage	-40°C to +100°C	*
MECHANICAL		
Case Size	2.41" x 1.82" x 0.61"	*
Weight	80g	*
Mating Socket	AC1037	*

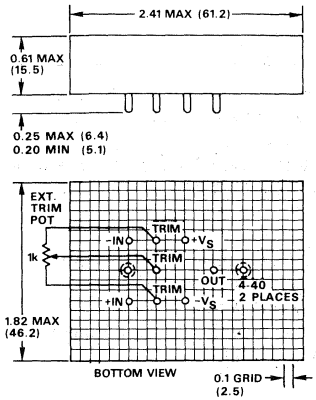
*Specifications same as 171J

[1] No external trim connection required.

Specifications subject to change without notice.

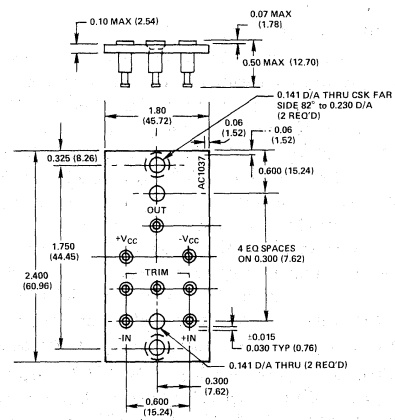
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



MATING SOCKET

Dimensions shown in inches and (mm).



MATING SOCKET AC1037

SINGLE SUPPLY OPERATION

As shown in Figure 1, the model 171 requires at least ±15 volts applied across it in order to operate properly. The 171 may be operated from a single floating supply voltage by using the power supply offsetting scheme shown in Figure 2. When this configuration is used, the 171 is capable of operating over its specified input and output voltage range.

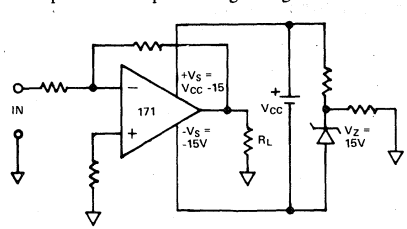


Figure 2. Single Supply Operation

ANALOG DEVICES

Low Noise Chopper Stabilized Amplifiers

MODELS 234, 235

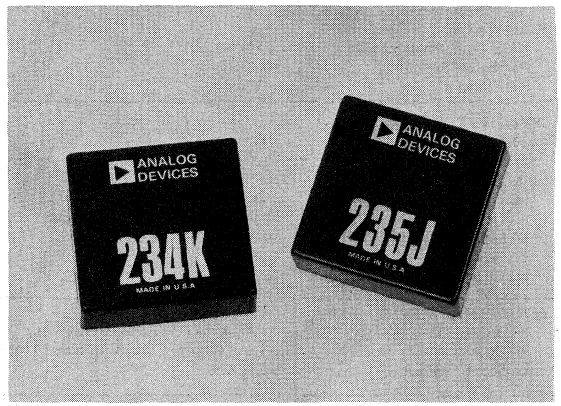
4

FEATURES

Ultra-Low Noise: 0.7μV p-p, 0.01Hz to 1Hz BW (234)
0.5μV p-p, 0.01Hz to 1Hz BW (235)
Very Low Offset Drift: 0.1μV/°C, 1pA/°C (234L)
0.1μV/°C, 0.5pA/°C (235L)
Excellent Long Term Stability: 5μV/year (235)
Fast Settling: 4μs to 0.01%, 2.5MHz BW (235)

APPLICATIONS

Precision Integration
Servo/Null Detector Loops
Microvolt/Picoamp Measurements
Bridge Amplifier
Controlled Current Source
Balance Scales and Weighing Instruments



GENERAL DESCRIPTION

Analog Devices' models 234, 235 are high performance, economy chopper-stabilized op amps that meet the demands of critical laboratory and industrial applications requiring ultra-low noise, exceptional long term offset stability and versatility. Both models feature compact plug-in modular design, and are ideally suited for new design applications, or upgrading of existing systems, where both improved performance and cost savings can be realized.

Model 234: The model 234 is designed for wideband applications and features 10^7 V/V open loop gain, 2.5MHz unity gain bandwidth, full power response to 500kHz and settling time of 4μs (to 0.01%, 10V step, 20kΩ load). The model 234 also features low input voltage noise of 0.7μV p-p (0.01Hz to 1Hz BW), low offset voltage drift of 1μV/°C (234J), 0.03μV/°C (234K) or 0.1μV/°C (234L) and long term stability of ±2μV/month.

Incorporating MOSFET choppers and discrete components (vs. IC op amps) for the main and stabilizing amplifier channels, this inverting design is virtually free of input chopper spikes and offers reduced modulation ripple for quieter wideband performance. These characteristics are especially desirable when operating from high source impedances (above 100kΩ) at wide bandwidths. To illustrate the improvements in noise and bandwidth performance, over previous Analog Devices' designs, comparative data is set forth in the following sections comparing models 232 and 233 with 234.

Model 235: The model 235 is recommended for applications where lowest cost and lowest noise are required. The model 235 features low input voltage noise of 0.5μV p-p (0.01Hz to 1Hz BW), low offset voltage drift of 0.5μV/°C (235J), 0.25μV/°C (235K), 0.1μV/°C (235L) and a long term stability of 5μV/year.

This combination of noise and drift performance makes model 235 ideally suited for demanding applications such as balance scales and weighing instruments requiring high accuracy and excellent long-term stability without the use of "front panel" balance pots or periodic internal adjustment.

Model 235 has been designed to virtually eliminate intermodulation problems caused by "beating" against power line frequencies. The chopper's ultra-stable oscillator is precisely set at the factory to a frequency that minimizes ineractions with harmonics of 50Hz, 60Hz and 400Hz power lines.

APPLICATIONS

In general, the models 234, 235 inverting amplifiers should be considered where long term stability of offset voltage must be maintained with time and temperature for precision designs, or wherever maintenance-free operation of instruments and remote circuits is essential. Typical applications include low drift amplification of microvolt signals, integration of low duty-cycle pulse trains and analog computing for general purpose designs. Low input noise and stable offset voltages also make 234, 235 an ideal preamp for precision low frequency applications such as DVMs, 12- to 16-bit A to D converters, and for error amplifiers in servo and null detector systems.

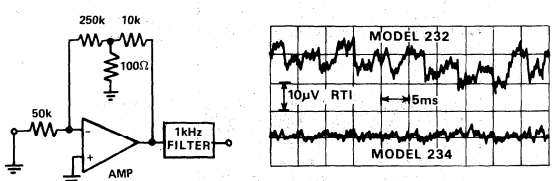


Figure 1. Model 234 Comparative Input Noise (RTI) Performance in a dc to 1kHz Bandwidth

For detailed information, contact factory.

SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

MODEL	234J	234K	234L	235J	235K	235L
OPEN LOOP GAIN						
DC, 2k ohm load	10^7 V/V min	*	*	5 x 10^7 V/V min	**	**
RATED OUTPUT						
Voltage	±10V min	*	*	*	*	*
Current	±5mA min	*	*	*	*	*
Load Capacitance Range	0–1000pF min	*	*	0.01µF	**	**
FREQUENCY[1]						
Unity Gain, Small Signal	2.5MHz	*	*	1MHz	**	**
Full Power Response	500kHz min	*	*	5kHz min	**	**
Slew Rate	30V/µs	*	*	0.3V/µs min	**	**
SETTLING TIME to 0.01%						
20kΩ load, 10V step	4µs	*	*	N/A	N/A	N/A
INPUT OFFSET VOLTAGE						
Initial Offset[2]	±50µV max	±20µV max	±20µV max	±25µV max	**	±15µV max
vs. Temp, 0 to +70°C	±1.0µV/°C max	±0.3µV/°C max	±0.1µV/°C max	±0.5µV/°C max	±0.25µV/°C max	±0.1µV/°C max
vs. Supply Voltage	±0.2µV/%	*	*	±0.1µV/%	**	**
vs. Time	±2µV/month	*	*	±5µV/year	**	**
vs. Turn On, 10 sec to 10 min	±3µV	*	*	*	*	*
INPUT BIAS CURRENT						
Initial, @ +25°C	±100pA max	*	*	*	±50pA max	±50pA max
vs. Temp, 0 to +70°C	±4pA/°C max	±2pA/°C max	±1pA/°C max	1pA/°C max	0.5pA/°C max	0.5pA/°C max
vs. Supply Voltage	±0.5pA/%	*	*	0.2pA/%	**	**
INPUT IMPEDANCE						
Inverting Input to Signal Ground	300k ohms	*	*	*	*	*
INPUT NOISE						
Voltage, 0.01 to 1Hz	0.7µV p-p	*	*	0.5µV p-p	2µV p-p max	2µV p-p max
0.1 to 10Hz	1.5µV p-p	*	*	3.5µV p-p	**	**
10Hz to 10kHz	2µV rms	*	*	5µV rms	**	**
Current, 0.01 to 1Hz	2pA p-p	*	*	10pA p-p	**	**
0.1 to 10Hz	4pA p-p	*	*	30pA p-p	**	**
INPUT VOLTAGE RANGE						
(-) Input to Signal Ground	±15V max	*	*	*	*	*
POWER SUPPLY (V dc)[3]						
Rated Performance	±15V @ 5mA	*	*	*	*	*
Operating	±(12 to 18)V	*	*	*	*	*
TEMPERATURE RANGE						
Rated Specifications	0 to +70°C	*	*	*	*	*
Operating	-25°C to +85°C	*	*	*	*	*
Storage	-25°C to +100°C	*	*	-55°C to +125°C	**	**

NOTES
*Specifications same as model 234J.
**Specifications same as model 235J.
[1] Model 235 overload recovery, 10 sec typ.
[2] Externally adjustable to zero.
[3] Recommended power supply: Analog Devices model 904, ±15V dc @ 50mA.

Specifications subject to change without notice.

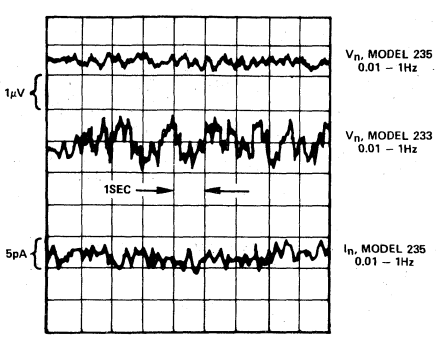
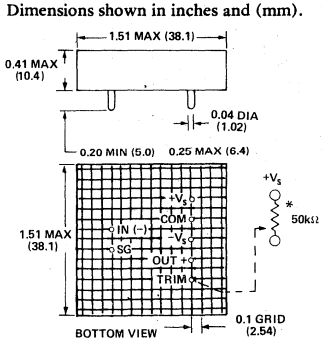


Figure 2. Model 235 Voltage and Current Noise, Model 233 Voltage Noise Shown for Comparison.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTES:
*Connect Trim Terminal to Common if Trim Pot is not used.
1. SG Tied to Common.
2. Mating Socket AC1010.
3. Weight: 27 grams.

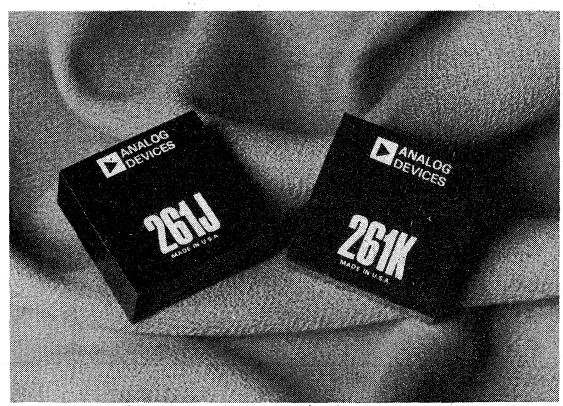
ANALOG DEVICES

Low Noise Non-Inverting Chopper Amplifier

MODEL 261

FEATURES
- Non-Inverting Input
- $10^9\Omega$ Common Mode Impedance
- Protected MOSFET Chopper
- Ultra Low Drift 0.1μV/°C, Max (261K)
- Guaranteed Low Noise of 0.4μVp-p (0.01 to 1Hz)
- Low Cost

APPLICATIONS
- Microvolt & Millivolt Measurements
- Meter & Recorder Preamplifier
- Semiconductor Strain Gage Amplifier
- Biological Sensors
- Potentiometer Buffer



GENERAL DESCRIPTION

Model 261 is a low cost non-inverting chopper amplifier featuring ultra low drift of 0.1μV/°C, open loop gain of greater than 10 million V/V and guaranteed low noise performance of 0.4μV p-p max in a 0.01 to 1Hz bandwidth. It is ideally suited for low level pre-amplifier applications where high input impedance and low noise are essential.

Model 261 also offers a solution to beat frequency problems caused by a low frequency carrier mixing with harmonics of the ac line. Its carrier frequency of 3500Hz is nearly a decade higher than that of models previously available. The required harmonic of the ac line that could cause interference with a 3500Hz carrier has negligible energy content and beat frequencies are eliminated. As a further protection against interfering signals, model 261 has been completely shielded internally. This protective shield reduces interference due to RF signals, as well as carrier signals from adjacent chopper amplifiers.

Still another advantage of the 261 due to its higher chopper frequency and shielded design is an output signal that is free from both distortion and chopper spikes. The result is a design that can process low level signals while maintaining low distortion and high signal to noise ratios.

CHOPPER VS. CHOPPER-STABILIZED

Most conventional ultra-stable amplifiers are chopper-stabilized to achieve low drift. In these units, the higher frequency signal components are separated and directly amplified, while the low frequency and dc components are separately chopped, amplified, demodulated, and then summed with the high frequency components in an output stage. This method provides wide bandwidth and excellent performance at the expense of increased cost and complexity. Since many requirements for ultra-low drift amplification involve only dc and low frequency signals, the additional high frequency amplifier stage found in most chopper-stabilized amplifiers has been eliminated from the model 261. This design approach has made it possible to achieve a practical non-inverting configuration, which retains the advantages of low cost and small size. The input stage of the model 261 chops the signal at a 3500Hz rate, resulting in a maximum useful -3dB bandwidth of about 100Hz. For increased flexibility in meeting specific design requirements, terminals are provided for an external compensation capacitor, which determines the amplifier's gain-bandwidth product.

INPUT IMPEDANCE

One of the prime advantages of the non-inverting amplifier is the capability of bootstrapping the input impedance up to the level of the common mode impedance. For the model 261, this means that the 40kΩ open loop input resistance will be multiplied by the open loop gain times the feedback factor. With a typical open loop gain of 40×10^6, closed loop gains of up to 1600 will allow the user to realize $10^9\Omega$ input resistance. Even at a gain of 10,000, the effective input resistance will be over 100 megohms. (i.e.) $(40k\Omega)\frac{40 \times 10^6}{10^4} = 160M\Omega$.

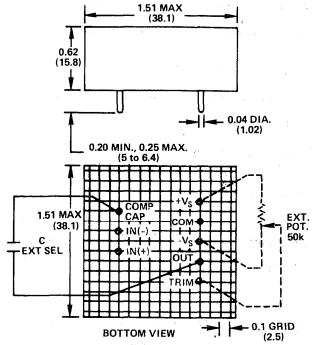
SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

Model	261J	261K
OPEN LOOP GAIN		
DC rated load	10^7 V/V min	*
RATED OUTPUT		
Voltage	±10V min	*
Current	±5mA min	*
Load Capacitance Range	0 to 0.001μF	*
FREQUENCY RESPONSE[1]		
Small Signal, -3dB	100Hz	*
Full Power Response	2-50Hz min	*
Slewing Rate	100V/s min	*
Overload Recovery	300ms	*
INPUT OFFSET VOLTAGE		
External Trim Pot[2]	50kΩ	*
Initial Offset, +25°C	±25μV max	*
Avg vs Temp (0 to +70°C)	±0.3μV/°C max	±0.1μV/°C max
Supply Voltage	±0.1μV/%	*
Time	±½μV/month	*
Warm-Up Drift	<3μV in 20 minutes	*
INPUT BIAS CURRENT		
Initial Bias, +25°C, + Input	±300pA max	*
Avg vs Temp (0 to +70°C)	±10pA/°C max	*
Initial Bias, +25°C, - Input	±10nA max	*
Avg vs Supply Voltage	±3pA/%	*
INPUT IMPEDANCE		
Differential	40kΩ||0.01μF	*
Common Mode	10^9 Ω||0.02μF	*
INPUT NOISE		
Voltage, 0.01 to 1Hz, p-p	0.4μV max	*
0.01 to 10Hz, p-p	1.0μV max	*
Current, 0.01 to 1Hz, p-p	8pA	*
0.01 to 10Hz, p-p	20pA	*
INPUT VOLTAGE RANGE		
Common Mode Voltage	±0.5V min	±1.0V min
Common Mode Rejection	300,000	*
Max Safe Differential Voltage	±20V	*
Max Safe Common Mode Voltage	±20V	*
POWER SUPPLY[3]		
Voltage, Rated Specification	±(14 to 16)V	*
Voltage, Operating	±(13 to 18)V	*
Current, Quiescent	±7mA	*
TEMPERATURE RANGE		
Rated Specifications	0 to +70°C	*
Operating	-25°C to +85°C	*
Storage	-55°C to +125°C	*
MECHANICAL		
Case Size	1.5" x 1.5" x 0.62"	*
Mating Socket	AC1022	*
Weight	1.75 oz. (50g)	*

[1] See applications information.
[2] Ground trim terminal if trim potentiometer is not used.
[3] Recommended power supply, ADI model 904, ±15V @ 50mA output.
*Specifications same as for model 261J.
Specifications subject to change without notice.

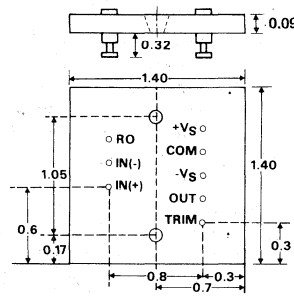
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



1. Trim terminal should be grounded if potentiometer is not used.
2. See Note 1 below for cap value. Use Polycarbonate, Mylar, Mica, Glass, or Polystyrene capacitor for best performance.

MATING SOCKET AC1022



Notes
1. R.O. is connection for compensation capacitor.
2. Bottom View Shown.
3. Mounting holes 0.141 Dia., countersunk 82° to 0.23" Dia.
4. All in line pins spaced 0.2".
5. Dimensions in inches.
6. Markings printed on socket.

OTHER ULTRA LOW DRIFT, LOW NOISE AMPLIFIER

Model 235: Chopper stabilized amplifier has noise of less than 1μV p-p and drift is only 0.1μV/°C (235L).

NON-INVERTING VS. INVERTING OPERATION

The major limitation of the standard inverting type chopper stabilized amplifier is due to the practical limit on input impedance resulting from input bias current characteristics. If one attempts to obtain 10^7 ohms input impedance by using a 10^7 ohm input resistor with an inverting amplifier, this resistor will convert input current drifts of 0.5pA/°C into equivalent voltage drifts of 5μV/°C. It will also add Johnson Noise of 2.5μV p-p/$\sqrt{Hz}$ to the amplifier's input. These results negate the advantage of selecting the chopper-stabilized amplifier in the first place. Noise current will similarly increase the input uncertainty: inverting amplifier input noise currents of 10pA become 100μV noise voltages (referred to input). Furthermore, uncompensated initial bias currents of 50pA cause additional offsets of 500μV. Due to the non-inverting configuration of the model 261, these limitations are avoided. The input bias current (with its drift and noise) flows only through the signal source impedance, effectively eliminating the multiplication of drift and noise and offset caused by the input resistor in the inverting configuration. These benefits of the model 261 are shown graphically in Figure 1. When required input impedance is more than 300,000 ohms, the model 261 gives increasingly superior performance. One additional advantage is that the gain-setting precision resistors can be low-cost low value resistors instead of the more costly high resistance values.

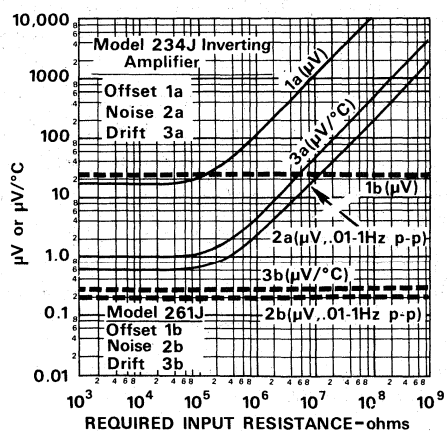


Figure 1. Offset, Drift, & Noise vs. Required Input Resistance

NON-INVERTING AMPLIFIER SELECTION CRITERIA

(Model 261 vs. chopperless amplifiers)

In selecting an amplifier for low drift, one of the major considerations is the effect of source resistance. For low values of source resistance, the total offset (or drift) for differential amplifiers is essentially equal to the amplifier's offset (or drift) voltage. At the value of source resistance equal to the ratio of offset voltage to difference current, or offset voltage drift to difference current drift, the respective current is contributing an error equal to its corresponding voltage error. For values of source resistance larger than this calculated value, the current error's contribution will be dominant. In this section, model 261's drift and offset are compared with two low drift chopperless differential amplifiers, one with FET input, the other with bipolar input.

Fixed Source Resistance. If source resistance is fixed, bipolar chopperless amplifiers not having internal bias current drift compensation can benefit by the use of a compensating resistor in series with the (-) input. Under these conditions, Figure 2 shows a comparison of total drift /°C vs. source resistance for the model 261K, the model 184L low drift bipolar amplifier, and the model 52K low drift FET amplifier. For source resistances up to 200,000 ohms, the model 261 gives the lowest temperature drift. Total drift (R.T.I.) is equal to:

$$\Delta E_{in}/\Delta T = \Delta E_{os}/\Delta T + R_S\,(\Delta I_{os}/\Delta T) \text{ (Models 184, 52)}$$

$$\Delta E_{in}/\Delta T = \Delta E_{os}/\Delta T + R_S\,(\Delta I_b/\Delta T) \text{ (Model 261)}$$

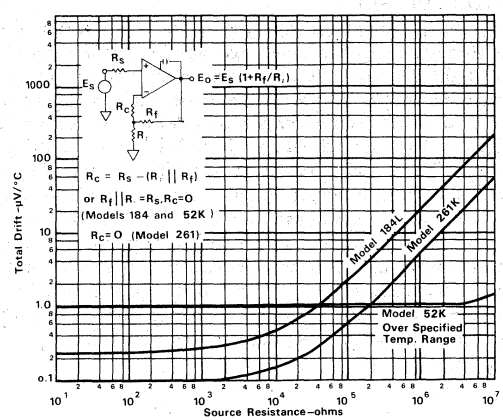


Figure 2. Offset Drift vs. Fixed Source Resistance

Variable Source Resistance. For situations where the source resistance can vary over a significant range, for instance when the amplifier's source is a multiturn potentiometer, a different set of conditions apply. The effective drift current to be considered for differential chopperless amplifiers is now the Input Bias Current/°C, rather than the Input Difference Current/°C (I_{os}/°C). A two to one improvement in drift for the model 184 can be obtained if the bias current balancing resistor (R_C in Figure 3) is made equal to the mean value of the source resistance. Under these conditions, drift will be approximately:

$$\Delta E_{in}/\Delta T = \Delta E_{os}/\Delta T + \tfrac{1}{2}\,(R_S \text{ max} - R_S \text{ min})\,(\Delta I_b/\Delta T) + R_C\,(\Delta I_{os}/\Delta T) \text{ (Models 184, 52K)}$$

$$\Delta E_{in}/\Delta T = \Delta E_{os}/\Delta T + (R_S \text{ max})\,(\Delta I_b/\Delta T) \text{ (Model 261)}$$

Figure 3 shows the total drift for a source resistance varying from zero to the chosen value, for models 52K, 184L and 261K. For values up to 200,000 ohms the model 261 again gives the lowest total temperature drift.

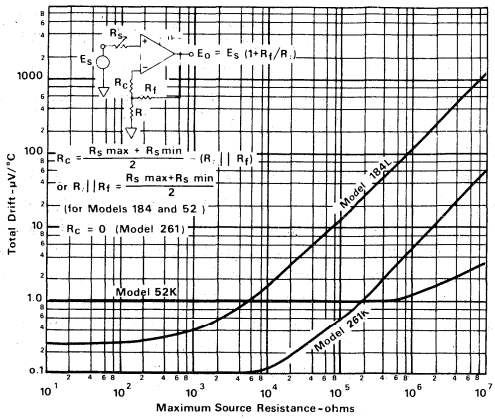


Figure 3. Offset Drift vs. Variable Source Resistance

INITIAL OFFSET

An initial offset voltage will develop due to bias current flowing through the source impedance. For fixed source impedances, this offset may be zeroed out in differential chopperless amplifiers not having internal bias current drift compensation by the use of the series compensating resistor, R_C shown in Figure 4. This offset should not be nulled out by adjusting the amplifier's offset trim because this will increase the offset voltage drift. With the model 261, however, all offsets may be zeroed out by means of the trim potentiometer. For variable source impedances, the offset should be zeroed out with the source impedance at its mean value. Figure 4 is a plot of the maximum offset which will occur with a given range of R_S variations, assuming the offsets are zeroed when operating with the mean value of R_S. Initial offset due to R_S is $I_b/2$ (R_S max - R_S min).

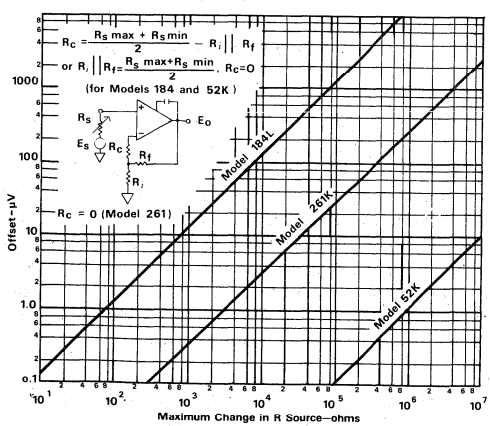


Figure 4. Offset vs. $\triangle R_S$

LONG TERM DRIFT

Offset voltage of any amplifier will show some change with time, due to normal component aging. It is important to realize that the published drift for amplifiers does not accumulate linearly with increasing time. For example, the voltage drift of the model 261 is specified as ±½µV/month (a calculated figure believed to be quite conservative). For calculation of random long term drift, a rule of thumb is that one should multiply drift by the square root of the time factor increase. For the model 261, this yields a conservative long term drift of less than 2µV per year.

NOISE

A major criterion in the selection of an amplifier for low level signals is the amplifier input noise, since this is usually the limiting factor on system resolution. This is particularly important whenever high source impedances are encountered, since current noise through the source impedance will appear as an additional voltage noise, combining with the basic amplifier voltage noise and Johnson noise of the resistor. The sum of these noise sources will then be amplified along with the desired signal. For this reason, special care has been taken to reduce noise voltage and current to a level far below that of comparable chopper amplifiers. The one Hertz bandwidth noise voltage and current are 0.4µV p-p max and 8pA p-p respectively. For 10Hz bandwidth, corresponding values are 1µV p-p max and 20pA p-p. Figure 5A is a graph of noise vs. bandwidth for both current and voltage. Figure 5B is a spectral density plot for determining spot noise at any frequency. Figure 6 is a plot of peak to peak noise which will be encountered for these bandwidths, as a function of source resistance.

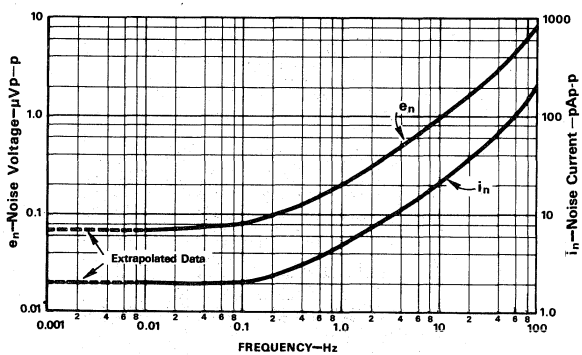


Figure 5A. Noise Current and Voltage vs. Bandwidth. Measured from 0.01Hz.

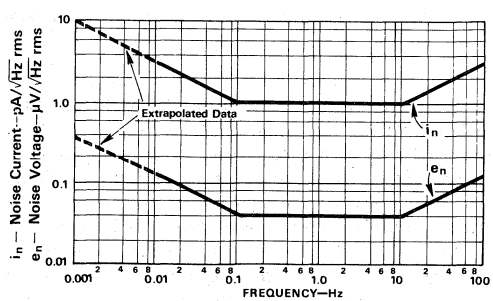


Figure 5B. Spectral Density of Current and Voltage

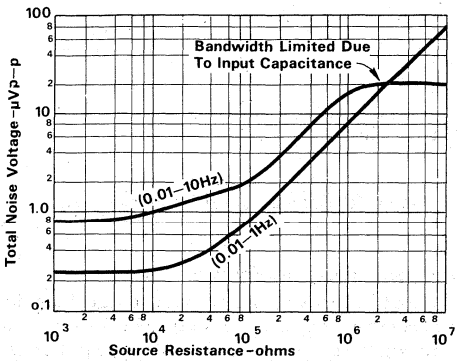


Figure 6. Total Noise vs. Source Resistance

HOW THE MODEL 261 OPERATES

As shown in Figure 7, the model 261 consists of five specific circuit functions. The input signal is fed through a resistor to the MOSFET Chopper. When the MOSFET is off (high resistance), the error signal appears at the input to the ac-coupled amplifier. When the MOSFET transistor is on (low resistance), the input to this amplifier is reduced to near zero. The difference between the on and off voltages at the amplifier is a square wave of amplitude slightly less than the error voltage. The attenuating effect of the MOSFET Chopper's "on" resistance is negligible. For example, if the attenuation were as much as 10%, the only effect would be to lower the potential open loop gain of the amplifier by the same amount.

The ac-coupled amplifier, consisting primarily of a linear integrated circuit, amplifies the resulting chopper error signal. Its output is capacitively coupled into a synchronous demodulator which reconstructs the low frequency-dc input signal, preserving polarity information. The drift of the input stage is not present in the demodulated signal since it was not chopped by the input network. The demodulated signal is filtered and further amplified by the integrator connected output dc amplifier.

Using the system just described, the remaining drift and offset, referred to the amplifier input, is equal to the output dc amplifier stage input drift and offset divided by the ac-coupled amplifier's gain. If the output stage integrated circuit amplified had a 100μV/°C drift, and the ac-coupled amplifier gain is 1000, then the drift, referred to the input will be 0.1μV/°C (the specification for the model 261K). The same considerations apply for offset voltage, accounting for its low value and the excellent long term stability of this amplifier.

The chopping signal is generated by a standard multivibrator. The frequency is not critical, and the multivibrator circuit is protected against latch-up.

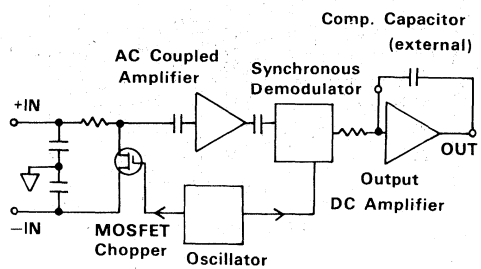


Figure 7. Model 261 Block Diagram

APPLICATION NOTES

Measurement of small signals or accurate handling of larger signals always requires care. Model 261 was specifically designed to minimize the problems raised by dc drift. To obtain best results, it is necessary to maintain good engineering practice and to observe a few requirements for optimizing performance of this precision instrument.

OFFSET VOLTAGE AND CURRENT TRIM

With the trim terminal connected to common, initial offset voltage of the model 261 is less than 25μV. An additional offset voltage is developed by the flow of the input bias current through the resistance of the signal source. With a 10,000 ohm source resistance and worst case bias current of 300pA, the maximum additional offset voltage would be only 3μV. For many applications, these offset voltages may be ignored, and the expense of a trim potentiometer and its adjustment is avoided. If the application requires lower offsets, an external 50,000 ohm trim potentiometer may be connected to zero the offset voltages, as shown previously. This trimming operation will not affect the drift or noise characteristics of the model 261.

INVERTING AND DIFFERENTIAL INPUT OPERATION

The input current to the amplifier's (–) terminal is less than ±10nA. Differential input operation of the amplifier is allowable, but the impedance from the inverting terminal to ground should not exceed 5000 ohms, and the common mode voltage range for best performance should not be exceeded. For purely inverting applications the user should select Analog Devices' models 234 or 235 chopper stabilized amplifiers, which are optimized for inverting operation.

SELECTABLE BANDWIDTH

For practical low-frequency applications, the model 261 uses an external compensation capacitor to determine the gain-bandwidth product. Its value may be chosen to allow the use of the maximum 100Hz –3dB bandwidth, at any given value of closed loop gain. By using a larger value of compensation capacitance, the bandwidth can be limited to any desired value below 100Hz, as required by the application. The minimum value of the required compensation capacitor, in μF, is 1000/GB, where G is the desired closed-loop dc gain, and B is the –3dB bandwidth. For example, the minimum value of recommended capacitance (for 100Hz bandwidth to –3dB) is

10/G. Shown in Figure 8 are curves of the amplifier's response for various closed loop gains while using values of capacitance appropriate for maintaining 100Hz (-3dB) bandwidth. Figure 9 illustrates the amplifier's open-loop response with various values of the compensation capacitor. It is recommended that the capacitor be polycarbonate, mylar, mica, glass or polystyrene for best performance.

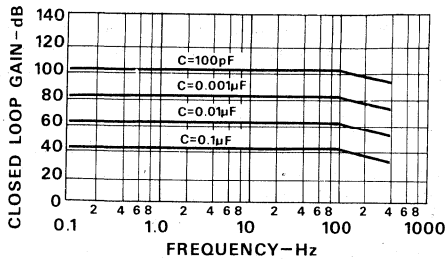


Figure 8. Compensation vs. Gain for 100Hz Bandwidth

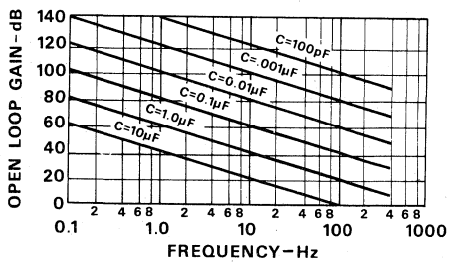


Figure 9. Open Loop Response vs. Compensation

FULL POWER RESPONSE

Full power output at any frequency can be obtained only with closed loop gains exceeding 10. This is due to the common mode voltage limitation described below.

The maximum full power output frequency is 50Hz, and will be obtained when using compensation capacitors of less than 0.013μF. For larger compensation capacitors, f_p is given by the formula:

$$f_p \text{ (Hz)} = 0.66/C \text{ (}\mu\text{F)}$$

When using a low gain, for instance 10, the maximum f_p will be 0.66Hz due to the 1.0μF required compensation capacitor for this closed loop gain. Under such conditions the user may wish to employ the compensation circuit of Figure 10. This will increase f_p to 5Hz (for a gain of 30). For higher gains, an increase in f_p will be obtained (with the same circuit), although the rise in f_p will not be proportionately as large.

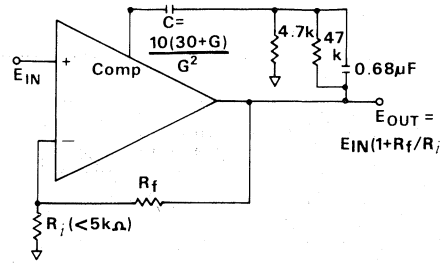


Figure 10. Compensation for Increased f_p

COMMON MODE CONSIDERATIONS

In the model 261, the maximum safe input voltage, both differential and common mode, exceeds ±20 volts. However, in order to maintain the specified Common Mode Rejection Ratio of 300,000 it is necessary that common mode voltage be limited to ±1.0 volts for the model 261K and ±0.5 volts for the model 261J. These values will not be exceeded by normal input signal swings if the amplifiers closed loop gain exceeds 10 and 20, respectively. Since most applications will use this amplifier at gains of 100 or more, the specified common mode range should prove entirely adequate.

COMMON MODE REJECTION

Model 261 is designed to provide high stability, high gain and low noise in non-inverting applications where the high input impedance minimizes input signal attenuation. Although operation as a differential amplifier is possible, it is not recommende

In the non-inverting mode, there is a source of error due to the common mode voltage; however this error term can be completely ignored since the error due to open loop gain will dominate.

INVERTING INPUT TERMINAL RESISTANCE (R_i)

An attempt should be made to maintain low resistance from the inverting input terminal to ground. This will prevent the negative input's bias current from degrading the offset performance of the amplifier. This restriction in no way relates to the source resistance seen by the positive (non-inverting) input terminal.

Isolation Amplifiers

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•New product since the *1980 Data-Acquisition Components and Subsystems Catalog*

Selection Guide
Isolation Amplifiers

SELECTION GUIDE – ISOLATION AMPLIFIERS

		WIDE BAND, PRECISION	LOWEST COST		±6500V MAX DIFF INPUT		UNCOMMITTED OP AMP	HYBRID		
								INDUSTRIAL	MEDICAL	MILITARY
		289	290A	292A	284J	286J	277	AD293	AD294A	AD294S/ 883B
Max Input/Output CMV	±2500V dc pk max	•			•	•	•	•	•	•
	±1500V dc pk max		•	•						
	±850V dc pk max									
Nonlinearity	±0.012%	•					•			
	±0.025%				•	•		•	•	
	±0.050%									
	±0.100%		•	•						•
Output Voltage	±5V				•					
	±10V	•	•	•		•	•	•	•	•
Gain Range	1–1000V/V						•	•	•	•
	1–100V/V	•	•	•		•				
	1–10V/V				•					
Synchronized Operation	With External Oscillator			•		•				
	With Internal Oscillator	•						•	•	
Output Amplifier		•					•	•	•	•
Isolated Power Out		•	•	•	•	•	•			
Defibrillation Protection					•	•			•	
Three Port Isolation		•						•	•	•
Volume I Page		5-35	–	–	–	–	–	5-27	5-27	5-27
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See *Signal Conditioners* for other analog/analog products with input/output isolation—including current-output devices.

Orientation
Isolation Amplifiers

The *isolation amplifier* (or *isolator*) has an input circuit that is galvanically isolated from the power supply and the output circuit. Isolators are intended for applications requiring safe, accurate measurement of dc and low-frequency voltage or current in the presence of high common-mode voltage (to thousands of volts) with high CMR, line-receiving of signals transmitted at high impedance in noisy environments, and for safety in general-purpose measurements where dc and line-frequency leakage must be maintained at levels well below certain mandated minima.* Principal applications are in electrical environments of the kind associated with medical equipment, conventional and nuclear power plants, automatic test equipment, and industrial process-control systems.

Analog Devices Isolators described in this section use electromagnetically coupled high-frequency carrier techniques for communication of power to and signals from the input circuit.

CHOOSING AN ISOLATOR

The choice of an isolator depends on the desired *functional characteristics* and the required *specifications*. Functional characteristics include such considerations as number of channels, range of output common-mode (output to power supply), nature of the front-end amplifier (amplification only or general op-amp functioning), and the availability of isolated power for additional external front-end circuitry. Key specifications include performance specs and "absolute max/min" mandated safety specifications. Definitions of specifications follow this section. In addition to the products listed here, which are recommended for new designs, a number of older products are still available; data sheets are available upon request. In addition to the useful applications information on the data sheets published here, a designers' guide[1], available upon request, provides information useful to the circuit designer.

The devices described in this section are all voltage-output isolation amplifiers, useful in general-purpose circuit applications for instrumentation amplifiers or op amps where isolation is a necessity. In addition to these devices, there are a growing number of isolators available from Analog Devices that perform dedicated functions, for use where isolation is necessary or desirable. Some of their applications can be seen in the *Transducer Interfacing Handbook*[2].

Data for other products employing isolation techniques may be found in these sections of this Volume: Transducers and Signal Conditioners, Digital-to-Analog Converters, Synchro/Resolver-Digital Converters, Digital Panel Instruments, Intelligent Measurement-and-Control Subsystems, Linear Test Systems, and MACSYM. Power Supplies and DC-DC Converters, being transformer-coupled, also provide isolation.

*Examples of such requirements may be found in UL STD 544 and SWC (Surge Withstand Capability) in IEEE Standard for Transient Voltage Protection 472-1974.

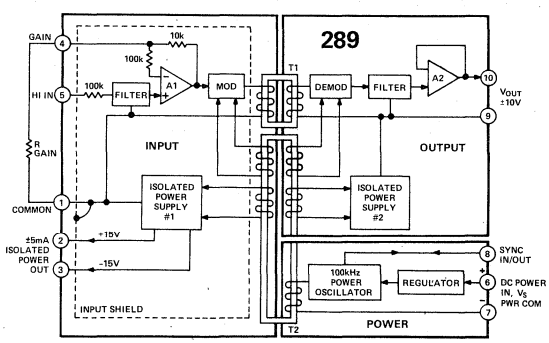
[1] *Analog Devices Isolation and Instrumentation Amplifiers Designer's Guide"* (1980)

[2] Sheingold, D. H., ed. *Transducer Interfacing Handbook—A guide to analog signal conditioning.* Norwood MA 02062 (P.O. Box 796): Analog Devices, Inc., 1980, $14.50

Examples of such products include the 2B54 Thermocouple/mV 4-Channel Multiplexer/Amplifier, the 2B22 Voltage-or-Current-to 4-to-20mA Converter, the DAC1423 10-bit Digital-to-4-to-20mA Converter, the AD2036, AD2037, and AD2038 Scanning Panel Instruments, and the μMAC-4000 Intelligent Measurement-and-Control Subsystems.

Functional Characteristics The figure shows the circuit architecture of a self-contained isolator, Model 289. The various models differ, but their properties can be discussed in terms of the device shown. An isolator of this type requires power from a two-terminal dc supply. An internal oscillator converts the dc power to ac, which is transformer-coupled to the shielded input section, then converted to dc for the input stage and the auxiliary power output. The ac carrier is also modulated by the amplifier output, transformer-coupled to the output stage, demodulated by a phase-sensitive demodulator (using the carrier as the reference), filtered, and amplified, using isolated dc power, derived from the carrier.

The amplifier in this example is a resistor-protected op amp (actually, the protection works both ways – it protects the amplifier against differential overloads (120V rms continuous) and it protects sensitive input sources from supply voltage if the amplifier malfunctions), connected for a programmable gain from 1 to 100V/V, as determined by a single external resistor. Since both input terminals are floating, the amplifier functions effectively as an instrumentation amplifier. All but one of the amplifiers in this series function in the instrumentation-amplifier mode, but with various gain ranges. The 277 is an exception; its input stage is an uncommitted high-gain low-drift, low-noise op amp, and the output terminal of the input stage is available for feedback connections to perform a wide range of single-ended or differential operations. Because of the transformer coupling, the outputs of all these devices are isolated from their input stages.



In the figure, it can be seen that the demodulator drive is magnetically coupled from the oscillator to the output stage.

This permits the output to operate at a dc common-mode potential with respect to power common. An isolator of this type is said to provide *three-port* isolation, because there are three isolated ports: input, power supply, and output. The AD293 and AD294 have 3 isolated sections, but the op amp supply is tied to output common. The data sheets carry block diagrams, which show the architecture of each device; 3-port devices, in general, have an output common-mode voltage spec in the "Rated Output" section. Two-port devices are those in which there is a dc connection between the oscillator power supply and the output stage.

The 289, as can be seen, is a completely self-contained device. There are applications for which a degree of "unbundling" can lead to economy and improved performance. For example, if there are many input channels to be isolated, economies can be realized by the use of a common oscillator. In addition, the common oscillator makes it possible to avoid the possibility of small errors due to beat frequencies developed by small amounts of crosstalk.

Several synchronized multichannel devices are available. Model 292A is essentially a 290A with a power amplifier instead of an oscillator. It requires a dc power input and a pair of leads for a low-power oscillator input, which can be furnished by a 281 synchronizable oscillator. The 281 will drive from one to 16 292As, and it will also synchronize additional 281s for increments of up to 16 292s per 281.

SPECIFICATIONS

The illustration on the next page shows a typical specification block and defines the specifications of key interest.

NONLINEARITY – This is the peak deviation from a best straight line, expressed as a % of peak-to-peak output. Should be considered when signal fidelity is of prime importance.

MAX SAFE DIFFERENTIAL INPUT – Max voltage that can be safely applied across input terminals. Important to consider for fail-safe designs in the presence of high voltages.

OVERLOAD RESISTANCE – This is the apparent input impedance under conditions of amplifier saturation. It limits differential fault currents.

INPUT NOISE – Total noise, referred to the input. Facilitates comparison with expected signal input levels.

ISOLATED SUPPLY – Dual supply voltages, completely isolated from the input power supply terminals, provide the capability to excite floating input signal conditioners, front-end amplifiers, as well as remote transducers.

Model	289K
GAIN (NONINVERTING)	
Range	1 to 100V/V
Formula	$G = 1 + \frac{10k\Omega}{R_G\,(k\Omega)}$
Deviation from Formula	±1.5% max
vs. Temperature (0 to +70°C)[1]	15ppm/°C typ (50ppm/°C max)
Nonlinearity, (±5V Swing)[2,3]	±0.025% max
INPUT VOLTAGE RATINGS	
Linear Differential Range (G = 1V/V)	±10V min
Max Safe Differential Input	
Continuous	120V rms
1 Minute	240V rms
Max CMV (Inputs to Outputs)	
Continuous ac or dc	±2500V peak max
ac, 60Hz, 1 Minute Duration	2500V rms
CMR, Inputs to Outputs 60Hz	
$R_S \leq 1k\Omega$, Balanced Source Impedance	120dB
$R_S \leq 1k\Omega$, HI IN Lead Only	104dB min
Max Leakage Current, Input to Output @ 115V rms, 60Hz ac	2μA rms max
INPUT IMPEDANCE	
Differential	$33pF \| 10^8\,\Omega$
Overload	100kΩ
Common Mode	$20pF \| 5 \times 10^{10}\,\Omega$
INPUT DIFFERENCE CURRENT	
Initial @ +25°C	10nA (75nA max)
vs. Temperature (0 to 70°C)	0.15nA/°C
INPUT NOISE (GAIN = 100V/V)	
Voltage	
0.05Hz to 100Hz	8μV p-p
10Hz to 1kHz	3μV rms
Current	
0.05Hz to 100Hz	3pA rms
FREQUENCY RESPONSE	
Small Signal –3dB	
G = 1V/V	20kHz
G = 100V/V	5kHz
Full Power, 10V p-p Output	
G = 1V/V	5kHz
G = 100V/V	3.5kHz
Full Power, 20V p-p Output	
G = 1V/V	2.3kHz
G = 100V/V	2.3kHz
Slew Rate	0.14V/μs
Settling Time[4], ±0.05%, ±10V Step	400μs
OFFSET VOLTAGE, REFERRED TO INPUT	
Initial, @ +25°C	$\pm 5 \pm \frac{10}{G}$ mV max
vs. Temperature (0 to +70°C)	$\pm 15 \pm \frac{100}{G}$ max
vs. Supply Voltage (+15V to +20V change)	$\pm 2 \pm \frac{10}{G}\,\mu V/V$
RATED OUTPUT	
Voltage, 2kΩ Load	±10V min
Output Impedance	<1Ω(dc to 100Hz)
Output Ripple, 0.1MHz Bandwidth	
No Signal IN	5mV p-p
$+10V_{IN}$	50mV p-p
ISOLATED POWER SUPPLY	
Voltage	±15V dc
Accuracy	±10%
Current	±5mA, min
Regulation No Load to Full Load	±5%
Ripple, 0.1MHz Bandwidth, No Load	25mV p-p
Full Load	75mV p-p
POWER SUPPLY, SINGLE POLARITY[5]	
Voltage, Rated Performance	+14.4V to +25V
Voltage, Operating	+8.5V to +25V
Current, Quiescent (@ V_S = +15V)	+25mA
TEMPERATURE RANGE	
Rated Performance	0 to +70°C
Operating	–15°C to +75°C
Storage	–55°C to +85°C
CASE DIMENSIONS	1.5" X 2.0" X 0.75"

NOTES:
[1] Gain temperature drift is specified as a percentage of output signal level.
[2] Gain nonlinearity is specified as a percentage of 10V pk-pk output span.
[3] When isolated power output is used, nonlinearity increases by ±0.002%/mA of current drawn.
[4] G = 1V/V; with 2-pole, 5kHz output filter.
[5] Recommended power supply, ADI model 904, ±15V @ 50mA output.
Specifications subject to change without notice.

CMV, INPUTS TO OUTPUTS – Voltage that may be safely applied to *both* inputs with respect to outputs or power common. Necessary consideration in applications with high CMV input or when high voltage transients may occur at the input.

CMR, INPUTS TO OUTPUTS – Indicates ability to reject common mode voltages between inputs and outputs. Important when processing small signals riding on high common mode voltages.

LEAKAGE CURRENT – Maximum input leakage current when power-line voltage is impressed on inputs. Vital consideration for patient safety in medical applications.

OFFSET VOLTAGE REFERRED TO INPUT – Total input drift is composed of two sources (input and output stage drifts) and is gain (G) dependent. Referring offsets to the input allows them to be compared to signal levels.

ANALOG DEVICES

Hybrid Industrial/ Medical Isolation Amplifier

AD293/AD294

FEATURES

High Common Mode Voltage: AD293 ±2500V peak max
AD294 ±8000V peak max
Nonlinearity: ±0.05% max (AD293B)
Adjustable Input & Output Gain: 1V/V to 1000V/V
Complies with NEMA ICS1-111
Meets UL Std 544 Leakage: 2.0μA max @ 115V ac, 60Hz
Hermetically Sealed Hybrid Construction
Military Versions Available
Low Cost:

APPLICATIONS

Off Ground Signal Measurement
Industrial Control
Nuclear & Military Instrumentation
High Voltage Protection for Data Acquisition Systems
Medical Diagnostic and Patient Monitoring Equipment

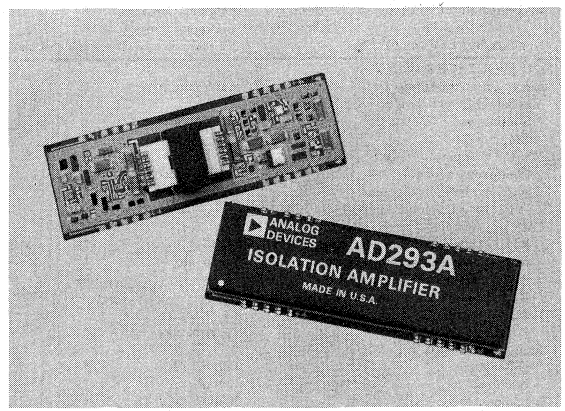
GENERAL DESCRIPTION

The AD293/AD294 are low-cost, high-accuracy, high reliability hybrid isolation amplifiers designed specifically for industrial, medical and military applications. The AD293 is available in three selected versions for industrial and military use; two of which are graded for nonlinearity, the AD293A (±0.1% max) and the AD293B (±0.05% max). The third version, AD293S/883B, is designed for extended temperature operation (−55°C to +125°C) offering screening and testing per MIL-STD-883B. The AD294A provides low leakage and higher CMV capability required for medical applications. Using modulation techniques with a proprietary hybrid magnetic transformer, the AD293/AD294 provides isolation from ground loop and leakage paths and guarantees common mode voltage protection up to ±2500V/±8000V peak respectively. All versions provide a small signal (−3dB) frequency response from dc to 2.5kHz and a large signal (full power) frequency response from dc to 250Hz at a gain of 1V/V. Gain, from 1V/V to 1000V/V, can be programmed at either the input section or output section allowing for user flexibility.

The AD293/AD294 are available in hermetically sealed 40 pin DIP ceramic packages that insure quality performance, high stability, and high reliability. Input/output pin spacing comply with NEMA (ICS1-111) separation specifications which is necessary for many industrial applications.

WHERE TO USE THE AD293/AD294

Industrial: In process control systems, high CMV instrumentation and multi-channel computer interface systems, the AD293 provides guaranteed protection against high transient voltages, lethal ground fault currents and high common mode voltages.



Medical: In biomedical and patient monitoring equipment such as ECG recorders, diagnostic systems and blood pressure monitors, the AD294A offers protection from lethal ground fault currents as well as 8kV peak defibrillator pulse inputs.

Low level signal recording and monitoring is achieved with the AD294A's low input noise (10μV p-p @ G = 100V/V) high CMR (100dB min @ 60Hz).

Military: In servo systems and instrumentation the AD293S/883B provides isolation from both ground loops and high common mode voltages.

DESIGN FEATURES AND USER BENEFITS

Adjustable Gain: Gain can be selected at either the input, output, or both. Thus, circuit response can be tailored to the user's application. The input gain can be selected from 1V/V to 100V/V with a single resistor. The output gain can be selected from 1V/V to 10V/V with or without compensation. The AD293/AD294 provides the user with flexibility for circuit optimization without requiring external active components.

Buffered Output: The AD293/AD294 prevent inaccuracies related to low impedance loads by providing an uncommitted output amplifier capable of supplying ±10V @ 2mA min.

Isolated Power: Low level isolated power provides −13V @ 200μA. This feature permits the AD293/AD294 to enhance system designs by eliminating the need for a separate isolated dc/dc converter.

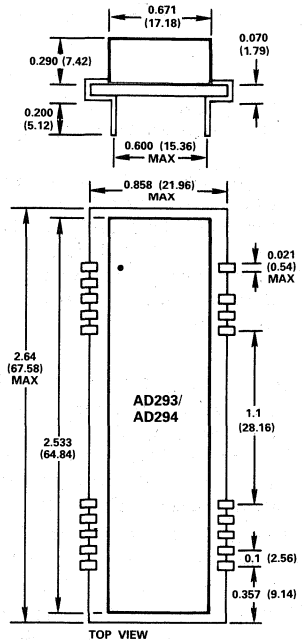
SPECIFICATIONS (typical @ + 25°C, & V_S = 15V unless otherwise noted)

MODEL	AD293A	AD293B	AD293S/883B†	AD294A
GAIN				
Range	1 to 1000V/V	*	*	*
Formula (Input)	$G_{IN} = \left(1 + \frac{100k}{R_G}\right)$; $R_G \geq 1k\Omega$; G_{IN} max = 100			
(Output)	$G_{OUT} = \left(1 + \frac{R_A}{R_B}\right)$; $1 \leq G_{OUT} \leq 10$; G_{OUT} max = 10			
Deviation from Formula	± 1.0%	*	*	*
vs. Temperature (− 25°C to + 85°C)[1] (Gain = 1)	± 50ppm/°C max	*	*	*
(Gain > 1)	± 100ppm/°C max	*	*	*
Nonlinearity (± 5V swing)[2,3]	± 0.1% max	± 0.05% max	*	*
INPUT VOLTAGE RATINGS				
Linear Differential Range	± 10V min	*	*	*
Max Safe Differential Input				
Continuous	120V rms max	*	*	*
1 Minute	240V rms max	*	*	*
Max CMV (Inputs to Outputs)				
Continuous (ac or dc)	± 2500V peak	*	*	± 3500V peak
ac, 60Hz, 1 minute Duration	2500V rms	*	*	3500V rms
Pulse, 10ms Duration, 1 pulse/10 sec	—	—	—	± 8000V peak
CMR				
$R_S \leq 1k\Omega$ Balanced Source Impedance	115dB	*	*	*
$R_S \leq 1k$ Source Impedance Imbalance	100dB min	*	*	*
$R_S \leq 5k$ Balanced Source Impedance	—	—	—	115dB
$R_S \leq 5k$ Source Impedance Imbalance	—	—	—	100dB min
Leakage Current, Input to Output				
@ 115V ac, 60Hz	2μA rms max	*	*	*
Input Impedance, G = 1				
Differential	$150pF \| 10^8\Omega$	*	*	*
Overload	100kΩ	*	*	*
Common Mode	$30pF \| (5 \times 10^{10}\Omega)$	*	*	*
Input Difference Current				
Initial @ + 25 °C	2nA (7nA max)	*	*	*
vs. Temperature	2pA/°C	*	*	*
Input Noise (G = 100V/V)				
Voltage				
0.05Hz to 100Hz	10 μV p-p	*	*	*
10Hz to 1kHz	5μV rms	*	*	*
Current				
0.05Hz to 100Hz	50pA p-p	*	*	*
FREQUENCY RESPONSE				
Small Signal (− 3dB) G = 1V/V to 100V/V	2.5kHz	*	*	*
Full Power, 20V p-p Output				
G = 1V/V (G_{IN} = 1V/V, G_{OUT} = 1V/V)	250Hz	*	*	*
G = 100V/V (G_{IN} = 100V/V, G_{OUT} = 1V/V)	250Hz	*	*	*
G = 10V/V (G_{IN} = 1V/V, G_{OUT} = 10V/V)	2.5kHz	*	*	*
Slew Rate	9.1V/ms	*	*	*
OFFSET VOLTAGE, REFERRED TO INPUT				
Initial, @ + 25°C, max	$\left(\pm 8 \pm \frac{10}{G}\right)$mV	*	*	*
vs. Temperature				
(− 25°C to + 85°C) max	$\left(\pm 25 \pm \frac{150}{G}\right)\mu V/°C$	$\left(\pm 5 \pm \frac{100}{G}\right)\mu V/°C$	*	*
vs. Supply Voltage	75μV/V	*	*	*
RATED OUTPUT				
Voltage, 5kΩ Load	± 10V min	*	*	*
Output Impedance	< 1Ω	*	*	*
Output Ripple, (dc to 100kHz) Bandwidth	4mV p-p	*	*	*
POWER SUPPLY				
Voltage, Rated Performance	± 15V dc ± 5%	*	*	*
Voltage, Operating	± 15V dc ± 10%	*	*	*
Current, Quiescent (@ V_S = ± 15V)	+ 10mA, − 1mA	*	*	*
ISOLATED POWER	− 13V dc @ 200μA	*	*	*
TEMPERATURE RANGE				
Rated Performance	− 25°C to + 85°C	*	− 55°C to + 125°C	*
Operating	− 40°C to + 100°C	*	− 55°C to + 125°C	*
CASE DIMENSIONS	2.64″ × 0.86″ × 0.35″	*	*	*

NOTES:
*Specifications same as AD293A
†883B MIL version to be available in January, 1982.
[1]Gain temperature drift is specified as a percentage of output signal level.
[2]Gain nonlinearity is specified as a percentage of 10V pk-pk output span.
[3]Recommended power supply, ADI Model 904, ± 15V @ 50mA output.
Specifications are subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



RECOMMENDED MATING SOCKET: AUGAT NO. 240-AG39D (TO PRESERVE THE HIGH CMV INTEGRITY OF THE AD293/AD294 REMOVE ALL UNUSED SOCKET PINS.)

PIN DESIGNATIONS

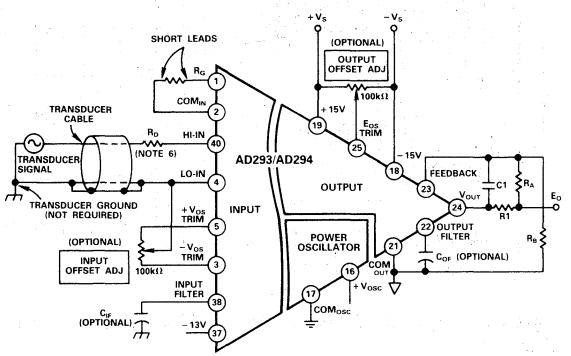
PIN	FUNCTION	PIN	FUNCTION
1	R_G	40	HI-IN
2	COM_{IN}		
3	$-V_{OS}$ TRIM	38	INPUT FILTER
4	LO-IN	37	−13V
5	$+V_{OS}$ TRIM	36	NC
16	$+V_{OSC}$	25	E_{OS} TRIM
17	COM_{OSC}	24	V_{OUT}
18	−15V	23	FEEDBACK
19	+15V	22	OUTPUT FILTER
20	SYNC	21	COM_{OUT}

Synchronization: Due to their hybrid transformer design and low power operation, RFI levels emitted by the AD293/AD294 are very low. A synchronization terminal is provided for use in high accuracy multi-channel applications. By connecting the synchronization terminals together and driving them with a TTL device, the AD293/AD294 internal oscillators will synchronize and "beat frequency" interference will be eliminated.

High Reliability: The AD293/AD294 are designed specifically to provide highly reliable operation in extremely harsh environments. These devices are available in hermetically sealed ceramic packages which use hybrid techniques and incorporate a revolutionary new hybrid magnetic transformer eliminating traditional wire wound methods. The AD293S/883B is manufactured and tested per MIL-STD-883B having a calculated MTBF of 1,682,369 hours.

INTERCONNECTIONS AND SHIELDING TECHNIQUE

To preserve the high CMR performance of the AD293/AD294, care must be taken to keep the capacitance balanced about the input terminals. Use twisted shielded cable, for the input signal, to reduce inductive and capacitive pickup. The cable shield should be connected to the common mode signal source and as close as possible to their respective terminal connections so pick-up can be minimized (shown in Figure 1).



NOTES:

1. GAIN RESISTORS R_G, R_A AND R_B, 1% 50ppm/°C METAL FILM TYPE.
2. INPUT GAIN $= 1 + \frac{100k}{R_G}$; $R_G \geq 1k$; MAX INPUT GAIN = 100V/V.
   $R_1 = 100\Omega$ AND $C_1 = 100pF$ (OPTIONAL); REQUIRED ONLY FOR CAPACITIVE LOADS >1000pF.
3. OUTPUT GAIN $= \frac{R_A \cdot R_B}{R_B}$; $1 \leq$ OUTPUT GAIN ≤ 10.
4. $C_{IF} = \frac{1}{2\pi F(97.5 \times 10^4)}$ FARADS.
5. $C_{OF} = \frac{1}{2\pi F(10^5)}$ FARADS.
6. R_D IS REQUIRED ONLY FOR THE AD294 TO PROVIDE PROTECTION AGAINST DEFIBRILLATOR PULSES. USE TWO 240kΩ 1/2 WATT RESISTORS WHEN MOUNTING, PLACE THEM IN SERIES AND AWAY FROM THE PCB.

Figure 1. Basic Isolator Interconnection

THEORY OF OPERATION

The AD293/AD294 attribute their outstanding performance to the innovation of a hybrid magnetic ceramic transformer T1 (shown in the block diagram of Figure 2). Windings are screened on two ceramic alumina substrates which are placed together separated by a ceramic isolation barrier. Then an E-core is carefully fitted around the substrates to complete the transformer.

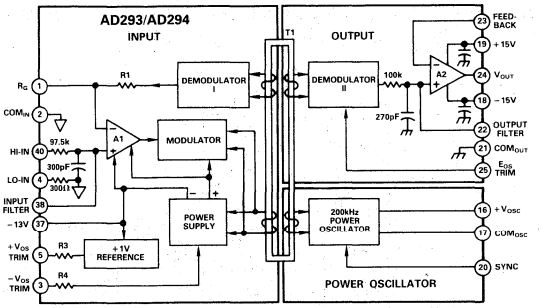


Figure 2. AD293/AD294 Block Diagram

Incorporating the carrier isolation technique, both power and signals are transferred between the amplifier's input stage and output circuitry via T1. The input signal is filtered and appears at the input of the inverting amplifier A1. This signal is then amplified by A1, with its gain (1V/V to 100V/V) determined by the value of resistance connected between R_G and COM_{IN}. The output of A1 is modulated, carried across the isolation barrier by signal transformer T1, and demodulated. The demodulator output voltage is filtered and then buffered by A2. Output gain (1V/V to 10V/V) and frequency compensation is determined by the value of resistance and capacitance selected between A2's feedback, V_{OUT}, and COM terminals. The 200kHz asymmetric square wave power oscillator drives the primary windings of transformer T1. The secondary windings of T1 then energizes the input power supply and drives both the modulator and demodulator.

INTERELECTRODE CAPACITANCE AND TERMINAL RATINGS

Capacitance: Interelectrode terminal capacitance effects are developed from stray capacitance that couple the input and output terminals together. The difference shown in Figure 3 between the AD293 and AD294 is a result of the separate transformer designs. Each terminal capacitance is shunted by leakage resistance exceeding $3.4 \times 10^9\Omega$.

Terminal Ratings: CMV performance is given in peak pulse and continuous ac or dc peak ratings. Continous peak ratings apply from dc up to the normal full power response frequencies. Figure 3 illustrates the AD293/AD294 ratings between terminals.

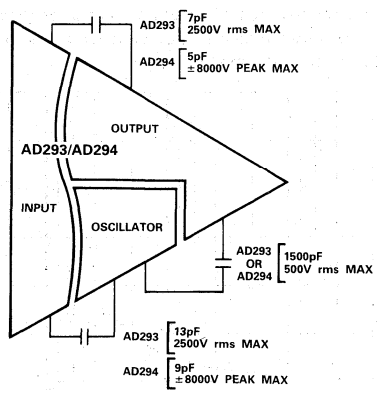


Figure 3. Interelectrode Capacitance and Terminal Ratings

OFFSET AND GAIN TRIM PROCEDURES

The calibration procedure, shown in Figure 4, illustrates the recommended techniques which can be used to minimize output error. In this example, the output span is +10V to −10V and gain = 100V/V (G_{IN} = 10V/V; G_{OUT} = 10V/V).

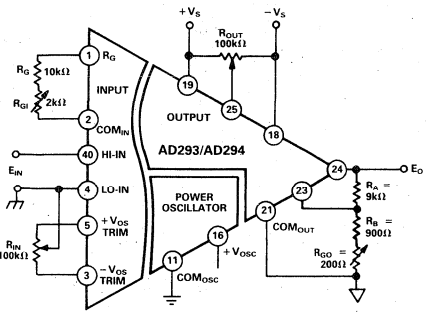


Figure 4. Recommended Offset & Gain Adjustments

Offset Adjustment

1. Set G_{OUT} = 1V/V by disconnecting R_B from COM.
2. Apply E_{IN} = 0 volts and adjust R_{IN} for E_O = 0 volts.
3. Connect R_B to COM.
4. Adjust R_{OUT} for E_O = 0 volts.

Gain Adjustment

5. Set G_{OUT} = 1V/V by disconnecting R_B from COM.
6. Apply E_{IN} = +1.000V and adjust R_G for E_O = +10.000V.
7. Connect R_B to COM.
8. Apply E_{IN} = +0.100V and adjust R_G for E_O = +10.000V.

LEAKAGE CURRENT LIMITS

The low coupling capacitance between input and output yields a ground leakage current of less than 2μA rms of 115V ac, 60Hz in the AD293/AD294 which meet standards established by UL STD 544.

For medical applications, the AD294 is designed to improve on patient safety current limits proposed by the F.D.A., U.L., A.A.M.I. and other regulatory agencies.

In patient monitoring equipment, such as ECG recorders, the AD294A will provide adequate isolation without exposing the patient to potentially lethal microshock hazards. With the use of passive components for input protection, this design limits input fault currents even under amplifier failure conditions.

PERFORMANCE CHARACTERISTICS

Phase vs. Frequency: The phase vs. frequency responses, for the AD293/AD294, is shown in Figure 5. The bandwidth is sufficient for the majority of isolation applications where accurate signal measurements must be made in the presence of noise and high common mode voltages.

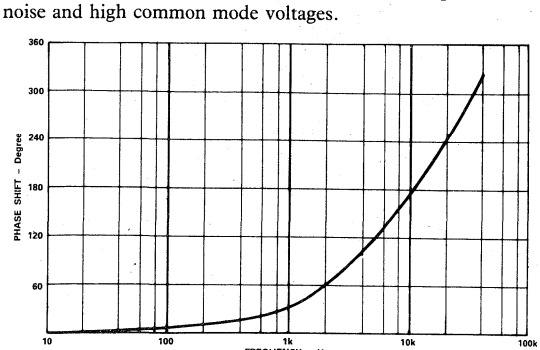


Figure 5. Typical AD293/AD294 – Phase vs. Frequency

Common Mode Rejection: Input-to-output CMR is dependent on source impedance imbalance, input signal frequency and amplifier gain. CMR is rated at 115V ac, 60Hz and 1kΩ (AD293)/5kΩ (AD294) source impedance imbalance at a gain of 1V/V. Figure 6 illustrates the CMR vs. frequency characteristics for the AD293/AD294. CMR approaches 144dB at dc with sources impedance as high as 1kΩ(AD293)/5kΩ (AD294).

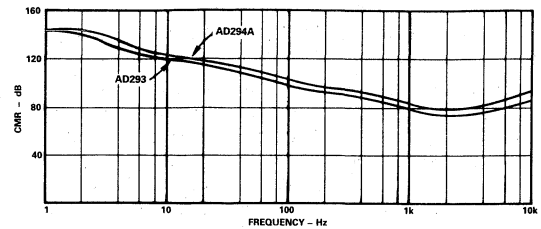


Figure 6. Typical AD293/AD294 – CMR vs. Frequency

Figure 7 illustrates the effect of source impedance imbalance on CMR performance at 60Hz for various gain settings. CMR is maintained greater than 60dB for source imbalances up to 100kΩ. As shown, increasing isolator gain increases CMR.

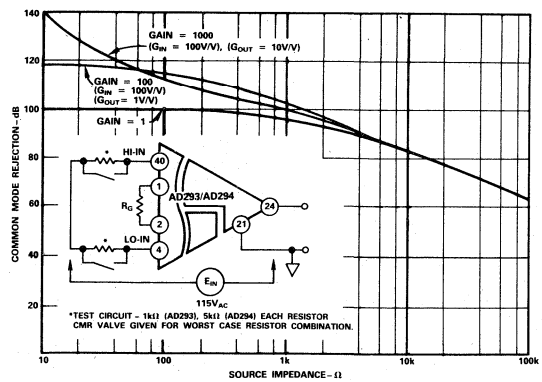


Figure 7. Typical AD293/AD294 – CMR vs. Source Impedance

Input Voltage Noise: Voltage noise, referred to input, is dependent on gain and bandwidth as illustrated in Figure 8. RMS voltage noise in a bandwidth from 0.05Hz to 100kHz is shown on the horizontal axis. The noise in a bandwidth from 0.05Hz to 100Hz is typically 5μV pk-pk at a gain of 1000V/V.

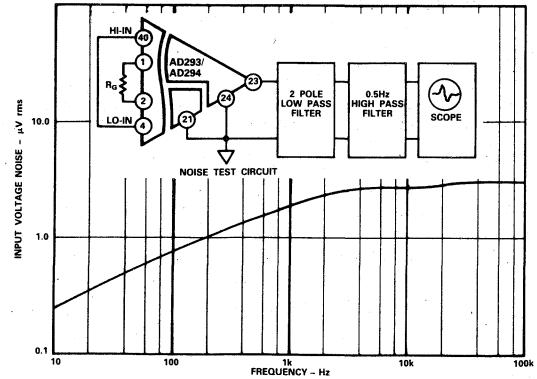


Figure 8. Typical AD293/AD294 – Input Noise vs. Frequency

The peak-to-peak value is derived by multiplying the rms value @ F = 100Hz (0.75μV rms) by 6.6.

For applications requiring improved noise performance, additional low pass filters may be placed at either the input or output sections to selectively roll-off noise and undesired signals beyond the bandwidth of interest.

Gain Nonlinearity vs. Gain

Figure 9, shows the AD293/AD294 gain nonlinearity vs. gain as a function of output gain. As input gain is increased, gain nonlinearity increases. Although, as output gain is increased to ten, gain nonlinearity decreases.

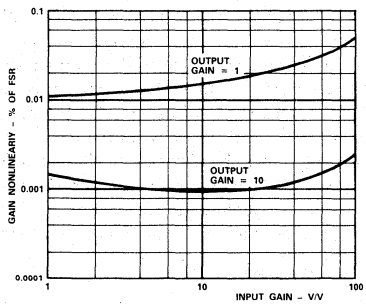


Figure 9. Typical AD293/AD294 – Gain Nonlinearity vs. Gain as a Function of Output Gain

Full Power Bandwidth vs. Gain

Figure 10 shows the −3dB full power bandwidth vs. gain with the input and output gain curves shown separately. As shown, the −3dB full power bandwidth with gain provided at the input is typically 330Hz. But with gain provided only at the output, the −3dB full power bandwidth approaches the small signal bandwidth.

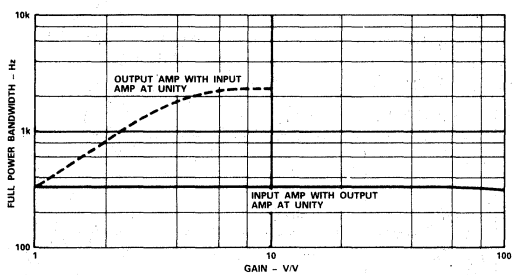


Figure 10. Typical AD293/AD294 - Full Power Bandwidth vs. Gain

Gain Nonlinearity vs. Output Swing

The gain nonlinearity vs. output swing, for the AD293/AD294, is illustrated in Figure 11. As shown, increasing either the input gain or the output swing will cause the gain nonlinearity to increase. Here the input gain is varied from 1V/V to 100V/V.

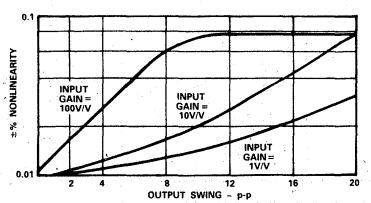


Figure 11. Typical AD293/AD294 - Gain Nonlinearity vs. Output Swing

OPTIMIZING THE AD293/AD294

The AD293/AD294 can be optimized for many applications as shown by the performance charts on the previous page. Gain and filtration can be implemented on both the input and output stages while providing true galvanic isolation. Provisions for an additional two poles of filtration are also available without the addition of external operational amplifiers. Due to their low power consumption and novel transformer design, the beat frequency problem normally associated with adjacent isolation amplifiers is eliminated. A sync terminal is provided for applications where ultra-sensitive circuitry might interpret the isolator carrier frequency.

SELECTING GAIN

The AD293/AD294 contain both input and output amplifiers (see Figures 1 and 2), the gains of which can be set independently. The selection of a particular combination tailors isolator properties to the application, minimizes errors, and optimizes frequency response.

Nonlinearity is the deviation of response from a straight line. This error arises from slight differences in responses of the input demodulator I and demodulator II, their respective transformer windings responses, and rectification of carrier signal in the input stage due to large signal amplitudes in this section. Hence, linearity is best obtained by raising output gain and lowering input gain.

Gain errors are deviations in slope from the predicted gain equation. Gain errors are attributable to the difference in gain between demodulators I and II. These errors are quite small, due to the highly predictable and uniform nature of the thick-film transformer. The gain drift of this portion of gain error is also small. Since this gain error source dominates at unity gain, the unity gain temperature coefficients of these units is very small. As input gain is taken, errors arise due to the inaccuracies of the internal feedback resistor R8, and user selected R_G. Failure of these resistors to temperature track introduces a gain TC. R8 is trimmed within ±2% and has a TC of ±100ppm/°C. Since the temperature coefficient of R8 is not user controllable, best gain TC at low gains is favored by taking output gain. The output stage also contributes gain error only when gain is taken. Here, both the feedback and gain resistors are user supplied and can be made as accurate as desired.

Offset errors are apparent both in the input stage and in the transformer-output stage combination. Provisions are available to eliminate these initial offset errors at both the input and output stages through trim potentiometers. These errors also have temperature dependence where at unity gain, output offset drift dominates. Taking output gain multiplies output drift by the gain taken. Taking input gain helps dilute output stage offset drift and is recommended where offset drift is to be minimized.

Errors due to small signal and large signal bandwidth limitations can also be optimized in the AD293/AD294. Small signal bandwidth is limited by lack of gain as frequency is raised, a condition caused by the necessity to limit bandwidth internally to preserve stability in the A1, modulator, input demodulator loop. The input stage contains most of the small signal bandwidth limitations thus, taking input gain limits small signal bandwidth (see Figure 10). The demodulators limit slew rate and large signal bandwidth. Apparent slew rate at the isolator output is

multiplied by gain taken in the output stage. With maximum gain taken in the output stage, large signal bandwidth for moderate swings approaches small signal bandwidth (shown in Figure 10). Thus applying input gain, limits bandwidth while output gain enhances it.

FILTRATION

With the AD293/AD294, the addition of filtration can be implemented in a number of different configurations without the use of external operational amplifiers. Capacitors can be placed in series with the input or output terminals or configured in combination with the gain setting resistors to tailor performance. An input filter terminal and an output filter terminal are provided for user selectable filtration. Characteristics are determined by the formulas shown in Figure 1.

REDUCING NORMAL MODE VOLTAGE

A prime isolator function is the rejection of common mode signals. The extremely high input to output resistance of isolators allows excellent rejection of dc common mode voltages. As frequency rises, the small capacitance across the isolation barrier causes an ac common mode current to flow through that barrier, which is proportional to applied common mode voltage, frequency and barrier capacitance. Since the isolation mechanism (transformer T1) is more initimately connected to the input low terminal than the input high terminal, the bulk of common mode current flows through the input low terminal. Any resistance in series with the input source and the input low terminal then develops a normal mode voltage, which may constitute objectionable interference.

An isolator cannot separate normal mode interference from the desired signal without help, but interference can be rejected in several ways.

Conversion of common mode current to normal mode voltage can be reduced by minimizing resistance in the input low lead. In the AD293/AD294 CMR is enhanced and input trimming sacrificed by returning the input signal to pin 2. With known stable source resistances common mode current to normal mode voltage conversion can also be cancelled as shown in Figure 13.

ISOLATED INDUSTRIAL APPLICATIONS

As illustrated in Figure 14, the AD293 can be applied where differential signal sources are used such as an isolated strain gauge. With a third wire connected to the common mode potential of that source, a common mode current is forced to flow thorough the third wire and through the isolation barrier; thus, sparing the differential input wires the necessity of conducting the common mode current. In this manner, the isolator is responsive to only the differential inputs while ignoring the passage of common mode currents. Input gain is selected via R_G and determined by the input gain formula.

MEDICAL APPLICATIONS

In medical applications, a good connection to the patient, even on the third wire cannot be guaranteed due to electrode resistance to and through the skin. Illustrated in Figure 12 is a medical front end with right leg drive powered by the AD294A. Here the common mode drive amplifier helps force common mode current to flow in the third wire in preference to the differential input wires. The FET input has low noise current to avoid development of voltage noise in the input protection resistors. These resistors protect the input from defibrillator pulses with the AD294A having the capability of withstanding an 8kV pulse. The patient is also protected from fault currents due to input component failure. It is necessary to connect the third wire to establish the input common mode level. If not connected the input common mode level, with respect to common of the input section power supplies, will cause the isolator to drift out of its linear range. Layout is also very important, both for common mode rejection and isolation.

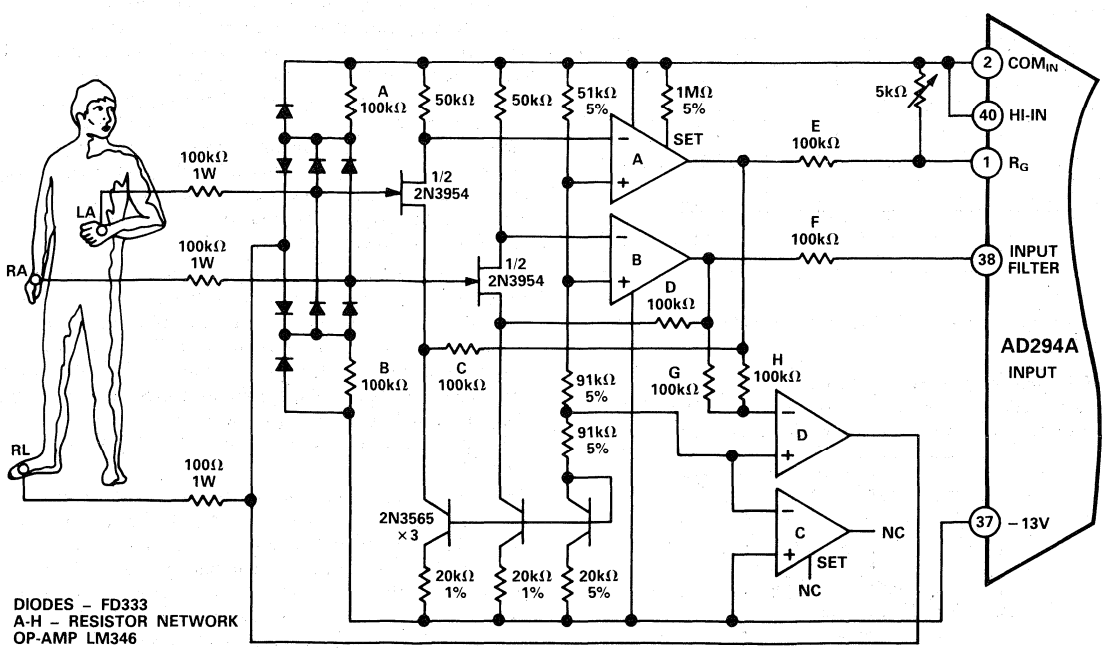


Figure 12. Multilead Medical Application Using the AD294A with Right Leg Drive

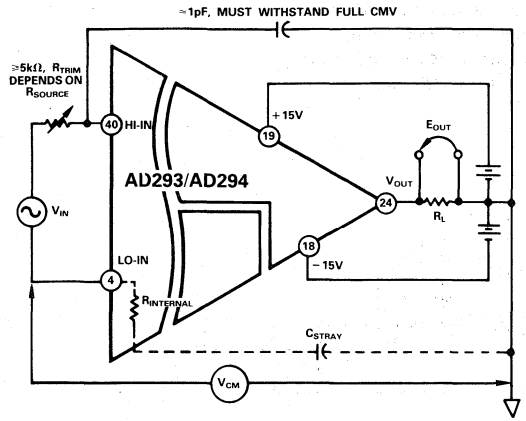


Figure 13. Improving CMR by Cancellation

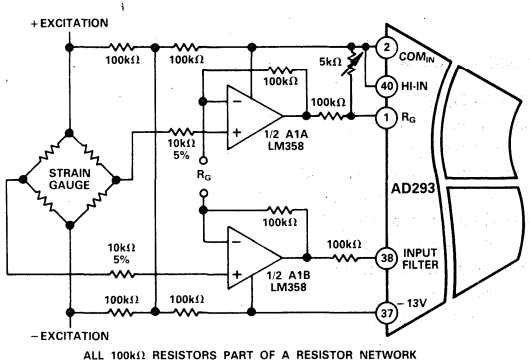


Figure 14. Isolated Strain Gauge Using Front End of AD293

CURRENT LOOP INTERFACE

Illustrated in Figure 15, the AD293 provides an isolated sensor interface that is compatible with standard 4-to-20mA current loops. Here high common mode rejection and high common mode voltage suppression are easily attained with the AD293. The AD293 conditions the 0V to 10V input signal and provides a proportional voltage at the isolator's output. Then the circuitry shown converts it into a 4 to 20mA current, which in turn, may be applied to the loop load R_L.

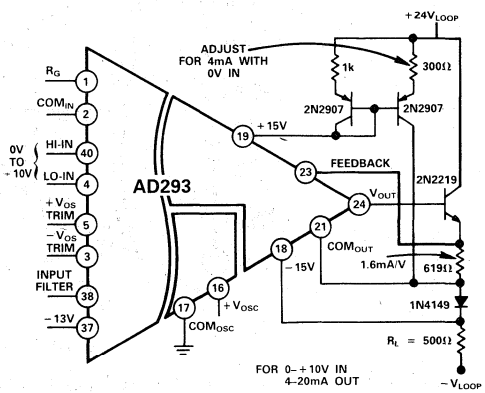


Figure 15. Isolated Current Loop Interface

TEMPERATURE MEASUREMENT AND COLD JUNCTION COMPENSATION

Illustrated in Figure 16, the AD293 can be used for isolated temperature measurements while providing cold junction compensation. With the circuitry connected as shown, the LM334 must be thermally connected to the cold junction terminal for an accurate temperature measurement to be made of this terminal. The 500Ω potentiometer will set the gain accuracy while the 100Ω potentiometer establishes offset trimming. Using this configuration, accurate temperature measurements of the industry's popular J type thermocouple can be made with the AD293 providing the added isolation feature. Gain and filtration can be addressed as required.

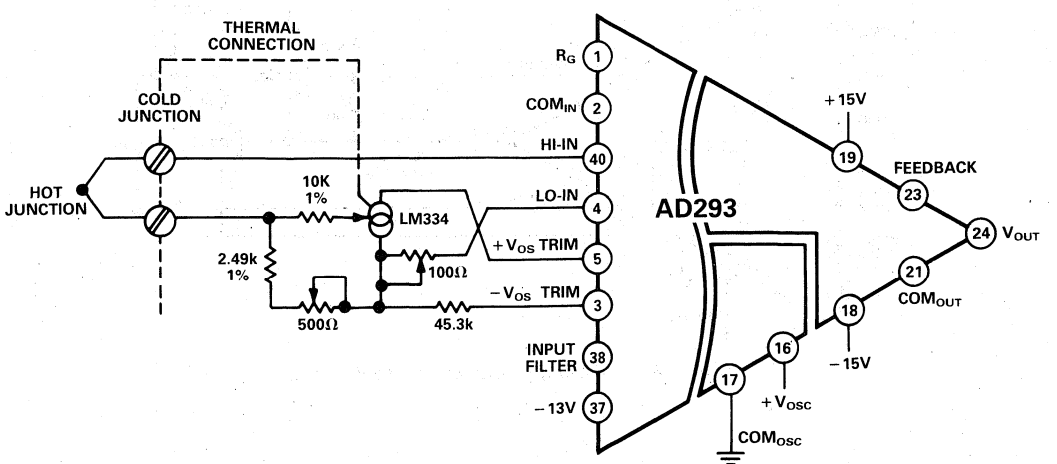


Figure 16. Temperature Measurement & Cold Junction Compensation

DRIVING CAPACITIVE LOADS

For driving capactive loads greater than 1000pF, compensation should be implemented as shown in Figure 17. Here a 100pF capacitor and 100Ω resistor are used to insure that the AD293 output stage remains stable. These components can also be changed to tailor frequency response to the particular application. The 100Ω resistor isolates the output of the AD293 while the 100pF provides response lead.

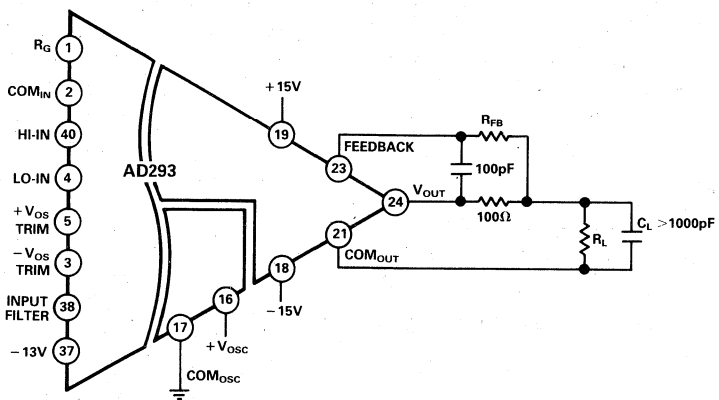


Figure 17. Driving Capacitive Loads

INCREASING OUTPUT DRIVE CAPABILITY

For applications requiring increased output drive, Figure 18 illustrates a single solution. Here the output voltage of the AD293 is conditioned and applied to the drive circuitry. R_A will supply the output stage with unity gain as connected. For gain to be added to the output stage, connect R_B as shown. Output gain will be determined by the output equation previously stated in the specifications. R_O and C_O should also be implemented so output stability will be insured. With this output drive circuitry, 200Ω loads can be easily driven with ±10V @ 50mA.

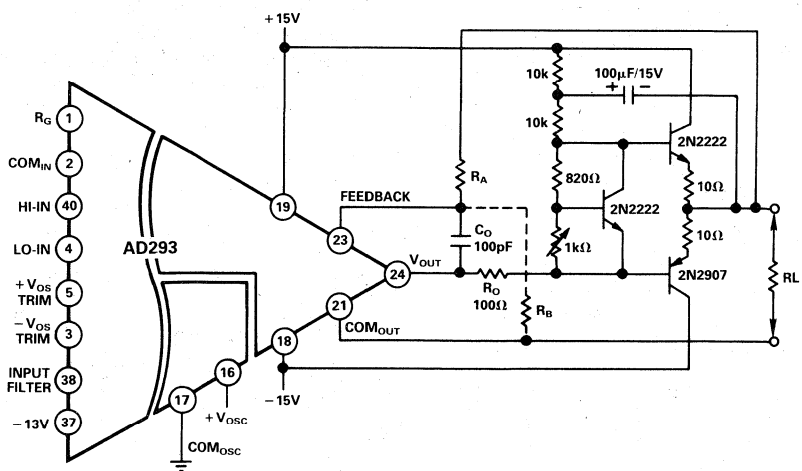


Figure 18. Increasing Output Drive Capability

ANALOG DEVICES

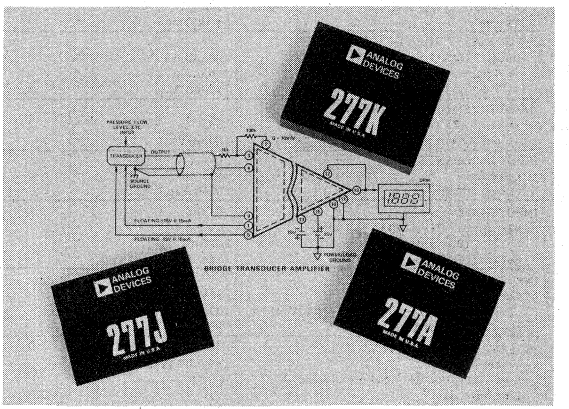
Precision Isolation Amplifier
High CMV/CMR, ±15V Floating Power
MODEL 277

FEATURES

Versatile Op Amp Front End: Inverting, Non-Inverting, Differential Applications
Low Nonlinearity: 0.025% max, Model 277K
Low Input Offset Voltage Drift: 1μV/°C max, Model 277K
Floating Power Supply: ±15V dc @ ±15mA
High CMR: 160dB min @ dc
High CMV: 3500V_{rms}

APPLICATIONS

Programmable Gain Isolated Amplifier
Isolated Power Source and Amplifier for Bridge Measurements
Instrumentation Amplifier
Instrumentation Grade Process Signal Isolator
Current Shunt Measurements



GENERAL DESCRIPTION

Model 277 is a versatile isolation amplifier which combines a high-performance, uncommitted operational amplifier front end with a precision, isolated output stage and a floating power supply section. This configuration, shown in Figure 1, makes the 277 ideally suited to instrumentation applications where the need for various forms of signal conditioning, high CMV protection and isolated transducer power requirements are encountered.

The input stage is a low drift (±1μV/°C max, model 277K) differential op amp that may be connected for use in inverting, non-inverting and differential configurations. The circuitry employed around the operational amplifier input stage can be designed by the user to suit each application's particular signal processing needs. A full ±10V signal range is available at the output of the front end amplifier.

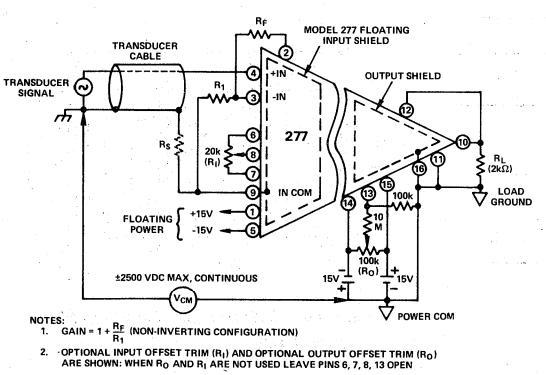


Figure 1. Transducer, Power, Gain Resistors, and Shielding Interconnection

The isolated output stage includes a special modulator/demodulator technique which provides the 277 with 160dB minimum dc common mode rejection between input and output common and an input-to-output CMV rating of 3500V_{rms}. When combined with the output stage's low nonlinearity (0.05%, models 277J/A and 0.025% model 277K), these high CMR and CMV ratings facilitate accurate measurements in the presence of noisy electrical equipment such as motors and relays. In addition, model 277A offers a -25°C to +85°C rated operating temperature range. All versions of model 277 have a ±10 volt output range.

The floating power supply section provides isolated ±15 volt outputs capable of delivering currents up to ±15mA. This feature permits model 277 to power transducers and auxiliary isolated circuitry, thereby eliminating the need for a separate isolated dc/dc converter.

All of the features of the model 277 isolation amplifier are packaged in a compact (3″ x 2.2″ x 0.59″) module. As an assurance of high performance reliability, every model 277 is factory tested for CMV rating by application of 3500V_{rms} (±4900V peak) between input and output common terminals for one minute (meets NEMA and CSA requirements for 660V_{rms} service.) In addition, the 277 has a calculated MTBF of 133,000 hours.

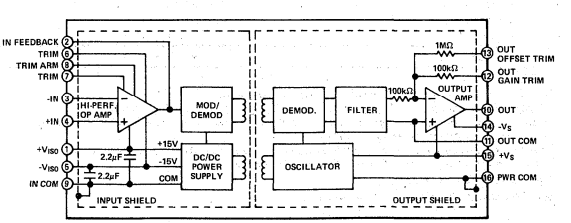


Figure 2. Model 277 Functional Block Diagram

For detailed information, contact factory.

SPECIFICATIONS (typical at +25°C and ±15V unless otherwise noted)

MODEL	277J	277K	277A
INPUT STAGE PERFORMANCE[1,2]			
OPEN LOOP GAIN	106dB min	*	*
INPUT OFFSET VOLTAGE			
Initial, @ +25°C (Adjustable to Zero)	±1.5mV max	*	*
vs. Temperature			
Offset Untrimmed	±5μV/°C max	*	±5μV/°C
Offset Trimmed to Zero	±3μV/°C max	±1μV/°C max	*
vs. Supply Voltage	±30μV/V	*	*
vs. Time	±3.5μV/mo	*	*
INPUT BIAS CURRENT			
Initial, @ +25°C	±20nA max	*	*
vs. Temperature	±50pA/°C	*	*
vs. Supply Voltage	±100pA/V	*	*
INPUT DIFFERENCE CURRENT			
Initial, @ +25°C	±6nA	*	*
vs. Supply Voltage	±50pA/V	*	*
INPUT IMPEDANCE			
Differential	4MΩ	*	*
Common Mode[3]	100MΩ||4pF	*	*
INPUT NOISE			
Voltage, 0.01Hz to 10Hz	1μV p-p	*	*
10Hz to 1kHz	3μV rms	*	*
Current, 0.01Hz to 10Hz	35pA p-p	*	*
INPUT VOLTAGE RANGE			
Common Mode Voltage[3]	±10V min	*	*
Common Mode Rejection[3], CMV = ±10V, 60Hz	100dB	*	*
Max Safe Differential Voltage	±13V	*	*
ISOLATED POWER SUPPLY[4]			
Voltage/Current[2]	±15V @ ±15mA max	*	*
Load Regulation (No Load – Full Load)	+0, -6%	*	*
Line Regulation	1V/V	*	*
Ripple, Full Load	30mV p-p @ 70kHz	*	*
OUTPUT STAGE PERFORMANCE			
GAIN	1V/V	*	*
Gain Error	±0.5% max	*	*
vs. Temperature	±50ppm/°C max	*	*
Nonlinearity, ±10V Output	±0.05% max	±0.025% max	*
VOLTAGE RATINGS[5]			
Max CMV, Output Com/Input Com			
ac, 60Hz, 1 Minute	$3500V_{rms}$ max	*	*
Nonrecurring Spike (<1 Second)	±5000V pk max	*	*
Peak ac or dc, Continuous	±2500V max	*	*
CMR, Output Com/Input Com[5]			
dc	160dB min	*	*
60Hz	120dB min	*	*
Leak. Cur., Input/output $115V_{rms}$, 60Hz	1μA rms max	*	*
ISOLATION IMPEDANCE[5]			
Input Com/Output Com	$10^{12}Ω$||16pF	*	*
OUTPUT OFFSET VOLTAGE			
Initial, @ +25°C (Adjustable to Zero)	±10mV max	*	*
vs. Temperature	±100μV/°C max	±50μV/°C max	±100μV/° C max
vs. Supply Voltage	±1mV/V	*	*
vs. Time	±100μV/mo	*	*
FREQUENCY RESPONSE			
Small Signal, -3dB	2.5kHz	*	*
Full Power, 20V p-p Output	1.5kHz	*	*
Settling Time ±10V Step to 0.1%	1ms	*	*
RATED OUTPUT			
. Voltage/Current	±10V min @ ±5mA min	*	*
OUTPUT NOISE			
Voltage, 0.01Hz to 10Hz	7μV p-p	*	*
10Hz to 1kHz	25μV rms	*	*
POWER SUPPLY[6]			
Voltage, Rated Performance	±15V dc	*	*
Voltage, Operating	±(14 to 16)V dc	*	*
Current, Quiescent	+35, -5mA	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	-25°C to +85°C
Operating	-25°C to +85°C	*	*
Storage	-55°C to +85°C	*	*
CASE SIZE	3.0" x 2.2" x 0.59"	*	*

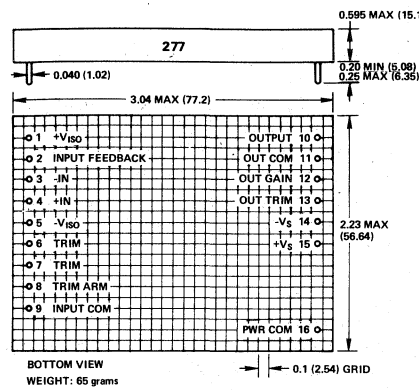
NOTES:
[1] Current drawn from INPUT FEEDBACK terminal must be ≤5mA.
[2] Total current drawn from IN FEEDBACK and either $+V_{ISO}$ or $-V_{ISO}$ must be ≤15mA.
[3] Input common mode specifications are measured at +IN and -IN terminals with respect to INPUT COM.
[4] Protected for momentary shorts to IN COM.
[5] Isolation specifications are measured at INPUT COM with respect to OUT COM and PWR COM.
[6] Recommended power supply, ADI model 904, ±15V @ ±50mA.

*Specifications same as model 277J.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)



MATING SOCKET – AC1053

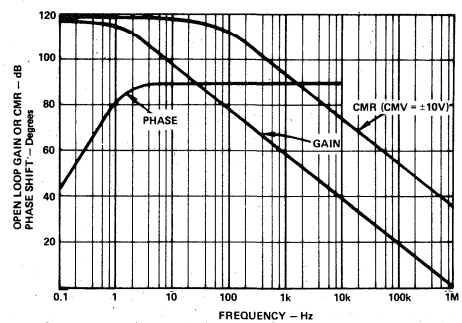


Figure 3. Input Stage Gain, CMR and Phase vs. Frequency

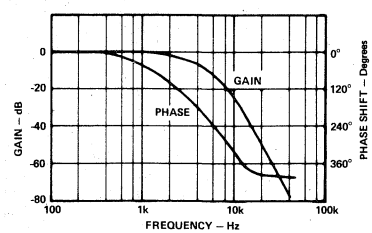


Figure 4. Output Stage Gain and Phase vs. Frequency

ANALOG DEVICES

High CMV, High Performance Isolation Amplifiers

MODELS 284J, 286J, 281

FEATURES

- High CMV Isolation: ±5000V pk, 10ms Pulse; ±2500V dc Continuous
- High CMR: 110dB min with 5kΩ Imbalance
- Low Nonlinearity: 0.05% @ 10V pk-pk Output
- High Gain Stability: ±0.0075%/°C, ±0.001%/1000 hours
- Low Input Offset Voltage Drift: 10μV/°C, G = 100V/V (Model 286J)
- Resistor Programmed Gain: 1 to 10V/V (284J) 1 to 100V/V (286J)
- Isolated Power Supply: ±8.5V dc @ ±5mA (284J) ±15V dc @ ±15mA (286J)
- Meets IEEE Std 472: Transient Protection (SWC)
- Meets UL Std 544 Leakage @ 115V ac, 60Hz: 2.0μA max (284J) 2.5μA max (286J)

APPLICATIONS

- Fetal Heartbeat Monitoring
- Multi-Channel ECG Recording
- Ground Loop Elimination in Industrial and Process Control
- High Voltage Protection in Data Acquisition Systems
- 4-20mA Isolated Current Loop Receiver

GENERAL DESCRIPTION

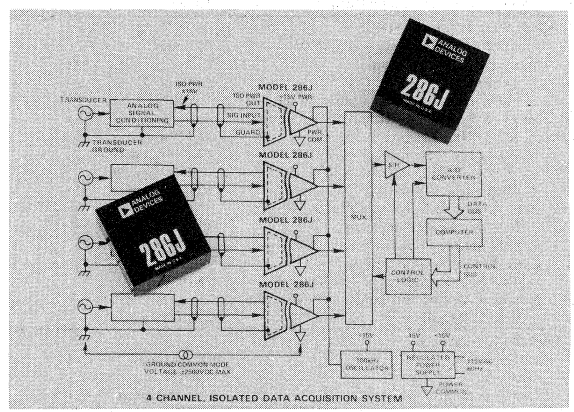
The models 284J, 286J are low cost, high performance isolation amplifiers designed for high CMV isolation and low leakage in biomedical, industrial and data acquisition systems. Using modulation techniques with reliable transformer isolation, the models 284J, 286J protect both patients and ultra-sensitive equipment from high CMV transients up to ±5000V pk (10ms pulse) or 2500V dc continuous, high CMR of 110dB (5kΩ imbalance) and feature maximum leakage current of less than 3μA rms, @ 115V ac, 60Hz (inputs to power common).

The model 284J is a self-contained isolation amplifier for single channel applications. For multi-channel applications, the model 286J combined with an external synchronizing oscillator such as the model 281 may be used; up to 16 model 286J amplifiers can be driven from 1 model 281 oscillator. Additional channels may be obtained by configuring an unlimited number of 284Js with several ganged 281 oscillators.

Both models also provide resistor-programmable gain of 1 to 10V/V (284J) or 1 to 100V/V (286J), high gain stability of 0.0075%/°C, low nonlinearity of 0.05% @ 10V pk-pk output and isolated power supply outputs of ±15V dc @ ±15mA (286J) or ±8.5V dc @ ±5mA (284J).

WHERE TO USE MODELS 284J, 286J

Industrial Applications: In data acquisition systems, computer interface systems, process signal isolators and high CMV instrumentation, models 284J, 286J offer complete galvanic isolation and protection against damage from transients and fault voltages. High level transducer interface capability is afforded



4 CHANNEL ISOLATED DATA ACQUISITION SYSTEM

with model 286J's 20V pk-pk or model 284J's 10V pk-pk input signal range at a gain of 1V/V operation. In portable field designs, single supply, wide range operation (+8V to +16V) offers simple battery operation.

Medical Applications: In biomedical and patient monitoring equipment such as multi-channel VCG, ECG, and polygraph recorders, models 284J, 286J offer protection from lethal ground fault currents as well as 5kV defibrillator pulse inputs. Low level bioelectric signal recording is achieved with low input noise (8μV pk-pk @ G = max gain) and high CMR (110dB, min @ 60Hz).

DESIGN FEATURES AND USER BENEFITS

High Reliability: Models 284J, 286J are conservatively designed, compact modules, capable of reliable operation in harsh environments. Models 284J, 286J have calculated MTBF of over 390,000 hours and are designed to meet MIL-STD-202E environmental testing as well as the IEEE Standard for Transient Voltage Protection (472-1974: Surge Withstand Capability). As an additional assurance of reliability, every model 284J and 286J is factory tested for CMV and input ratings by application of 5kV pk, 10ms pulses, between input terminals as well as input/output terminals.

Isolated Power Supply: Dual regulated supplies, completely isolated from the input power terminals (±2500V dc isolation), provides the capability to excite floating signal conditioners, front end buffer amplifiers as well as remote transducers such as thermistors or bridges.

Adjustable Gain: A single external resistor enables gain adjustment from 1V/V to 100V/V (286J) or 1V/V to 10V/V (284J) providing the flexibility of applying models 284J, 286J in both high-level transducer interfacing as well as low-level sensor measurements.

For detailed information, contact factory.

SPECIFICATIONS (typical @ +25°C and V_S = +15V dc unless otherwise noted)

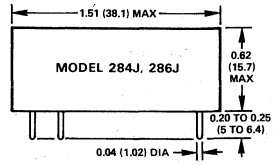
MODEL	284J	286J[1]
GAIN (NON-INVERTING)		
Range (50kΩ Load)	1 to 10V/V	1 to 100V/V
Formula	$\text{Gain} = [1 + \frac{100k\Omega}{10.7k\Omega + R_j(k\Omega)}]$	$\text{Gain} = [1 + \frac{100k\Omega}{1k\Omega + R_j(k\Omega)}]$
Deviation from Formula	±3%	±4%
vs. Time	±0.001%/1000 Hours	*
vs. Temperature (0 to +70°C)[2]	±0.0075%/°C	*
Nonlinearity, 10V pk-pk Output[2]	±0.05%	*
INPUT VOLTAGE RATINGS		
Linear Differential Range, G = 1V/V	±5V min	±10V min
Max Safe Differential Input		
Continuous	$240V_{rms}$	*
Pulse, 10ms duration, 1 pulse/10 sec	$\pm 6500V_{pk}$ max	*
Max CMV, Inputs to Outputs		
AC, 60Hz, 1 minute duration	$2500V_{rms}$	*
Pulse, 10ms duration, 1 pulse/10 sec	$\pm 2500V_{pk}$ max	*
With 510kΩ in series with Guard	$\pm 5000V_{pk}$ max	*
Continuous, AC or DC	$\pm 2500V_{pk}$ max	*
CMR, Inputs to Outputs, 60Hz, $R_S \leq 5k\Omega$		
Balanced Source Impedance	114dB	*
5kΩ Source Impedance Imbalance	110dB min	*
CMR, Inputs to Guard, 60Hz		
1kΩ Source Impedance Imbalance	78dB	*
Max Leakage Current, Inputs to Power Common		
@ 115VAC, 60Hz	2.0μA rms max	2.5μA rms max
INPUT IMPEDANCE		
Differential	$10^8\ \Omega \| 70pF$	$10^8\ \Omega \| 150pF$
Overload	$10^8\ \Omega$	*
Common Mode	$5 \times 10^{10}\ \Omega \| 20pF$	*
INPUT DIFFERENCE CURRENT		
Initial, @ +25°C	±7nA max	*
vs. Temperature (0 to +70°C)	±0.1nA/°C	*
INPUT NOISE		
Voltage[3]		
0.05Hz to 100Hz	8μV pk-pk	*
10Hz to 1kHz	10μV rms	3μV rms
Current		
0.05Hz to 100Hz	5pA pk-pk	*
FREQUENCY RESPONSE		
Small Signal, -3dB	1kHz	*
Slew Rate	25mV/μs	*
Full Power, 10V p-p Output	200Hz	900Hz
Full Power, 20V p-p Output	N/A	400Hz
Recovery Time, to ±100μV after Application of $\pm 6500V_{pk}$ Differential Input Pulse	200ms	*
OFFSET VOLTAGE REFERRED TO INPUT		
Initial, @ +25°C, Adjustable to Zero	±(5 + 20/G)mV	±(5 + 45/G)mV
vs. Temperature (0 to +70°C)	±(1 + 150/G)μV/°C	±(7 + 250/G)μV/°C
vs. Supply Voltage	±1mV/%	*
RATED OUTPUT		
Voltage, 50kΩ Load	±5V min	±10V min
Output Impedance	1kΩ	*
Output Ripple, 1MHz Bandwidth	5mV pk-pk	20mV pk-pk
ISOLATED POWER OUTPUTS		
Voltage, ±5mA Load	±8.5V dc	±15V dc
Accuracy	±5%	0, -6%
Current	±5mA min	±15mA min
Regulation, No Load to Full Load	+0, -15%	+0, -10%
Ripple, 100kHz Bandwidth	100mV pk-pk	200mV pk-pk
POWER SUPPLY, SINGLE POLARITY[4]		
Voltage, Rated Performance	+15V dc	*
Voltage Operating	+(8 to 15.5)V dc	*
Current, Quiescent	+10mA	+13mA
TEMPERATURE RANGE		
Rated Performance	0 to +70°C	*
Operating	-25°C to +85°C	*
Storage	-55°C to +85°C	*
CASE DIMENSIONS[5]	1.5" x 1.5" x 0.62"	*

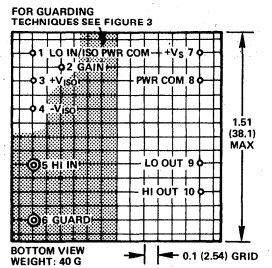
NOTES
*Specifications same as model 284J.
[1] Specifications for model 286J apply when driven by ADI model 281 oscillator.
[2] Gain temperature drift and gain nonlinearity are specified as a percentage of output signal level.
[3] Model 284J: Gain = 10V/V; Model 286J: Gain = 100V/V.
[4] Recommended power supply, ADI model 904, ±15V @ 50mA.
[5] Recommended mounting sockets – model 284J: ADI Part Number AC1049; model 286J: ADI Part Number AC1054.

Specifications subject to change without notice.

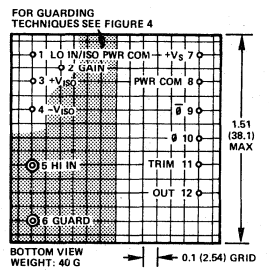
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).





Model 284J



Model 286J

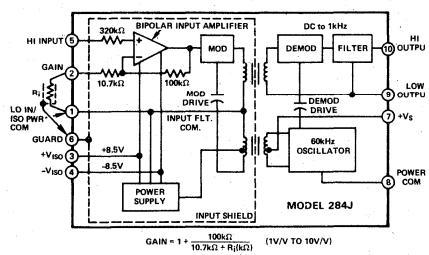


Figure 1. Block Diagram – Model 284J

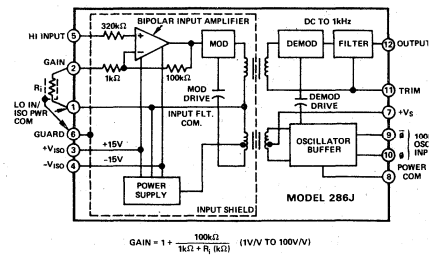
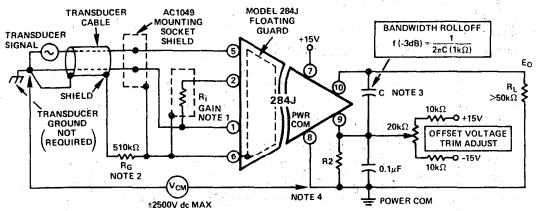


Figure 2. Block Diagram – Model 286J

INTERCONNECTION AND GUARDING TECHNIQUES

Models 284J, 286J can be applied directly to achieve rated performance as shown in Figures 3 and 4. To preserve the high



NOTE 1. GAIN RESISTOR, R_I, 1%, 50ppm/°C METAL FILM TYPE IS RECOMMENDED.
FOR GAIN = 1V/V, LEAVE TERMINAL 2 OPEN.
FOR GAIN = 10V/V, SHORT TERMINAL 2 TO TERMINAL 1

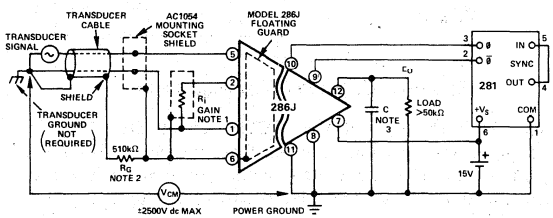
$$\text{GAIN} = 1 + \frac{100k\Omega}{10.7k\Omega + R_I(k\Omega)}$$

NOTE 2. GUARD RESISTOR, R_G, REQUIRED ONLY FOR CMV > ±2500V_{PK} (±5kV_{PK} MAX).
R_G MAY BE MOUNTED ON AC1049 MOUNTING SOCKET USING STANDOFF PROVIDED.
(USE ¼ WATT, 5%, CARBON COMPOSITION TYPE; ALLEN BRADLEY RECOMMENDED).

NOTE 3. OUTPUT FILTER CAPACITOR, C. SELECT TO ROLLOFF NOISE AND OUTPUT RIPPLE: (e.g. SELECT C = 1.5μF FOR dc TO 100Hz BANDWIDTH).

NOTE 4. R2 ~ 200Ω, G = 1; R2 ~ 2kΩ, G>1

Figure 3. Model 284J Basic Isolator Interconnection



NOTE 1. GAIN RESISTOR, R_I, USE 50ppm/°C, METAL FILM TYPE.
FOR GAIN = 1V/V, LEAVE TERMINAL 2 OPEN.
FOR GAIN = 100V/V, SHORT TERMINAL 2 TO TERMINAL 1
FOR GAINS FROM 1V/V TO 100V/V:

$$\text{GAIN} = 1 + \frac{100k\Omega}{1k\Omega + R_I\,(k\Omega)}$$

NOTE 2. OPTIONAL GUARD RESISTOR, R_G, REQUIRED ONLY FOR CMV > ±2500V_{PK}
R_G MAY BE CONVENIENTLY MOUNTED ON AC1054 MOUNTING SOCKET USING THE STANDOFF PROVIDED (R_G). USE 1/4 WATT, 5% CARBON COMPOSITION TYPE; (ALLEN BRADLEY RECOMMENDED).

NOTE 3. OUTPUT FILTER CAPACITOR C. SELECT TO ROLL-OFF NOISE AND OUTPUT RIPPLE: (e.g. SELECT C=1.5μF FOR dc TO 100Hz BANDWIDTH)

$$F\ (-3dB) = \frac{1}{2\pi C\,(1k\Omega)}$$

Figure 4. Model 286J Basic Isolator Interconnection

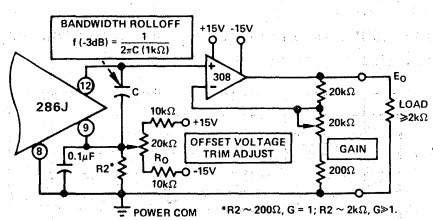


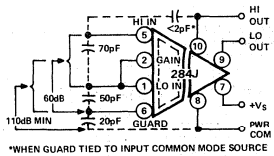
Figure 5. Model 286J Optional Connection: Offset Voltage Trim Adjust, Bandwidth (-3dB) Rolloff and Gain Adjust (G>100V/V)

CMR performance, care must be taken to keep the capacitance balanced about the input terminals. A shield should be provided on the printed circuit board under model 284J or 286J. The GUARD (Pin 6) should be connected to this shield. The guard-shield is provided with the mounting socket. To reduce effective cable capacitance, cable shield should be connected to the common mode signal source by connecting the shield as close as possible to the signal low.

Offset Voltage Trim Adjust: The trim adjust circuits shown in Figures 3 and 5 can be used to zero the output offset voltage over the specified gain range. The output terminals, HI OUT and LO OUT, can be floated with respect to PWR COM up to ±50V_{pk} max, offering three-port isolation. A 0.1μF capacitor is required from LO OUT to PWR COM whenever the output terminals are floated with respect to PWR COM. LO OUT can be connected directly to PWR COM when output offset trimming is not required.

INTERELECTRODE CAPACITANCE, TERMINAL RATINGS AND LEAKAGE CURRENTS LIMITS

Capacitance: Interelectrode terminal capacitance arising from stray coupling capacitance effects between the input terminals and the signal output terminals are each shunted by leakage resistance values exceeding 50kMΩ. Figures 6 and 8 illustrate the CMR ratings at 60Hz and 5kΩ source imbalance between signal input/output terminals, along with their respective capacitance.



*WHEN GUARD TIED TO INPUT COMMON MODE SOURCE

Figure 6. Model 284J Terminal Capacitance and CMR Ratings

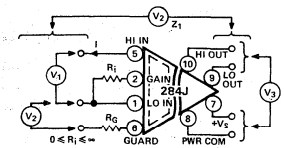
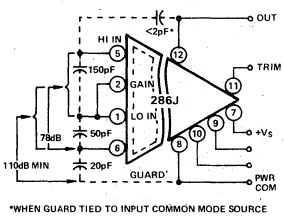


Figure 7. Model 284J Terminal Ratings



*WHEN GUARD TIED TO INPUT COMMON MODE SOURCE

Figure 8. Model 286J Terminal Capacitance and CMR Ratings

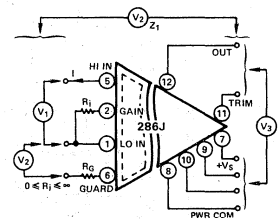


Figure 9. Model 286J Terminal Ratings

Terminal Ratings: CMV performance is given in both peak pulse and continuous ac or dc peak ratings. Pulse ratings are intended to support defibrillator and other transient voltages. Continuous peak ratings apply from dc up to the normal full power response frequencies. Figures 7 and 9 and Table 1 illustrate models 284J, 286J ratings between terminals.

SYMBOL	RATING	REMARKS
V1 (pulse)	±6500V_{PK} (10ms)	Withstand Voltage, Defibrillator
V1 (cont.)	±240V_{RMS}	Withstand Voltage, Steady State
V2 (pulse)	±2500V_{PK} (10ms) R_G = 0	Transient
V2 (pulse)	±5000V_{PK} (10ms) R_G = 510kΩ	Isolation, Defibrillator
V2 (cont.)	±2500V_{PK}	Isolation, Steady State
V3 (cont.)	±50V_{PK}	Isolation, dc
Z1	50kMΩ‖20pF	Isolation Impedance
I (286J)	50μA rms	Input Fault Limit, dc to 200kHz
I (284J	35μA rms	Input Fault Limit, dc to 60kHz

Table 1. Isolation Ratings Between Terminals

Leakage Current Limits: The low coupling capacitance between inputs and output yields a ground leakage current of less than 2.0μA rms (284J) and 2.5μA rms (286J) at 115V ac, 60Hz (or 0.02μA/V ac). As shown in Figures 10 and 11, the transformer coupled modulator signal, through stray coupling, also creates an internally generated leakage current. Line frequency leakage current levels are unaffected by the power on or off condition of models 284J, 286J.

For medical applications, models 284Jand 286J are designed to improve on patient safety current limits proposed by F.D.A., U.L., A.A.M.I. and other regulatory agencies (e.g., model 286J complies with leakage requirements for the Underwriters Laboratory STANDARD FOR SAFETY, MEDICAL AND DENTAL EQUIPMENT as established under UL544 for type A and B patient connected equipment – reference *Leakage Current,* paragraph 27.5).

In patient monitoring equipment, such as ECG recorders, models 284J, 286J will provide adequate isolation without exposing the patient to potentially lethal microshock hazards. Using passive components for input protection, this design limits input fault currents even under amplifier failure conditions.

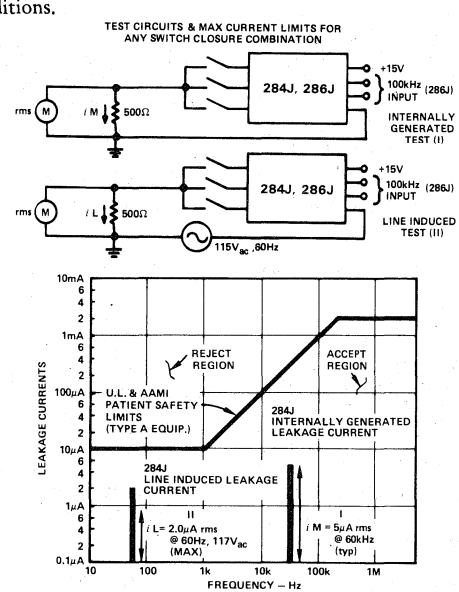


Figure10. Model 284J Leakage Current Performance from Line Induced and Internally Generated (Modulator) Operating Conditions

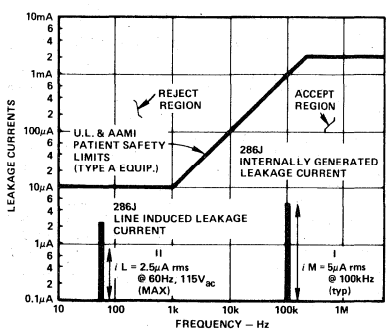


Figure 11. Model 286J Leakage Current Performance from Line Induced and Internally Generated (Modulator) Operating Conditions

GAIN AND OFFSET TRIM PROCEDURE, MODEL 284J

1. Apply e_{IN} = 0 volts and adjust R_O for e_O = 0 volts.
2. Apply e_{IN} = +1.000V dc and adjust R_G for e_O = +5.000V dc.
3. Apply e_{IN} = –1.000V dc and measure the output error (see curve a).
4. Adjust R_G until the output error is one half that measured in step 3 (see curve b).
5. Apply e_{IN} = +1.000V dc and adjust R_O until the output error is one half that measured in step 4 (see curve c).

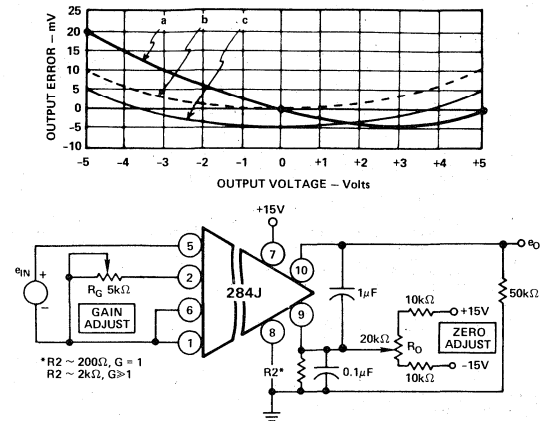


Figure 12. Gain and Offset Adjustment

GAIN AND OFFSET TRIM PROCEDURE, MODEL 286J

In applying the isolation amplifier, highest accuracy is achieved by adjustment of gain and offset voltage to minimize the peak error encountered over the selected output voltage span. The following procedure illustrates a calibration technique which can be used to minimize output error. In this example, the output span is +5V to –5V and operation at Gain = 10V/V is desired.

1. Apply e_{IN} = 0 volts and adjust R_O for e_O = 0 volts.
2. Apply e_{IN} = +0.500V dc and adjust R_G for e_O = +5.000V dc.
3. Apply e_{IN} = –0.500V dc and measure the output error (see curve a).
4. Adjust R_G until the output error is one half that measured in step 3 (see curve b).
5. Apply +0.500V dc and adjust R_O until the output error is one half that measured in step 4 (see curve c).

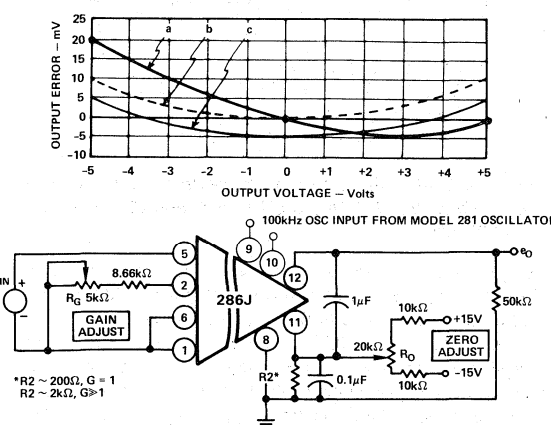


Figure 13. Gain and Offset Adjustment

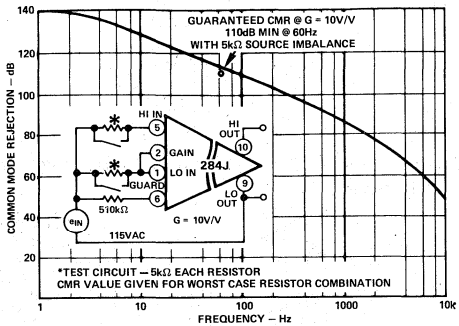


Figure 14. Model 284J Common Mode Rejection vs. Frequency

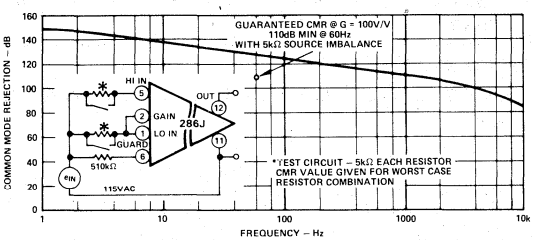


Figure 15. Model 286J Common Mode Rejection vs. Frequency

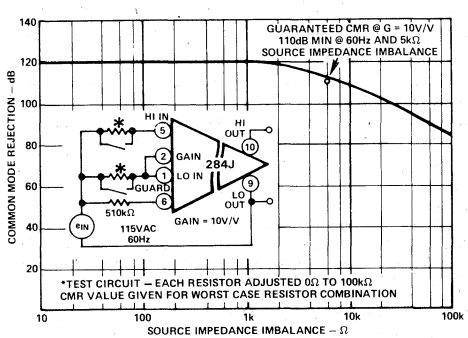


Figure 16. Model 284J Common Mode Rejection vs. Source Impedance Imbalance

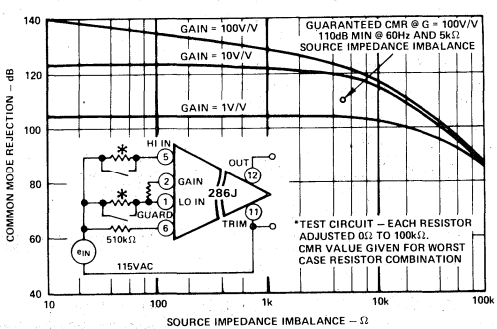


Figure 17. Model 286J Common Mode Rejection vs. Source Impedance Imbalance

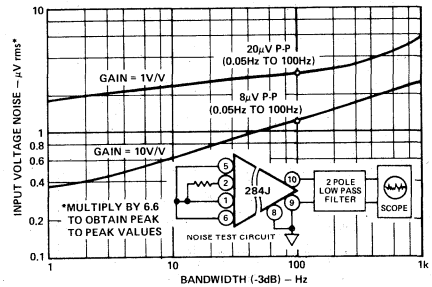


Figure 18. Model 284J Input Voltage Noise vs. Bandwidth

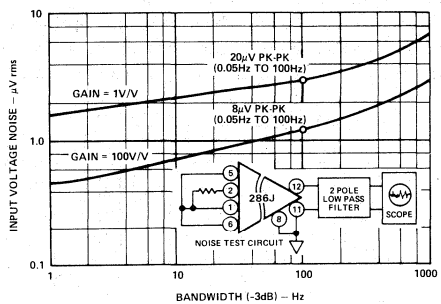


Figure 19. Model 286J Input Voltage Noise vs. Bandwidth

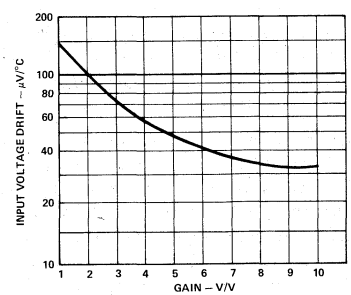


Figure 20. Model 284J Input Offset Voltage Drift vs. Gain

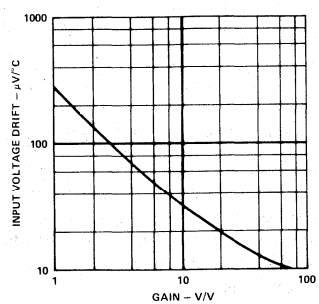


Figure 21. Model 286J Input Offset Voltage Drift vs. Gain

Applying the Multi-Channel Isolation Amplifier

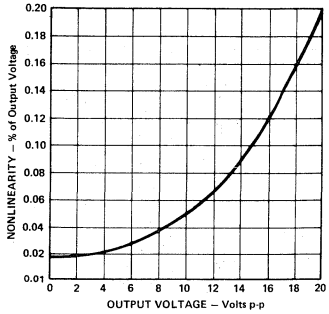
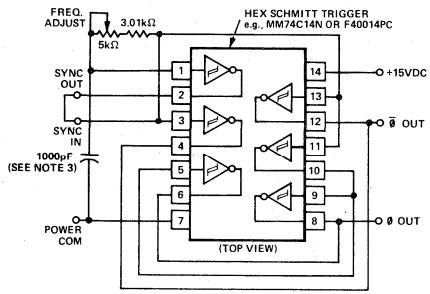


Figure 22. Model 286J Gain Nonlinearity vs. Output Voltage

REFERENCE EXCITATION OSCILLATOR*

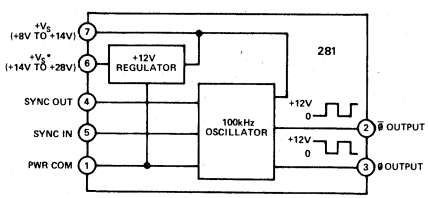
When applying model 286J, the user has the option of building a low cost 100kHz excitation oscillator, as shown in Figure 23, or purchasing a module from Analog Devices – model 281.



NOTES:
1. FREQ. ADJUST: ADJUST TRIM POT FOR OUTPUT FREQUENCY OF 100kHz ±5%.
2. FOR SLAVE OPERATION, REMOVE JUMPER FROM SYNC OUT AND SYNC IN PINS.
3. USE CERAMIC CAPACITOR, "COG" OR "NPO" CHARACTERISTIC.

Figure 23. Model 281 100kHz Oscillator – Logic and Interconnection Diagram

The block diagram of model 281 is shown in Figure 24. An internal +12V dc regulator is provided to permit the user the option of operating over two, pin selectable, power input ranges; terminal 6 offers a range of +14V dc to +28V dc; terminal 7 offers an input range of +8V dc to +14V dc.



*LEAVE TERMINAL 6 OPEN, WHEN POWER IS APPLIED TO TERMINAL 7.

Figure 24. Model 281 Block Diagram

Model 281 oscillator is capable of driving up to 16 model 286Js as shown in Figure 25. An additional model 281 may be driven in a slave-mode, as shown in Figure 26 to expand the total system channels from 16 to 32. By adding additional model 281's in this manner, systems of over 1000 channels may be easily configured.

EXTERNAL OSCILLATOR INTERCONNECTION

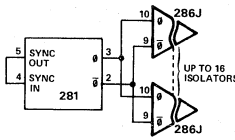


Figure 25. Model 281/286 Connection for Driving from 1 to 16 Isolators

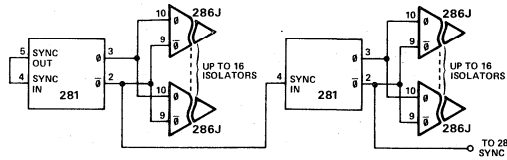


Figure 26. Model 281/286 Connection for Driving > 16 Isolators

SPECIFICATIONS

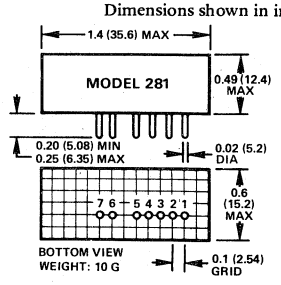
(typical @ +25° C and V_S = +15V dc unless otherwise noted)

MODEL	281*
OUTPUT	
Frequency	100kHz ±5%
Waveform	Squarewave
Voltage (ϕ and $\bar{\phi}$ terminals)	0 to +12V pk
Fan-Out[1,2]	16 max
POWER SUPPLY RANGE[3]	
High Input, Pin 6	+(14 to 28)V dc
Quiescent Current, N.L.	+5mA
F.L.	+16mA
Low Input, Pin 7	+(8 to 14)V dc
Quiescent Current, N.L.	+12mA
F.L.	+33mA
TEMPERATURE	
Rated Performance	0 to +70°C
Storage	-55°C to +85°C
MECHANICAL	
Case Size	1.4" x 0.6" x 0.49"
Weight	10 grams

[1] Model 286J oscillator drive input represents unity oscillator load.
[2] For applications requiring more than 16 286Js, additional 281s may be used in a master/slave mode. Refer to Figure 26.
[3] Full load consists of 16 model 286Js and 281 oscillator slave.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



PIN TERMINAL IDENTIFICATION

1	POWER COMMON
2	$\bar{\phi}$ OUTPUT
3	ϕ OUTPUT
4	SYNC INPUT
5	SYNC OUTPUT
6	$+V_S$: HIGH RANGE +(14 to 28)V_{dc}
7	$+V_S$: LOW RANGE +(8 to 14)V_{dc}

MATING SOCKET: Cinch #16 DIP or Equivalent

***CAUTION:**

ESD(Electro-static-discharge) sensitive device. Permanent damage may occur on unconnected devices subjected to high-energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



ANALOG DEVICES

Precision, Wide Bandwidth, Synchronized Isolation Amplifier

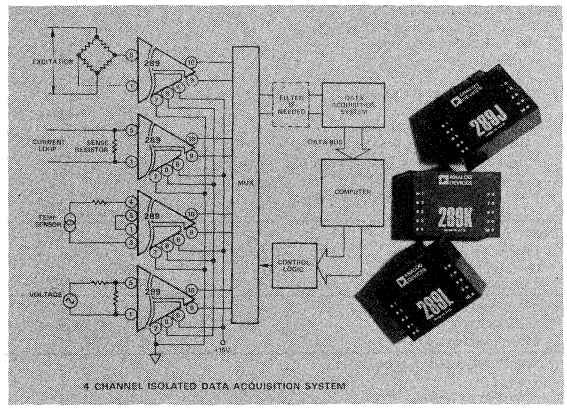
MODEL 289

FEATURES

Low Nonlinearity: ±0.012% max (289L)
Frequency Response: (-3dB) dc to 20kHz
(Full Power) dc to 5kHz
Gain Adjustable 1 to 100V/V, Single Resistor
3-Port Isolation: ±2500V CMV Isolation Input/Output
Low Gain Drift: ±0.005%/°C max
Floating Power Output: ±15V @ ±5mA
120dB CMR at 60Hz: Fully Shielded Input Stage
Meets UL Std. 544 Leakage: 2μA rms max, @ 115V ac, 60Hz

APPLICATIONS

Multi-Channel Data Acquisition Systems
Current Shunt Measurements
Process Signal Isolator
High Voltage Instrumentation Amplifier
SCR Motor Control



4 CHANNEL ISOLATED DATA ACQUISITION SYSTEM

GENERAL DESCRIPTION

Model 289 is a wideband, accurate, low cost isolation amplifier designed for instrumentation and industrial applications. Three accuracy selections are available offering guaranteed gain nonlinearity error at 10V p-p output: ±0.012% max (289L), ±0.025% max (289K), ±0.05% max (289J). All versions of the 289 provide a small signal frequency response from dc to 20kHz (-3dB) and a large signal response from dc to 5kHz (full power) at a gain of 1V/V. This new design offers true 3-port isolation, ±2500V dc between inputs and outputs (or power inputs), as well as 240V rms between power supply inputs and signal outputs. Using carrier modulation techniques with transformer isolation, model 289 interrupts ground loops and leakage paths and minimizes the effect of high voltage transients. It provides 120dB Common Mode Rejection between input and output common. The high CMV and CMR ratings of the model 289 facilitate accurate measurements in the presence of noisy electrical equipment such as motors and relays.

WHERE TO USE THE MODEL 289

The model 289 is designed to interface single and multichannel data acquisition systems with dc sensors such as thermocouples, strain gauges and other low level signals in harsh industrial environments. Providing high accuracy with complete galvanic isolation, and protection from line transients of fault voltages, model 289's performance is suitable for applications such as process controllers, current loop receivers, weighing systems, high CMV instrumentation and computer interface systems.

Use the model 289 when data must be acquired from floating transducers in computerized process control systems. The photograph above shows a typical multichannel application allowing potential differences or interrupting ground loops, among transducers, or between transducers and local ground.

DESIGN FEATURES AND USER BENEFITS

Isolated Power: The floating power supply section provides isolated ±15V outputs @ ±5mA. Isolated power is regulated to within ±5%. This feature permits model 289 to excite floating signal conditioners, front-end buffer amplifiers and remote transducers such as thermistors or bridges, eliminating the need for a separate isolated dc/dc converter.

Adjustable Gain: A single external resistor adjusts the model 289's gain from 1V/V to 100V/V for applications in high and low level transducer interfacing.

Synchronized: The model 289 provides a synchronization terminal for use in multichannel applications. Connecting the synchronization terminals of model 289s synchronizes their internal oscillators, thereby eliminating the problem of oscillator "beat frequency" interference that sometimes occurs when isolation amplifiers are closely mounted.

Internal Voltage Regulator: Improves power supply rejection and helps prevent carrier oscillator spikes from being broadcast via the isolator power terminal to the rest of the system.

Buffered Output: Prevents gain errors when an isolation amplifier is followed by a resistive load of low impedance. Model 289 can drive a 2kΩ load.

Three-Port Isolation: Provides true galvanic isolation between input, output and power supply ports. Eliminates need for power supply and output ports being returned through a common terminal.

Reliability: Model 289 is conservatively designed to be capable of reliable operation in harsh environments. Model 289 has a calculated MTBF of 271,835 hours. In addition, the model 289 meets UL Std. 544 leakage, 2μA rms @ 115V ac, 60Hz.

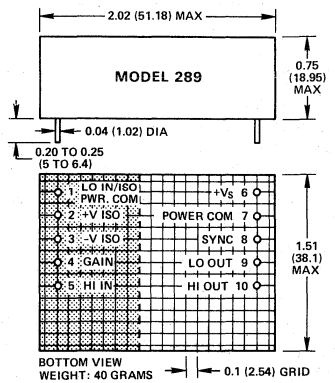
SPECIFICATIONS (typical @ +25°C and V_S = +14.4V to +25V dc unless otherwise noted)

Model	289J	289K	289L
GAIN (NONINVERTING)			
Range		1 to 100V/V	
Formula		$G = 1 + \frac{10k\Omega}{R_G(k\Omega)}$	
Deviation from Formula		±1.5% max	
vs. Temperature (0 to +70°C)[1]		15ppm/°C typ (50ppm/°C max)	
Nonlinearity, (±5V Swing)[2,3]	±0.05% max	±0.025% max	±0.012% max
INPUT VOLTAGE RATINGS			
Linear Differential Range (G = 1V/V)		±10V min	
Max Safe Differential Input			
Continuous		120V rms	
1 Minute		240V rms	
Max CMV (Inputs to Outputs)			
Continuous ac or dc		±2500V peak max	
ac, 60Hz, 1 Minute Duration		2500V rms	
CMR, Inputs to Outputs 60Hz			
$R_S \leq 1k\Omega$, Balanced Source Impedance		120dB	
$R_S \leq 1k\Omega$, HI IN Lead Only		104dB min	
Max Leakage Current, Input to Output @			
115V rms, 60Hz ac		2μA rms max	
INPUT IMPEDANCE			
Differential		$33pF \| 10^8 \Omega$	
Overload		100kΩ	
Common Mode		$20pF \| 5 \times 10^{10} \Omega$	
INPUT DIFFERENCE CURRENT			
Initial @ +25°C		10nA (75nA max)	
vs. Temperature (0 to 70°C)		0.15nA/°C	
INPUT NOISE (GAIN = 100V/V)			
Voltage			
0.05Hz to 100Hz		8μV p-p	
10Hz to 1kHz		3μV rms	
Current			
0.05Hz to 100Hz		3pA rms	
FREQUENCY RESPONSE			
Small Signal -3dB			
G = 1V/V		20kHz	
G = 100V/V		5kHz	
Full Power, 10V p-p Output			
G = 1V/V		5kHz	
G = 100V/V		3.5kHz	
Full Power, 20V p-p Output			
G = 1V/V		2.3kHz	
G = 100V/V		2.3kHz	
Slew Rate		0.14V/μs	
Settling Time[4] ±0.05%, ±10V Step		400μs	
OFFSET VOLTAGE, REFERRED TO INPUT			
Initial, @ +25°C		$\pm 5 \pm \frac{10}{G}$ mV max	
vs. Temperature (0 to +70°C)	$\pm 20 \pm \frac{200}{G}$ max	$\pm 15 \pm \frac{100}{G}$ max	$\pm 10 \pm \frac{50}{G}$ μV/°C max
vs. Supply Voltage (+15V to +20V change)		$\pm 2 \pm \frac{10}{G}$ μV/V	
RATED OUTPUT			
Voltage, 2kΩ Load		±10V min	
Output Impedance		<1Ω(dc to 100Hz)	
Output Ripple, 0.1MHz Bandwidth			
No Signal IN		5mV p-p	
$+10V_{IN}$		50mV p-p	
ISOLATED POWER SUPPLY			
Voltage		±15V dc	
Accuracy		±10%	
Current		±5mA, min	
Regulation No Load to Full Load		±5%	
Ripple, 0.1MHz Bandwidth, No Load		25mV p-p	
Full Load		75mV p-p	
POWER SUPPLY, SINGLE POLARITY[5]			
Voltage, Rated Performance		+14.4V to +25V	
Voltage, Operating		+8.5V to +25V	
Current, Quiescent (@ V_S = +15V)		+25mA	
TEMPERATURE RANGE			
Rated Performance		0 to +70°C	
Operating		-15°C to +75°C	
Storage		-55°C to +85°C	
CASE DIMENSIONS		1.5" X 2.0" X 0.75"	

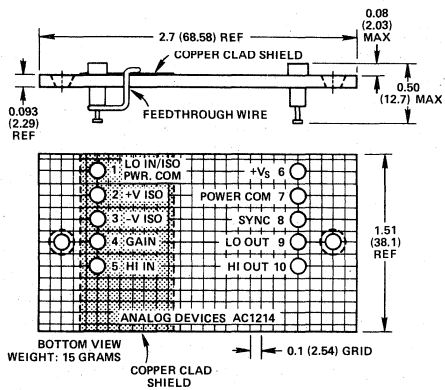
NOTES:
[1] Gain temperature drift is specified as a percentage of output signal level.
[2] Gain nonlinearity is specified as a percentage of 10V pk-pk output span.
[3] When isolated power output is used, nonlinearity increases by ±0.002%/mA of current drawn.
[4] G = 1V/V; with 2-pole, 5kHz output filter.
[5] Recommended power supply, ADI model 904, ±15V @ 50mA output.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



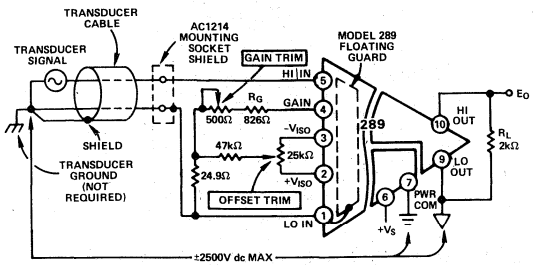
SHIELDED MATING SOCKET AC1214



INTERCONNECTIONS AND SHIELDING TECHNIQUE

To preserve the high CMR performance of model 289, care must be taken to keep the capacitance balanced about the input terminals. A shield should be provided on the printed circuit board under model 289 as illustrated in the outline drawing above (screened area). The LO IN/ISO PWR COM (pin 1) must be connected to this shield. This shield is provided with the mounting socket, model AC1214 (solder feedthrough wire to the socket pin 1 and copper foil surface). A recommended shielding technique using model AC1214 is illustrated in Figure 1.

Best CMR performance will be achieved by using twisted, shielded cable for the input signal to reduce inductive and capacitive pickup. To further reduce effective cable capacitance, the cable shield should be connected to the common mode signal source as close to signal low as possible (see Figure 1).



NOTE:
GAIN RESISTOR R_G, 1% 50ppm/°C METAL FILM TYPE IS RECOMMENDED.
FOR GAIN = 1V/V, LEAVE PIN 4 OPEN
FOR GAIN > 1V/V, CONNECT GAIN RESISTOR (R_G) BETWEEN PIN 4 AND PIN 1

$$\text{GAIN} = 1 + \frac{10k\Omega}{R_G(k\Omega)}$$

Figure 1. Basic Isolator Interconnection

THEORY OF OPERATION

The remarkable performance of the model 289 is derived from the carrier isolation technique used to transfer both signal and power between the amplifier's input stage and the rest of the circuitry. A block diagram is shown in Figure 2.

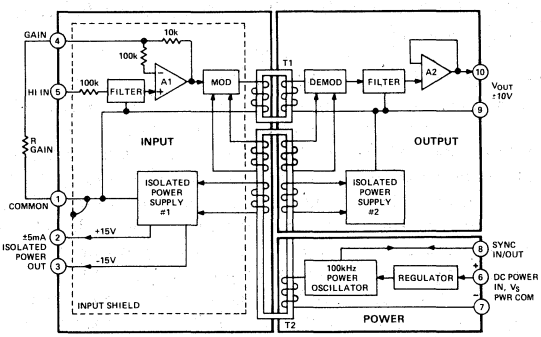


Figure 2. Model 289 Block Diagram

The input signal is filtered and appears at the input of the non-inverting amplifier, A1. This signal is amplified by A1, with its gain determined by the value of resistance connected externally between the gain terminal and the input common terminal. The output of A1 is modulated, carried across the isolation barrier by signal transformer T1, and demodulated. The demodulated voltage is filtered, amplified and buffered by amplifier A2, and applied to the output terminal. The voltage applied to the V_S terminal is set by the regulator to +12V which powers the 100kHz symmetrical square wave power oscillator. The oscillator drives the primary winding of transformer T2. The secondary windings of T2 energize both input and output power supplies, and drives both the modulator and demodulator.

INTERELECTRODE CAPACITANCE AND TERMINAL RATINGS

Capacitance: Interelectrode terminal capacitance, arising from stray coupling capacitance effects between the input terminals and the signal output terminals, are each shunted by leakage resistance values exceeding 50GΩ. Figure 3 illustrates model 289's capacitance, between terminals.

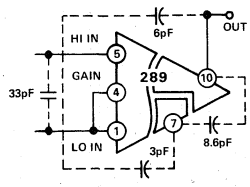


Figure 3. Model 289 Terminal Capacitance

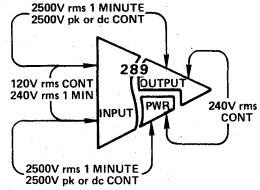


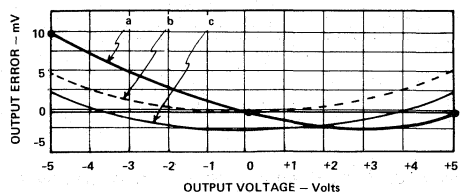
Figure 4. Model 289 Terminal Ratings

Terminal Ratings: CMV performance is given in both peak pulse and continuous ac, or dc peak ratings. Continuous peak ratings apply from dc up to the normal full power response frequencies. Figure 4 illustrates model 289 ratings between terminals.

GAIN AND OFFSET TRIM PROCEDURE

The following procedure illustrates a calibration technique which can be used to minimize output error. In this example, the output span is +5V to -5V and Gain = 10V/V.

1. Apply E_{IN} = 0 volts and adjust R_O for E_O = 0 volts.
2. Apply E_{IN} = +0.500V dc and adjust R_G for E_O = +5.000V dc.
3. Apply E_{IN} = -0.500V dc and measure the output error (see curve a).
4. Adjust R_G until the output error is one-half that measured in step 3 (see curve b).
5. Apply +0.500V dc and adjust R_O until the output error is one-half that measured in step 4 (see curve c).



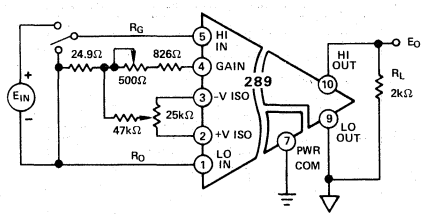


Figure 5a. Recommended Offset and Gain Adjustment for Gains > 1

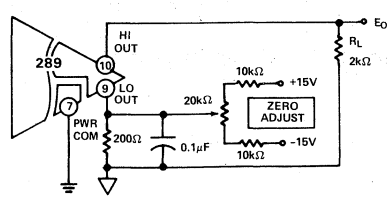


Figure 5b. Recommended Offset Adjustment for G = 1V/V

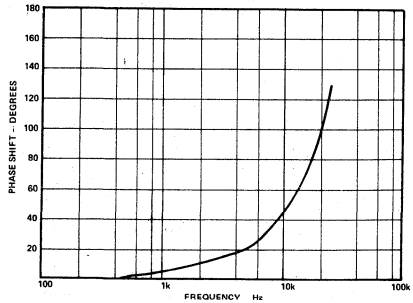


Figure 6. Typical 289 Phase vs. Frequency

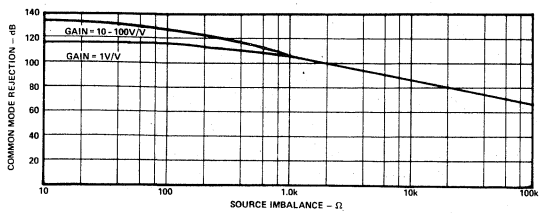


Figure 7. Typical 289 Common Mode Rejection vs. Source Impedance

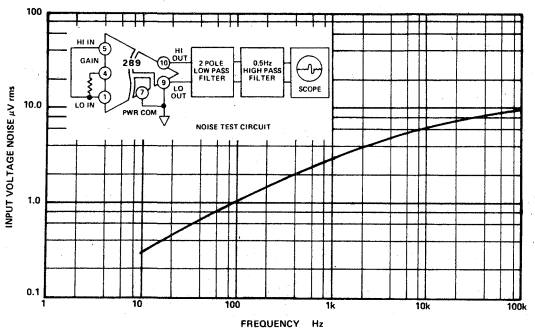


Figure 8. Typical Input Voltage Noise vs. Bandwidth

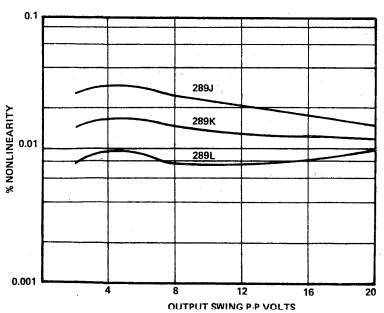


Figure 9. Typical Gain Nonlinearity vs. Output Swing

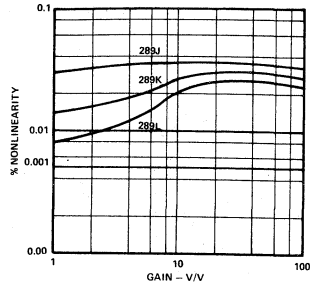


Figure 10. Typical Gain Nonlinearity vs. Gain

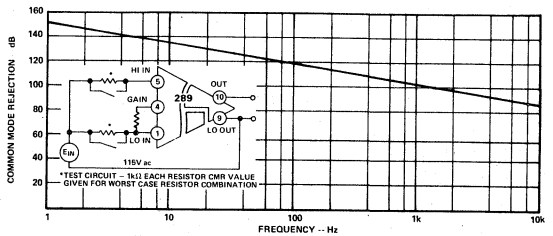


Figure 11. Typical Common Mode Rejection vs. Frequency at a Gain of 1V/V, CMR is typically 6dB Lower than at a Gain of 100V/V

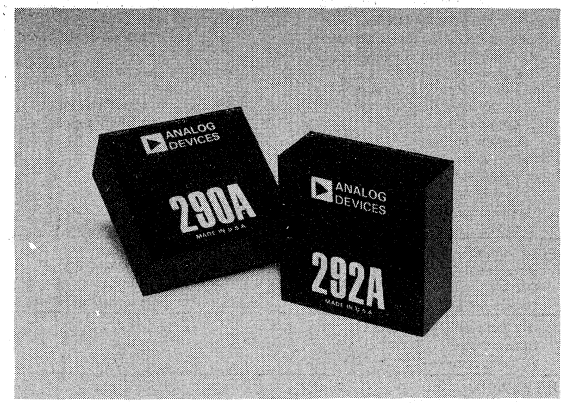
MULTICHANNEL APPLICATIONS

Isolation amplifiers containing internal oscillators may exhibit a slowly varying offset voltage at the output when used in multichannel applications. This offset voltage is the result of adjacent internal oscillators beating together. For example, if two adjacent isolation amplifiers have oscillator frequencies of 100.0kHz and 100.1kHz respectively, a portion of the difference frequency may appear as a slowly varying output offset voltage error. Model 289 eliminates this problem by offering a synchronization terminal (pin 8). When this terminal is interconnected with other model 289 synchronization terminals, the units are synchronized. Alternately, one or more units may be synchronized to an external 100kHz ±2% square-wave generator by the connection of synchronization termial(s) to that generator. The generator output should be 2.5V–5.0V p-p with 1kΩ source impedance to each unit. Use an external oscillator when you need to sync to an external 100kHz source, such as a sub-multiple of a microprocessor clock. A differential line driver, such as SN75158, can be used to drive large clusters of model 289. When using the synchronization pin, keep leads as short as possible and do not use shielded wire. These precautions are necessary to avoid capacitance from the synchronization terminal to other points. It should be noted that units synchronized must share the same power common to ensure a return path.

ANALOG DEVICES

Low Cost, Single and Multichannel Isolation Amplifier

MODELS 290A, 292A



FEATURES

Low Cost
Multichannel Capability Using External Oscillator (292A)
Isolated Power Supply: ±13V dc @ ±5mA (290A) or ±15mA (292A)
Low Nonlinearity: 0.1% @ 10V pk-pk Output
High Gain Stability: 0.001%/1000 Hours; 0.01%/°C
Small Size: 1.5″ × 1.5″ × 0.62″
Low Input Offset Voltage Drift: 10μV/°C (Gain = 100V/V)
Wide Input/Output Dynamic Range: 20V pk-pk
High CMV Isolation: 1500V dc, Continuous
Wide Gain Range: 1 to 100V/V

APPLICATIONS

Ground Loop Elimination in Industrial and Process Control
High Voltage Protection in Data Acquisition Systems
Off-Ground Signal Measurements

GENERAL DESCRIPTION

Models 290A and 292A are low cost, compact, isolation amplifiers that are optimized for single and multichannel industrial applications, respectively. The model 290A has a self-contained oscillator and is intended for single channel applications. A single external synchronizing oscillator can drive up to 16 model 292As or, a virtually limitless number of model 292As can be configured using multiple oscillators. The user can supply the external oscillator circuit or specify model 281 oscillator module, which includes a voltage regulator for operation over a wide single supply voltage range of +8V to +28V.

Models 290A and 292A design features include: adjustable gain, from 1 to 100V/V, dual isolated power, ±13V dc, ±1500V dc off ground isolation, 100dB minimum CMR at 60Hz, 1kΩ source imbalance, in a compact 1.5″ × 1.5″ × 0.6″ module. Models 290A and 292A achieve low input noise of 1μV pk-pk (10Hz bandwidth, G = 100V/V), nonlinearity of ±0.1% @ 10V pk-pk output, and an input/output dynamic range of 20V pk-pk.

Using modulation techniques with reliable transformer isolation, models 290A and 292A will interrupt ground loops, leakage paths, and voltage transients, while providing dc to 2kHz (−3dB) response.

WHERE TO USE MODELS 290A AND 292A

Industrial Applications: In data acquisition systems, computer interface systems, process signal isolators and high CMV instrumentation, models 290A and 292A offer complete galvanic isolation and protection against damage from transients and fault voltages. High level transducer interface capability is afforded with 20V pk-pk input signal range at a gain of 1V/V operation. In portable single or multichannel designs, single power supply operation (+8V to +16V) enables battery operation.

DESIGN FEATURES AND USER BENEFITS

Isolated Power: Dual ±13V dc output, completely isolated from the input power terminals (±1500V dc isolation), provides the capability to excite floating signal conditioners, front end buffer amplifiers and remote transducers such as thermistors or bridges.

Adjustable Gain: Models 290A and 292A adjustable gain offers compatibility with a wide class of input signals. A single external resistor enables gain adjustment from 1V/V to 100V/V providing flexibility in both high level transducer interfacing as well as low level sensor measurement applications.

Floating, Guarded Front-End: The input stage of models 290A and 292A can directly accept floating differential signals or it may be configured as a high performance instrumentation front-end to accept signals having CMV with respect to input power common.

High Reliability: Models 290A and 292A are conservatively designed, compact modules, capable of reliable operation in harsh environments. They have a calculated MTBF of over 400,000 hours and are designed to meet MIL-STD-202E environmental testing as well as the IEEE Standard for Transient Voltage Protection (472-1974: Surge Withstand Capability).

For detailed information, contact factory.

SPECIFICATIONS (typical @ +25°C; G = 100V/V and V_S = +15V dc, unless otherwise noted)

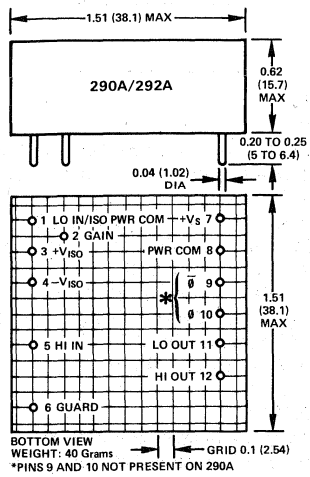
MODEL	290A	292A
GAIN (NONINVERTING)		
Range (50kΩ Load)		1 to 100V/V
Formula		$\text{Gain} = \left[1 + \frac{100k\Omega}{1k\Omega + R_i(k\Omega)}\right]$
Deviation from Formula		±3%
vs. Time		±0.001%/1000 Hours
vs. Temperature (-25°C to +85°C)[1]		±0.0075%/°C
Nonlinearity, G = 1V/V to 100V/V[2]		±0.1% (±0.25%)[3]
INPUT VOLTAGE RATINGS		
Linear Differential Range, G = 1V/V		±5V min (±10V min)[3]
Max Safe Differential Input		
Continuous, 1 min		110V rms
Max CMV, Inputs to Outputs		
ac, 60Hz, 1 Minute Duration		1500V rms max
Continuous, ac		±1000V pk max
Continuous, dc		±1500V pk max
CMR, Inputs to Outputs, 60Hz, $R_S \leq 1k\Omega$		
Balanced Source Impedance		106dB
1kΩ Hi In Lead Only		100dB min
Max Leakage Current, Inputs to Power Common		
@ 115V ac, 60Hz		10μA rms max
INPUT IMPEDANCE		
Differential		$10^8\Omega \| 70pF$
Overload		100kΩ
Common Mode		$5 \times 10^{10}\Omega \| 100pF$
INPUT DIFFERENCE CURRENT		
Initial, @ +25°C		+3nA
vs. Temperature (-25°C to +85°C)		±0.1nA/°C
INPUT NOISE		
Voltage, G = 100V/V		
0.01Hz to 10Hz		1μV p-p
10Hz to 1kHz		1.5μV rms
Current		
0.05Hz to 100Hz		5pA p-p
FREQUENCY RESPONSE		
Small Signal, -3dB, G = 1V/V		2.5kHz
Slew Rate		50mV/μs
Full Power, 10V p-p Output		
Gain - 1V/V thru 100V/V	2.0kHz(1.0kHz)[3]	3.0kHz(1.0kHz)[3]
OFFSET VOLTAGE REFERRED TO INPUT		
Initial, @ +25°C, Adjustable to Zero		±(5 + 50/G)mV
vs. Temperature (-25°C to +85°C)	±(10 + 150/G)μV/°C	±(8 + 250/G)μV/°C
vs. Supply Voltage		±1mV/%
RATED OUTPUT		
Voltage, 50k Load		±5V min (±10V min)[3]
Output Impedance		1kΩ
Output Ripple, 1MHz Bandwidth		10mV pk-pk
OSCILLATOR DRIVE INPUT		
Input Voltage	N/A	8 to 16V pk-pk
Input Frequency	N/A	100kHz ±5%, max
ISOLATED POWER OUTPUTS		
Voltage Full Load		±13V dc
Accuracy		±5%
Current[4]	±5mA min	±15mA min
Regulation, No Load to Full Load		+0, -15%
Ripple, 100kHz Bandwidth	200mV p-p	250mV p-p
POWER SUPPLY, SINGLE POLARITY		
Voltage, Rated Performance		+15V dc
Voltage, Operating		+8V dc to +15.5V dc
Current, Quiescent		+20mA
TEMPERATURE RANGE		
Rated Performance		-25°C to +85°C
Storage		-55°C to +85°C
CASE DIMENSIONS		1.5" X 1.5" X 0.62"

[1] Gain temperature drift is specified as a percentage of output signal level.
[2] Gain nonlinearity is specified as a percentage of 10V pk-pk output span.
[3] These specs apply for a 20V pk-pk output span.
[4] Do not load V_{ISO} when operating at output spans greater than 10V pk-pk.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



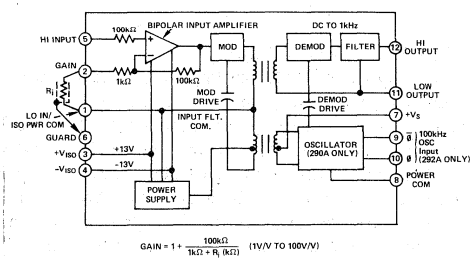


Figure 1. Block Diagram — Models 290A and 292A

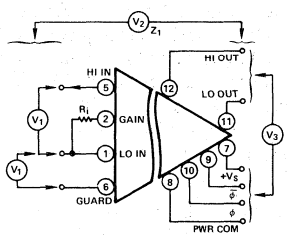


Figure 2. Model 290A and 292A Terminal Ratings

Symbol	Rating	Remarks
V_1	±110V rms (cont.)	Withstand Voltage, Steady State
V_2	±1000V pk (cont.)	Isolation, Steady State, ac
V_2	±1500V pk (cont.)	Isolation, Steady State, dc
V_2	±1500V rms (1 min)	Isolation, ac, 60Hz
V_3	±50V pk (cont.)	Isolation, dc
Z_1	$50G\Omega \| 20pF$	Isolation Impedance

Table 1. Isolation Ratings Between Terminals

CAUTION:

ESD(Electro-static-discharge) sensitive device. Permanent damage may occur on unconnected devices subjected to high-energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



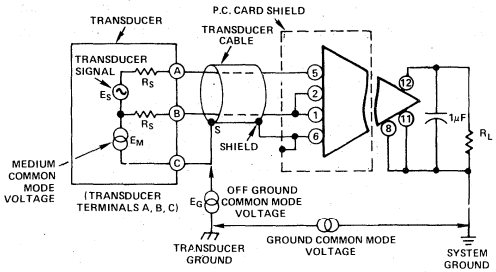
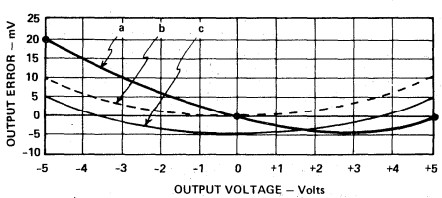


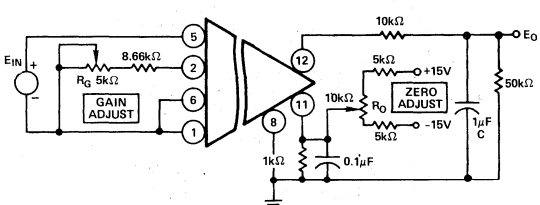
Figure 3. Transducer – Amplifier Interface

GAIN AND OFFSET TRIM PROCEDURE

In applying the isolation amplifier, highest accuracy is achieved by adjustment of gain and offset voltage to minimize the peak error encountered over the selected output voltage span. The following procedure illustrates a calibration technique which can be used to minimize output error. In this example, the output span is +5V to -5V and operation at Gain = 10V/V is desired.

1. Apply E_{IN} = 0 volts and adjust R_O for E_O = 0 volts.
2. Apply E_{IN} = +0.5V dc and adjust R_G for E_O = +5.0V dc.
3. Apply E_{IN} = -0.5V dc and measure the output error (see curve a).
4. Adjust R_G until the output error is one half that measured in step 3 (see curve b).
5. Apply +0.5V dc and adjust R_O until the output error is one half that measured in step 4 (see curve c).





GAIN RESISTOR, R_i, 1%, 50ppm/°C METAL FILM TYPE IS RECOMMENDED.
FOR GAIN = 1V/V, LEAVE TERMINAL 2 OPEN.
FOR GAIN = 100V/V, SHORT TERMINAL 2 TO TERMINAL 1

$$\text{GAIN} = 1 + \frac{100k\Omega}{1k\Omega + R_i(k\Omega)}$$

OUTPUT FILTER, 10kΩ RESISTOR AND CAPACITOR, C.
SELECT C TO ROLL-OFF NOISE AND OUTPUT RIPPLE:

$$f = (-3dB) = \frac{1}{2\pi C\,(11k\Omega)}$$

Figure 4. Gain and Offset Adjustment

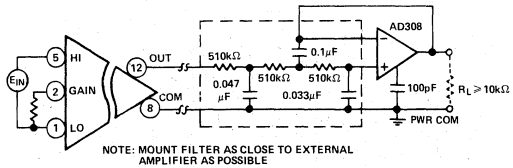


Figure 5. Selecting Bandwidth with a 3-Pole 5Hz Active Filter for Improved 60Hz Noise Reduction (typ 150dB @ 60Hz and 1kΩ Imbalance)

5

PERFORMANCE CHARACTERISTICS

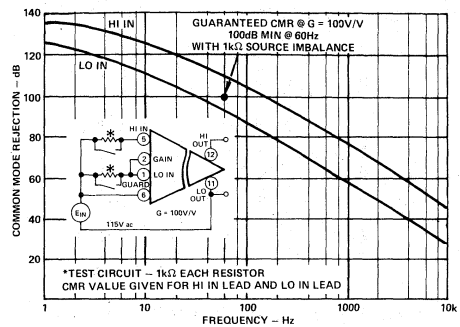


Figure 6. Typical Common Mode Rejection vs. Frequency

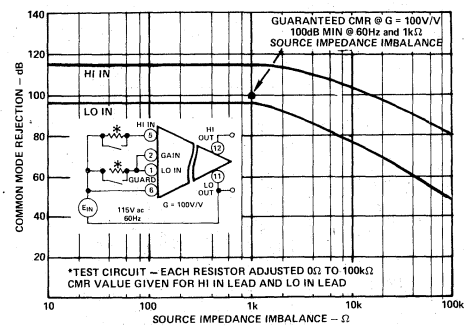


Figure 7. Typical Common Mode Rejection vs. Source Impedance Imbalance

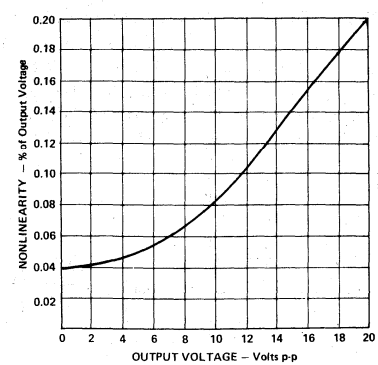


Figure 8. Typical Gain Nonlinearity vs. Output Voltage

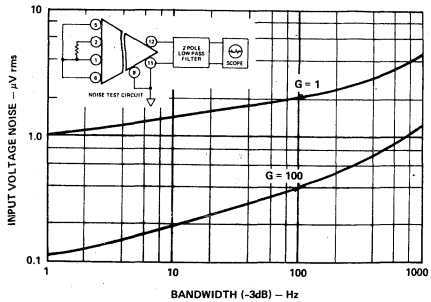


Figure 9. Typical Input Voltage Noise vs. Bandwidth

Input Offset Voltage Drift: Total input drift is composed of two sources, input and output stage drifts and is gain dependent. The curve of Figure 10 illustrates total input drift over the gain range of 1 to 100V/V.

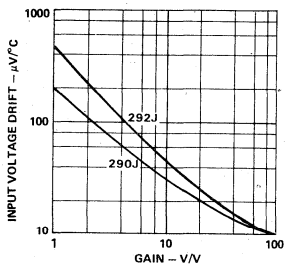
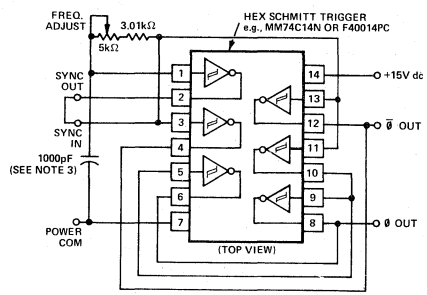


Figure 10. Typical Input Offset Voltage Drift vs. Gain

REFERENCE EXCITATION OSCILLATOR, MODEL 281

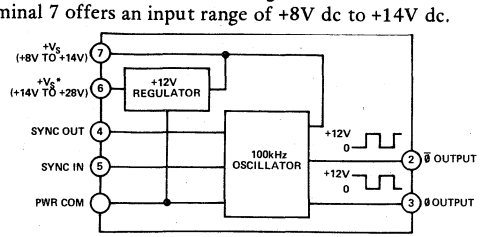
When applying model 292A, the user has the option of building a low cost 100kHz excitation oscillator, as shown in Figure 11, or purchasing a module from Analog Devices–model 281.



NOTES:
1. FREQ. ADJUST: ADJUST TRIM POT FOR OUTPUT FREQUENCY OF 100kHz ±5%.
2. FOR SLAVE OPERATION, REMOVE JUMPER FROM SYNC OUT AND SYNC IN PINS.
3. USE CERAMIC CAPACITOR, "COG" OR "NPO" CHARACTERISTIC.

Figure 11. 100kHz Oscillator Interconnection Diagram

The block diagram of model 281 is shown in Figure 12. An internal +12V dc regulator is provided to permit the user the option of operating over two, pin selectable, power input ranges; terminal 6 offers a range of +14V dc to +28V dc; terminal 7 offers an input range of +8V dc to +14V dc.



*LEAVE TERMINAL 6 OPEN, WHEN POWER IS APPLIED TO TERMINAL 7.

Figure 12. Model 281 Block Diagram

Model 281 oscillator is capable of driving up to 16 model 292As. As shown in Figure 13, an additional model 281 may be driven in a slave-mode to expand the total system channels from 16 to 32. By adding additional model 281s in this manner, systems of over 1000 channels may be easily configured.

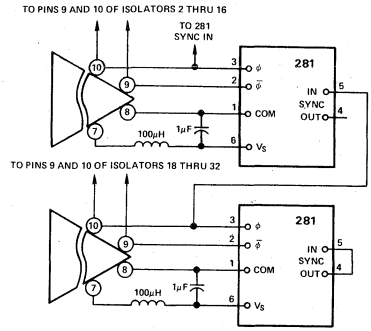


Figure 13. External Oscillator Interconnection

SPECIFICATIONS
(typical @ +25°C and V_S = +15V dc unless otherwise noted)

MODEL	281
OUTPUT	
Frequency	100kHz ±5%
Waveform	Squarewave
Voltage (ϕ and $\bar{\phi}$ terminals)	0 to +12V pk
Fan-Out[1,2]	16 max
POWER SUPPLY RANGE[3]	
High Input, Pin 6	+(14 to 28)V dc
Quiescent Current, N.L.	+5mA
F.L.	+16mA
Low Input, Pin 7	+(8 to 14)V dc
Quiescent Current, N.L.	+12mA
F.L.	+33mA
TEMPERATURE	
Rated Performance	0 to +70°C
Storage	-55°C to +85°C

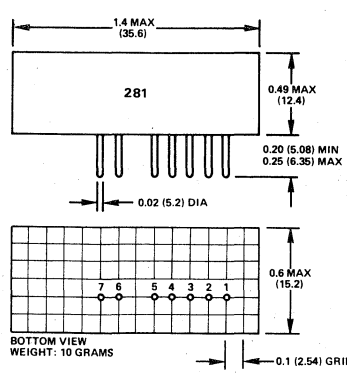
[1] Model 292A oscillator drive input represents unity oscillator load.
[2] For applications requiring more than 16 292As, additional 281s may be used in a master/slave mode. Refer to Figure 13.
[3] Full load consists of 16 model 292As and 281 oscillator slave.

Specifications subject to change without notice.

See Caution note on specifications table.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



PIN TERMINAL IDENTIFICATION

1	POWER COMMON	5	SYNC INPUT
2	$\bar{\phi}$ OUTPUT	6	$+V_S$: HIGH RANGE +(14 to 28)V dc
3	ϕ OUTPUT	7	$+V_S$: LOW RANGE +(8 to 14)V dc
4	SYNC OUTPUT		

MATING SOCKET:
CINCH #16 DIP OR EQUIVALENT

Analog Multipliers/Dividers

Contents

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General Information and Definitions of Specifications	6-4
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433J/B Multifunction Device: $Y(Z/X)^m$	6-11
436A/B Highest-Accuracy Internally Trimmed 2-Quadrant Divider	6-15

6

Selection Guide
Analog Multipliers/Dividers

In this Selection Guide, multiplier/divider products are partitioned into four categories:

1. General-purpose devices capable of optimization as multipliers or dividers
2. Internally trimmed devices optimized as multipliers
3. Internally trimmed devices optimized as dividers
4. Multifunction devices

Complete and detailed specifications, descriptions, and application information can be found in the data sheets. General information and definitions of important specifications can be found in the following pages.† Specifications are typical at rated supply voltage and load, and T_A = +25°C, unless noted otherwise.

1. GENERAL-PURPOSE EXTERNALLY TRIMMED DEVICES

Type	Characteristics	Vol I Page	Vol II Page
AD533J/K/L/S	Lowest cost general-purpose 4-quadrant multiplier, external trim to 0.5% max total error (L)	6-17	–

2. INTERNALLY TRIMMED MULTIPLIERS

Type	Characteristics		
AD532J/K/S	General-purpose 4-quadrant multiplier, differential inputs, standard pinouts, internally trimmed to 1.0% max total error (K), 0.04%/°C max (S)	6-11	–
Model 429A/B	Wide-bandwidth 4-quadrant multiplier, full-power response to 2MHz min, slewing rate 120V/μs min, -3dB bandwidth 10MHz, small-signal, 1% settling-time 500ns; pretrimmed to 0.5% max error (B)	6-37	6-7
AD534J/K/L/S/T	High-accuracy internally trimmed 4-quadrant multiplier featuring 0.25% max total error (L), low noise (90μV rms, 10Hz – 10kHz), and versatile differential input configuration.	6-21	–
AD539J/S	Wideband low distortion dual-channel 2-quadrant log/linear multiplier, signal bandwidth 35MHz	6-35	–

3. INTERNALLY TRIMMED DIVIDERS

Type	Characteristics		
Model 436A/B	High-accuracy 2-quadrant divider-only, pretrimmed to 0.25% max error (B, denominator [V_X] range from +0.1V to +10V [$\lvert V_Z \rvert \leqslant \lvert V_X \rvert$]), 2% max error over temperature (B), 1% max error 0 to +70°C.	–	6-15
AD535J/K#	2-quadrant divider, pretrimmed for 0.5% max total error (K version) for 10:1 denominator range. Differential inputs permit choice of denominator range. Differential inputs permit choice of denominator polarity.	6-29	–

4. MULTIFUNCTION DEVICES

Type	Characteristics		
Model 433J/B	Programmable multifunction device, $Y(Z/X)^m$ ($10V/E_{REF}$), one quadrant, m adjustable from 0.2 to 5, max division error 25mV (B, V_Z from 0.01V to 10V, V_X from 0.1V to 10V, $V_Z \leqslant V_X$), 1% max over temperature.	6-39	6-11

†Letter suffixes denote temperature range and performance grade. J/K/L are specified for 0 to +70°C; A/B are specified for -25°C to +85°C; S/T are specified for -55°C to +125°C.

Orientation
Analog Multipliers/Dividers

The devices catalogued in this section are high-performance modules that accept analog voltages and multiply, divide, square, and/or square-root them, depending on device properties and connections. As the Selection Guide indicates, a variety of additional devices performing comparable functions using IC technologies may be found in Volume I.

Multiplication For two inputs, V_x and V_y, a multiplier will provide the output, $E_{out} = V_xV_y/E_{ref}$, where E_{ref} is a dimensional constant, usually of 10V nominal value. If E_{ref} = 10V, E_{out} = 10V when V_x and V_y are 10V. Multipliers are used for modulation and demodulation, fixed and variable remote gain adjustment, power measurement, and mathematical operations in analog computing, curve fitting, and linearizing.

If the inputs may be of either positive or negative polarity, and the output polarity is in a correct relationship for multiplication, the device is called a "four-quadrant" multiplier, reflecting the 4 quadrants of the X-Y plane.

Squaring If $V_x = V_y = V_{in}$, a multiplier's output will be V_{in}^2/E_{ref}. A four-quadrant multiplier, used as a squarer, will have an output that is positive, whether V_{in} is positive or negative. Squarers are useful in frequency doubling, power measurement of constant loads, and mathematical operations.

Division For a numerator input, V_z, and a denominator input, V_x, an analog divider will provide the output, $E_{out} = E_{ref}(V_z/V_x)$. If E_{ref} = 10V, E_{out} will be 10V or less for $V_z \leqslant V_x$. V_x is of a single polarity and will not provide meaningful results if it approaches zero too closely. If V_z may be of either positive or negative polarity, the device is described as a "two-quadrant" divider, and the output will reflect the polarity of V_z. Analog dividers are used to compute ratios—such as efficiency, attenuation, or gain; they are also used for fixed and variable remote gain adjustment, ratiometric measurements, and for mathematical operations in analog computing.

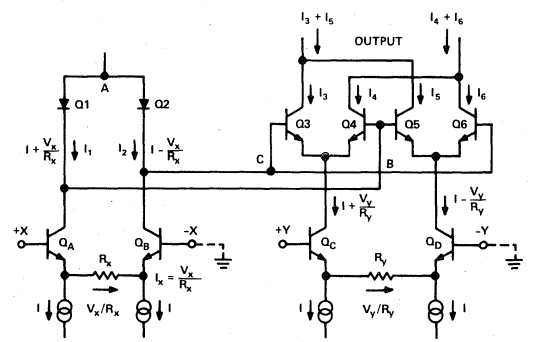
Square rooting For a numerator input, V_{in}, and a denominator input, E_o (the output fed back to the denominator input), the output of a divider is $E_o = E_{ref}(V_{in}/E_o)$; hence $E_o = \sqrt{E_{ref}V_{in}}$. A square-rooter works in one quadrant; some devices require external diode circuitry to prevent latchup if the input polarity changes, even momentarily. Square roots are used in vector and rms computation, to linearize flowmeters, and for mathematical operations in analog computing.

CHOOSING A MULTIPLIER, DIVIDER, etc.

A number of devices are listed here, differing in internal architecutre, external functional configuration, and performance specifications. Most have essentially fixed references; the model 433 is a *multifunction device* that performs the one-quadrant operation, $E_o = V_z(V_y/V_x)^m$, where m is an exponent adjustable from 1/5 to 5. With one exception (model 436 precision 2-quadrant divider), all of the devices listed here can be used for any of the functions defined above.

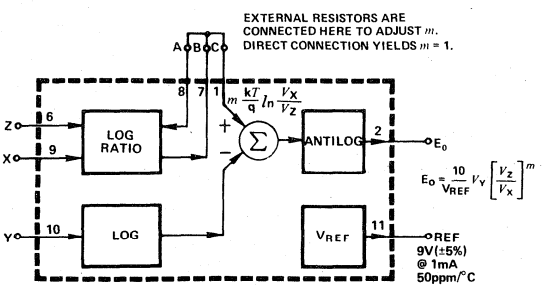
Considerable information on these functions, the nature of devices to perform them, and extensive discussions of their applications can be found in two publications available from Analog Devices.[1,2] A wealth of information is also to be found in the data sheets for the individual devices, published in this section. In addition to the products listed here, a number of popular earlier products are still available; data sheets are available upon request.

Internal Architecture All of the devices in this section rely on the logarithmic properties of silicon P-N junctions. With the exception of models 433 and 436, the circuit employed is basically like that of the "Gilbert cell" (its 4-quadrant-multiplying circuitry and performance are described in (1) and (2), with further references to original sources). The input voltages are converted to currents, the currents are multiplied together and divided by a reference, and the net output current, I_xI_y/I_{ref}, is converted to voltage by feedback around the output amplifier. The feedback terminals are available as inputs for applications involving division.



Basic 4-Quadrant Variable-Transconductance Multiplier Circuit

$$I_O = (I_3 + I_5) - (I_4 + I_6) = \frac{2\,V_X\,V_Y}{I\,R_X\,R_Y}$$



Functional Block Diagram of Model 433

In multifunction devices like Model 433, the feedback currents of the input op amps are used to develop logarithmic

[1] *Multiplier Application Guide*, available upon request
[2] *Nonlinear Circuits Handbook*, D. H. Sheingold, ed., 1976, 536pp., $5.95, P.O. Box 796, Norwood MA 02062

voltages across transistor base-emitter junctions; these voltages are summed and differenced and produce an exponential current proportional to V_yV_z/V_x via another transistor junction in the input path of the output amplifier. Thus, the output voltage is proportional to V_yV_z/V_x; an internally generated reference voltage is available as a fixed reference for the odd input in two-variable operations. In the 433, the internal emitter-voltage difference proportional to log (V_z/V_x) can be amplified or attenuated by the appropriate connection of a resistive attenuator with an attenuation ratio, m; since the antilog of $m(\log V_z/V_x)$ is $(V_z/V_x)^m$, the output of the 433 is proportional to $V_y(V_z/V_x)^m$. In the model 436 divider, the inputs are scaled and linearly combined, before the log-antilog computation takes place; the result is that the numerator (of V_z/V_x) may have positive or negative values. The 436 circuit is optimized and trimmed for performance as a dedicated divider; it has a fixed reference.

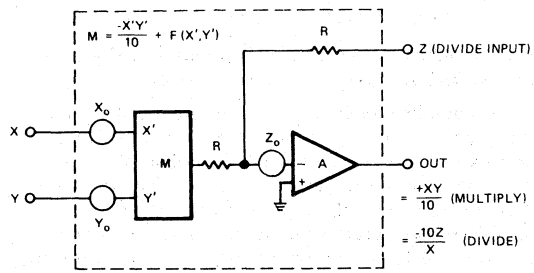
External functional configuration As noted earlier, with the exception of the model 436 dedicated divider, all of the devices listed here can be used for multiplication, division, squaring, and/or square-rooting (MDSSR), by the appropriate connection of external jumpers. Performance of pretrimmed devices is optimized in specified modes of operation. The data sheets show how devices are connected for the various modes of operation; where appropriate, the trim circuits and procedures for optimizing performance are provided.

Technologies The devices described in these two volumes are either monolithic integrated circuits or high-performance modules. For any application, the user will evaluate a device on the basis of its performance in the desired mode(s). The modules in Volume II provide the highest performance: speed (model 429), accuracy as a divider (436), and accuracy in multifunction applications (433). On the other hand, the ICs in Volume I provide economy of cost and space, and the availability of "mil-temp" range (-55°C to +125°C) versions. The pretrimmed IC's (AD534, AD535 and AD532) use laser trimming of thin-film-on-silicon chips at the wafer stage and buried-Zener reference circuitry, as well as thermally balanced input stages and "core" circuitry, for overall maximum errors to 0.25%, and linearities as yet unmatched in the industry.

Performance Multiplier performance, specifications and test circuitry are described in great detail in the NONLINEAR CIRCUITS HANDBOOK. Here is a brief digest of the factors relating to low-frequency performance.

In theory, a multiplier has an output which is ideally the product of two input variables, X and Y, divided by the 10V scaling voltage. However, the practical multiplier is subject to various offset errors and nonlinearities, which must be accounted for in its application. This discussion is intended to assist the designer in understanding and interpreting multiplier and divider specifications and obtaining insight into device performance.

In practice (see the figure), the multiplier may be considered as having two parts, one (M) contains the input circuitry and the multiplying cell; the other is the gain-conditioning op amp, A.



Functional Block Diagram of Typical Multiplier/Divider

Also summed at the op-amp input is the feedback variable, Z. In multiplication, Z is connected to the output circuit. In division, Z and X are the inputs, and Y is connected to the output. The figure shows a model used for considering errors. X_o and Y_o are input offset voltages, Z_o is the offset-referred-to-the-input of the output amplifier, and $F(X', Y')$ is the nonlinearity, viewed as the departure from the ideal multiplication, $\frac{X'Y'}{10R}$. The output equation, including the errors is of the form

$$E_o = \frac{XY}{10B} \pm \left[\underbrace{\frac{X_oY}{10B}}_{\text{Linear "Y"}} \pm \underbrace{\frac{XY_o}{10B}}_{\text{Feedthrough "X"}} \pm \underbrace{Z_o}_{\text{Output offset}} + \underbrace{f(X,Y)}_{\text{Nonlinearity and feedthrough}}\right]$$

Product X_{offset} Y_{offset}

The errors are included in the bracketed term, except for gain error, which is the departure of "B", the gain-error term, from its nominal value of unity. The effects of input offsets (called "linear feedthrough") can be set to zero by applying external input biases, the output offset can be set to zero by biasing the output amplifier, and the gain can be externally calibrated by adjusting the reference or the feedback resistance. The remaining departure from the ideal output for any combination of input values is the irreducible *linearity error*, or *nonlinearity*, a function of X and Y that differs from device to device and, with temperature, within a given device. The component of nonlinearity for X = 0 is called "Y feedthrough" and for Y = 0, it is called "X feedthrough".

The "total error" specification includes the effects of all these errors. Although a guide to performance, it may produce an excessively conservative design in some applications. For example, output offset is not important if the output is to be capacitively coupled or the initial offset is nulled. Gain error is not important if system gain is to be adjusted elsewhere in the system or if gain is not a critical factor in system performance. If frequent calibration of offset and scale-factor errors is available (e.g., in a "smart" instrument, via software) non-

linearity becomes the limiting parameter. In such cases, improvements in predicted error can be achieved by using the approximate linearity equation:

$$f(X,Y) \cong |V_x| \epsilon_x + |V_y| \epsilon_y$$

were ϵ_x and ϵ_y are the specified fractional linearity errors (%/100) and V_x and V_y are the input signals.

When multipliers are fed back for use in division applications, it is important to recognize that maximum multiplication errors are increased approximately in proportion to the inverse of the denominator voltage ($10V/V_x$), and bandwidth is decreased in proportion to denominator voltage. Pretrimmed multipliers used in such applications, with wide dynamic range of X (e.g., 10:1), will always benefit greatly by the trimming of offsets, especially Z_O (affects offsets) and X_O (affects gain), for small values of X.

DEFINITIONS OF SPECIFICATIONS*

Accuracy is defined in terms of *total error* of the multiplier at room temperature and constant nominal supply voltage. *Total error* includes the sum of the effects of input and output dc offsets, nonlinearity, and feedthrough. *Temperature dependence* and *supply-voltage effects* are specified separately.

Scale Factor The *scale-factor error* (or *gain* error) is the difference between the average scale factor and the ideal scale factor (e.g., $(10V)^{-1}$). It is expressed in percent of the output signal. *Temperature dependence* is specified.

Output Offset refers to the offset voltage at the output-amplifier stage. This offset is usually minimized at manufacture and can be trimmed where high accuracy is desired. Output *offset vs. temperature* is also specified.

Linearity Error or *Nonlinearity* is the maximum difference between actual and "best-straight-line" theoretical output, for all pairs of input values, expressed as a percentage of full scale, with all other dc errors nulled. It is the irreducible minimum error. It is usually expressed in terms of X and Y nonlinearity, with the named input swinging over its full-scale range and the other input at (±) 10V. Y nonlinearity is considerably less than X nonlinearity in "Gilbert-cell" multipliers. This specification includes nonlinear feedthrough.

X or Y Feedthrough is the signal at the output for any value of X or Y input in the rated range, when the other input is zero. It has two components, a linear one, corresponding to an *input offset* at the zero input, which can be trimmed out (but can drift and has a *temperature specification*), and a nonlinear one, which is irreducible. *Feedthrough* is usually specified at one frequency (50Hz) for a 20V p-p sine wave input. It increases with frequency, and plots of typical feedthrough vs. frequency are provided on multiplier data sheets.

Noise is specified and measured with both inputs at zero signal and zero impedance (i.e., shorted). For low-frequency applications, filtering the output of the multiplier may improve small-signal resolution significantly.

Dynamic Parameters include: *small-signal bandwidth, full-power response, slew(ing) rate, small-signal amplitude error,* and *settling time.*

Small-signal bandwidth is the frequency at which the output is down 3dB from its low-frequency value (i.e., by about 30%) for a nominal output amplitude of 10% of full scale.

Full-power response is the maximum frequency at which the multiplier can produce full-scale voltage into its rated load without noticeable distortion.

Slew(ing) rate is the maximum rate of change of output voltage for the product of a full-scale dc voltage and a full-scale step input.

Small-signal amplitude error is defined in relation to the frequency at which the amplitude response, or scale factor, is in error by 1%, measured with a small (10% of full-scale) signal.

Settling time, for the product of a ±10V step and 10Vdc, is the total length of time the output takes to respond to an input change and stay within some specified error band of its final value. Settling time cannot be accurately predicted from any other dynamic specifications; it is specified in terms of a prescribed measurement.

Vector error is the most-sensitive measure of dynamic error. It is usually specified in terms of the frequency at which a phase error of 0.01 radians (0.57°) occurs.

*These are general definitions. Further definitions are provided as footnotes to the specification tables; they should be read carefully.

ANALOG DEVICES

Accurate, Wideband, Multiplier, Divider, Square Rooter

MODEL 429

FEATURES:
- 1.0%/0.5% Accuracy without Trimming (429A/B)
- Low Drift to 1.0mV/°C max
- Wideband — 10MHz
- 0.2% Nonlinearity max (429B)
- External Amplifiers not Required
- MTBF: 169, 268 Hours

APPLICATIONS:
- Fast Divider
- Modulation and Demodulation
- Phase Detection
- Instrumentation Calculations
- Analog Computer Functions
- Adaptive Process Control
- Trigonometric Computations



GENERAL DESCRIPTION

The model 429, an extremely fast multiplier/divider, should be considered if bandwidth, temperature coefficient, or accuracy are critical parameters. Based on the transconductance principle to achieve high speed, the model 429 offers a unique combination of features, those being ½% max error (429B) and 10MHz small signal bandwidth.

Both models 429A and 429B are internally trimmed achieving max errors of 1.0% and 0.5% respectively. By fine trimming the offset and feedthrough with external trim potentiometers typical performance may be improved to 0.5% for the 429A and 0.2% for the 429B.

In addition to high accuracy and high bandwidth, the model 429 offers exceptionally good stability for changes in ambient temperature. Model 429B is 100% temperature tested in order to guarantee an overall accuracy temperature coefficient of only 0.04%/°C max. Additionally, offset drift is held to only 1mV/°C max. To satisfy OEM requirements of low cost, the 429 uses transconductance principles with the latest design techniques and components to achieve guaranteed performance at competitive prices.

MULTIPLICATION ACCURACY

Multiplication accuracy is generally specified as a percentage of full scale output. This implies that error is independent of signal level. However, for signal levels less than 2/3 of full scale, error tends to decrease roughly in proportion to the input signal. A good approximation of error behavior is:

$f(X, Y) \cong |X| \epsilon_x + |Y| \epsilon_y$, where ϵ_x and ϵ_y are the fractional nonlinearities specified for the X and Y inputs

EXAMPLE: For model 429A, $\epsilon_x = 0.5\%$, $\epsilon_y = 0.3\%$. What maximum error can one expect for x = 5V, y = 1V, providing the offset is zeroed out? Can one get less by interchanging inputs?

1. Nominal output is XY/10 = (5)(1)/10 = 500mV
2. Expected error is (5) (0.5%) + (1) (0.3%) = 28mV, 5.6% of output (0.28% of F.S.)
3. Interchanging inputs (1) (0.5%) + (5) (0.3%) = 20mV, 4.0% of output (0.20% of F.S.)

Compare this with the overly conservative error predicted by the overall 1% of full scale specification: 100mV, or 20% of output.

FREQUENCY RELATED SPECIFICATIONS

Accuracy, and its components, feedthrough, linearity, gain, (and phase shift) are frequency dependent. Feedthrough is constant up to 100kHz for the Y input, and up to 400kHz for the X input. Beyond these frequencies it rises at approximately a 6dB/octave rate due to distributed capacitive coupling. A plot of typical feedthrough vs. frequency is shown in Figure 1. For this measurement one input is driven with a 20V p-p sine wave while the other input is grounded and the feedthrough is measured at the output. This error will decrease roughly in proportion to the input signal, and will also vary with temperature (about 0.01%/°C of the nonzero input). Low frequency feedthrough error can be further reduced from the internally trimmed limits by the use of optional external potentiometers.

Nonlinearity likewise increases with frequency at a 6dB/octave rate above the break frequency. With the Y input driven at 10V p-p, and the X input anywhere between ±10V dc, the break frequency is 25kHz. For corresponding X input conditions, the break occurs at 60kHz. Figure 2 is a plot of the typical nonlinearity vs. frequency for the model 429.

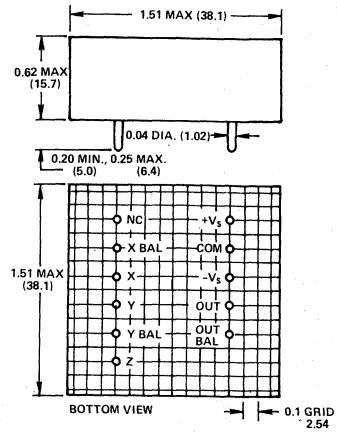
SPECIFICATIONS (typical @ +25°C and ±15VDC unless otherwise noted)

MODEL	429A	429B
MULTIPLICATION CHARACTERISTICS		
Output Function	XY/10	*
Error, with Internal Trim, at +25°C	±1% max	±0.5% max
Error, with External Trim, at +25°C	±0.7%	±0.3%
Avg. vs. Temp (−25°C to +85°C)	±0.05%/°C	±0.04%/°C max
Avg vs. Supply	±0.05%/%	*
SCALE FACTOR		
Initial Error at +25°C	0.5%	0.25%
Avg vs. Temp (−25°C to +85°C)	0.03%/°C	0.02%/°C
Avg vs. Supply	0.03%/%	*
OUTPUT OFFSET		
Initial at +25°C (Adjustable to Zero)	±20mV max	±10mV max
Avg vs. Temp (−25°C to +85°C)	±2mV/°C	±1mV/°C max
Avg vs. Supply	±1mV/%	*
NONLINEARITY		
X Input		
(X = 20V p-p 50Hz, Y = ±10V)	0.5% max	0.2% max
Y Input		
(Y = 20V p-p 50Hz, X = ±10V)	0.3% max	0.2% max
FEEDTHROUGH		
X = 0, Y = 20V p-p, 50Hz	50mV p-p, max	20mV p-p, max
With External Trim	16mV p-p	10mV p-p
Y = 0, X = 20V p-p, 50Hz	100mV p-p, max	30mV p-p, max
With External Trim	50mV p-p	20mV p-p
BANDWIDTH		
−3dB	10MHz	*
Full Power Response	2MHz min	*
Slew Rate	120V/μs min	*
1% Amplitude Error	300kHz min	*
1% Vector Error (0.57°)	50kHz min	*
Differential Phase Shift ($\theta_x - \theta_y$)	1° @ 1MHz	*
Small Signal Rise Time 10-90%	40ns	*
Settling to ±1% (±10V step)	500ns	*
Overload Recovery	0.2μs	*
OUTPUT NOISE		
5Hz to 10kHz	0.6mV rms	*
5Hz to 10MHz	3.0mV rms	*
OUTPUT CHARACTERISTICS		
Voltage, 1kΩ load	±11V min	*
Current	±11mA min	*
Load Capacitance	0.01μF max	*
INPUT RESISTANCE		
X Input	10kΩ±5%	*
Y Input	11kΩ±2%	*
Z Input	27kΩ±10%	*
INPUT BIAS CURRENT		
Input X, Y, Z	±100nA	*
Z	±20μA	*
MAXIMUM INPUT VOLTAGE		
For Rated Accuracy	±10.5V	*
Maximum Safe	±16V	*
WARM UP		
To Rated Specifications	1 second	*
POWER SUPPLY[1]		
Rated Performance	±(14.8 to 15.3)V dc	*
Operating	±(14 to 16)V dc	*
Quiescent Current	±12mA	*
TEMPERATURE RANGE		
Rated Performance	−25°C to +85°C	*
Operating	−25°C to +85°C	*
Storage	−55°C to +125°C	*
MECHANICAL		
Weight	2 oz.	*
Socket	AC1023	*
Case Dimensions	1.5" x 1.5" x 0.62"	*

*Specifications same as model 429A.
[1] Recommended power supply, ADI model 904, ±15V @ 50mA output.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

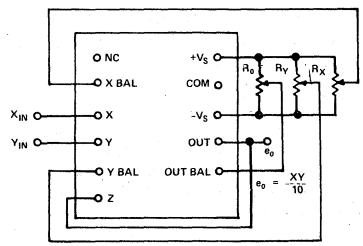
Dimensions shown in inches and (mm).



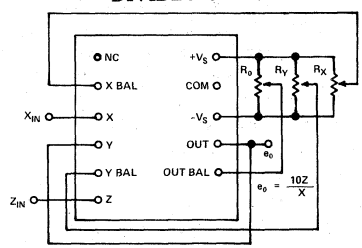
PIN CONNECTIONS

Bottom View Shown in all Figures.
Optional Trim Pots
Shown are not Required
for Rated Accuracy.

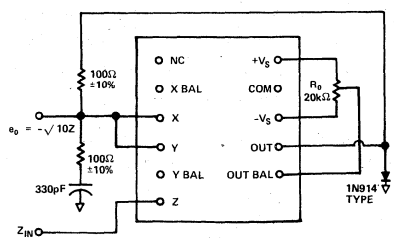
MULTIPLY MODE



DIVIDE MODE



SQUARE ROOT MODE



All trim pots 20kΩ.

Gain and input to output phase shift for the model 429 are shown in Figure 2. Naturally, no multiplier will maintain accuracy at frequencies approaching the small signal bandwidth. For the model 429, the 1% amplitude error will occur at 500kHz. If input to output phase shift is a criterion, then the 1% "vector" error occurs at 50kHz.

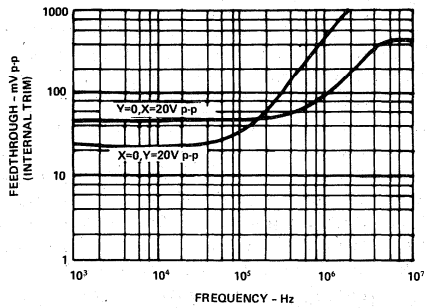


Figure 1. Feedthrough vs Frequency

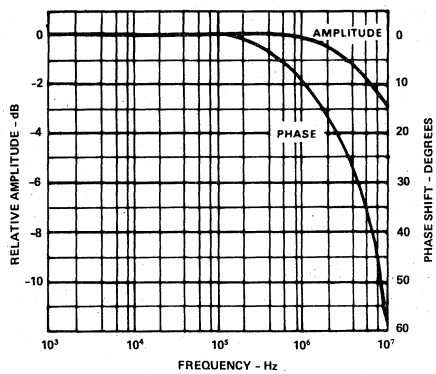


Figure 2. Typical Amplitude and Phase vs Frequency

OPTIONAL TRIM — MULTIPLY MODE

As shipped, the multiplier meets its listed specifications without use of any external trim potentiometers. Terminals are provided for optional feedthrough and offset adjustments. Using these adjustments overall static multiplication error may be reduced to only 0.2%. The 20kΩ trim potentiometers should be connected across the ± supply voltage terminals with the arm of each potentiometer connected to the desired balance terminal (see Specifications page).

ADJUSTMENT PROCEDURE FOR OFFSET

1. Jumper X input and Y input to ground.
2. Adjust R_0 for an output of zero volts.
3. Remove jumper from X and Y inputs.

ADJUSTMENT PROCEDURE FOR FEEDTHROUGH

1. Jumper Y input to ground and apply 20V p-p at 1kHz to X input.
2. Adjust R_Y for minimum output voltage.
3. Remove jumper from Y input.
4. Jumper X input to ground and apply 20V p-p at 1kHz to Y input.
5. Adjust R_X for minimum output voltage.
6. Remove jumper from X terminal.

DIVISION

The high bandwidth and excellent linearity of model 429 allows it to be used in divider applications achieving high performance in the dc to 8MHz region. Restrictions imposed on divide operation, and the contribution of error terms are illustrated in the error analysis below.

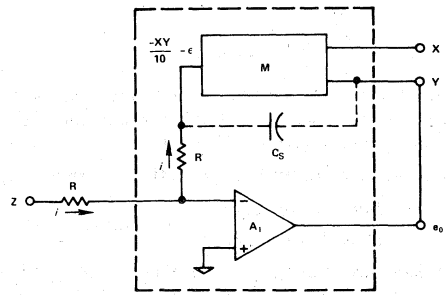


Figure 3. Divider Circuit

Shown in Figure 3 is a typical multiplier/divider which has been connected for divide operation by inserting the multiplier cell, M, in the op amp's feedback loop. Errors associated with the op amp, A_1, are incorporated in ϵ, which represents all errors. In order to insure negative feedback, the X input range is restricted to negative values.

Summing currents at the op amp's summing junction:

$$\frac{Z}{R} = \frac{\frac{XY}{10} + \epsilon}{R}$$

Solving for Y, which is also ϵ_0:

$$Y = \frac{10\,(Z - \epsilon)}{X}$$

or,

$$\epsilon_0 = \frac{10Z}{X} - \frac{10\epsilon}{X}$$

And now breaking ϵ into its constituents

$$\epsilon_0 = \underbrace{\frac{10Z}{X}}_{\text{ideal divider}} - \underbrace{\frac{10E_{NV}}{X}}_{\text{noise error}} - \underbrace{\frac{10E_{OS}}{X}}_{\text{offset error}} - \underbrace{\frac{10E_{OS}/^{\circ}C}{X}}_{\text{offset drift error}} - \underbrace{\frac{10E_{NLX}}{X}}_{\text{X nonlinearity error}} - \underbrace{\frac{10E_{NLY}}{X}}_{\text{Y nonlinearity error}}$$

These errors can be broken down into two categories, static errors and signal dependent errors. All of the static errors associated with the divide mode are inversely proportional to the denominator signal level. The signal dependent errors are the X and Y nonlinearities. For model 429B nonlinearity errors are 0.2% for both the X and Y inputs. Substituting these values in the error terms yields:

$$-\frac{10\,(0.2\%)\,X}{X} - \frac{10\,(0.2\%)\,Y}{X}$$

The importance of using the terminal with largest nonlinearity for the denominator is revealed by the above expression. Effects of X nonlinearity are virtually independent of signal level and may be trimmed out. Nonlinearities of Y typically contribute 200mV for X = Z = 1V i.e., (10 [0.2%] 10V) = 200mV. This error can be reduced if external trims are used to optimize divider performance.

Bandwidth is also degraded with a decrease in denominator level, due to the increase in system gain;

i.e.) for X = Z = 1V, ϵ_0 = 10V

$$\text{and} \quad \frac{\epsilon_0}{Z} = \frac{10}{1} = 10$$

Since the gain bandwidth product is constant, a bandwidth of 1/10 of that obtained for full scale denominator levels will be obtained for division at 1V levels.

For other denominator levels, bandwidth is determined by:

$$\text{B. W.} = \frac{\text{Denominator Level}}{\text{Full Scale Denominator}} \times (\text{Multiplier B.W.}) \times K$$

where K is a constant having a value less than unity. It is introduced due to a combination of stray capacitance paralleling the multiplier cell and effects of feedthrough. For model 429

$$\text{B.W.} = \left(\frac{X}{10}\right) 8\text{MHz}$$

Before selecting a multiplier/divider for divide applications, errors resulting from the lowest anticipated denominator signal should be considered. After such considerations have been made, one can further appreciate the importance of starting with an accurate, high speed multiplier such as model 429. It is also highly recommended that the optional trim procedure for division be performed.

OPTIONAL TRIMMING – DIVIDE MODE

Connections are made as shown on Specifications page.

The suggested trim procedure is (starting with centered adjust adjustments):

*1. With Z = 0, trim R_0 to hold output constant, as X is varied from -10V toward -1.0V.
2. With Z = 0, trim R_Y for zero at X = -10V.
3. With Z = X and/or Z = -X, trim R_X for minimum worst-case variation as X is varied from -10V to -1.0V.
4. Repeat 1 and 2 if step 3 required large initial adjustment.

*For best accuracy X should be allowed to vary from -10V to lowest expected denominator.

SQUARE ROOTING

When connected as shown on Specifications page, the model 429 will provide the square root of Z_{IN}.

By summing currents at the op amp's summing junction:

$$\frac{Z}{R} = \frac{XY}{10R} + \frac{\epsilon}{R} = \frac{Y^2}{10R} + \frac{\epsilon}{R}$$

where ϵ represents all errors associated with the multiplier. Solving for the output voltage, Y.

$$\epsilon_0 = \pm \sqrt{10\,(Z - \epsilon)}$$

There are two values of ϵ_0 for every value of Z. However, only negative values of ϵ_0 will provide the negative feedback necessary for circuit stability. To restrict the output from going positive, a diode is connected as shown on Specifications page. The output is then:

$$\epsilon_0 = -\sqrt{10\,(Z - \epsilon)}$$

Errors, ϵ, associated with the multiplier, are inside the square root and consequently their effect, for large values of Z, is reduced. The reason for the improved performance can be seen by inspecting the circuit. The output is fed back to both the X and Z terminals, resulting in twice the feedback as would be obtained for the divide mode. An alternative method of considering error performance is to consider errors as being at the Z terminal. By differentiating the ideal transfer function with respect to Z, errors for various values of Z may be determined:

$$\frac{de_0}{dZ} = \frac{d}{dZ}\sqrt{10Z} = \tfrac{1}{2}\sqrt{\frac{10}{Z}}$$

The factor of ½ has the advantage of reducing errors by a factor of 2 for Z = 10, but also introduces the potential problem of instability. Since the feedback gain is the reciprocal of the forward gain, the slope of the forward gain is 2. Additional phase margin is required to support the increased gain in the feedback path. Model 429 is optimized for phase margin in the multiply and divide modes producing minimum vector errors at high frequencies. To avoid the potential problem of instability, the RC network shown previously is recommended. This network restricts the bandwidth and guarantees stability for all positive values of Z.

OPTIONAL ADJUSTMENT PROCEDURE – SQUARE ROOT

1. Apply a voltage to the Z terminal equal to the lowest anticipated input voltage.
2. Adjust R_0 such that $e_0 = -\sqrt{10Z}$, where Z is the voltage applied in step 1.

DIVISION SPECIFICATIONS (TYPICAL)

OUTPUT FUNCTION	10(Z)/X
Numerator Range	±10V
Denominator Range, 1% Accuracy	-1 to -10V
Denominator Range, 5% Accuracy	-0.2V to -10V
Bandwidth Formula, (Hz, -3dB)	(8MHz)(X)/10

SQUARE ROOTING SPECIFICATIONS (TYPICAL)

OUTPUT FUNCTION	$-\sqrt{10(Z)}$
Dynamic Range	1000 to 1 (+0.010V ≤Z≤+10V)
Accuracy (% of Full Scale)	0.5%
Bandwidth Formula, (Hz, -3dB)	(5MHz) $\sqrt{\lvert X\rvert/10}$

Table 1. Division & Square Rooting Specifications

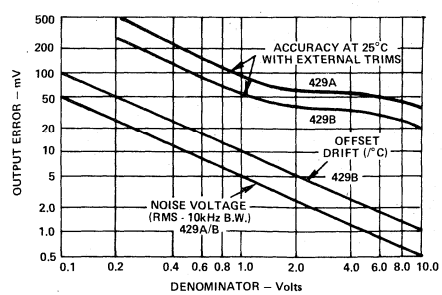
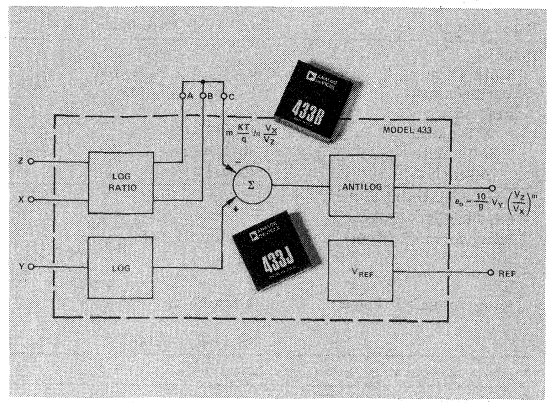


Figure 3. Typical Error Performance of Model 429 in Divide Mode for Worst Case of $|e_0| = 10V$

ANALOG DEVICES

Programmable Multifunction Module

MODEL 433



FEATURES

Versatility: Provides Transfer Characteristics of Several Function Modules
Divides Over a 100:1 Range With a Max Error of 0.25% (433B)
Internal Voltage Reference
Hermetically Sealed Semiconductors
No External Trims Required
Low Cost

APPLICATIONS

Transducer Linearization
Signal Processing
Raising to Arbitrary Powers
Vector Functions
Trigonometric Functions (Sine, Cosine, Arctangent)

GENERAL DESCRIPTION

The model 433 is an extremely versatile function module which implements the transfer function:

$$e_o = \frac{10}{V_{REF}} V_y \left(\frac{V_z}{V_x}\right)^m, \quad 0.2 \leqslant m \leqslant 5.0$$

V_{REF} = +9.0 Volts

By either jumper connections on the pins, or selection of two external resistors the user can program the 433 to: multiply, divide, square, square root, root of a ratio, square of a ratio, or raise voltage ratios to an arbitrary power, *m*.

When used with a low cost op amp, such as AD741, the model 433 may be used to compute the true rms value of a varying signal. With two such op amps, the 433 can be used to perform accurate vector computations over wide ranges of the vector sum.

Due to its log/antilog circuit approach, signal levels of 100mV to 10V may be processed with a maximum output error of 0.25% F.S. (433B). The allowable input range for the three input variables is 0.01 to +10V, for which there is a typical error of ±5mV ±0.3% of the theoretical output voltage for model 433J, and ±1mV ±0.15% for 433B.

Because of its small size, accuracy, versatility, and speed (and all at low cost), the model 433 will prove to be an essential component in equipment requiring on-the-spot computations in real time, or for linearizing a wide range of transducer characteristics in medical, industrial, and process control equipment. Designed with the OEM's needs in mind, the model 433 is attractively priced for new equipment designs.

PRINCIPLE OF OPERATION

The model 433 is comprised of log and antilog circuits interconnected as shown in Figure 1. The log ratio circuit provides

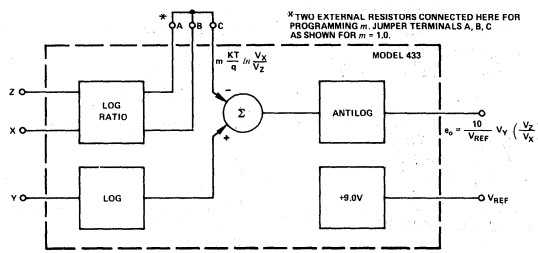


Figure 1. Functional Block Diagram

the log of V_x/V_z to terminals A, B, C where, for exponents other than unity, it is scaled by two external programming resistors (see hook-up diagrams for connection and values of these two resistors). The scaled log ratio from terminal C is subtracted from a signal proportional to the log of V_y. The resulting expression is operated on by the antilog circuit, yielding an output of

$$e_o = \frac{10}{V_{REF}} V_y \left(\frac{V_z}{V_x}\right)^m, \quad V_{REF} = +9.0 \text{ Volts}$$

The voltage reference circuit is a high stability (0.005%/°C) voltage source which is generated internally. It is provided as an output terminal for user convenience, and may be used as a constant at any of the input terminals.

ONE-QUADRANT DIVIDER

When connected as a divider, the model 433B has less than ¼% output error over an input signal range of 100:1. This performance is obtained with no external trims, and is nearly twenty times better than that attainable with a 0.1% multiplier/divider connected in a feedback loop.

SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

Model	433J	433B
Transfer Function	$e_o = +\frac{10}{V_{REF}} V_y \left(\frac{V_z}{V_x}\right)^m$	*
Reference Terminal Voltage[1]		
V_{REF} (Internal Source)	+9.0V ±5% @ 1mA	*
vs Temp, Rated	±0.005%/°C	*
Rated Output[1]	+10.5V @ 5mA, min	*
Input		
Signal Range	$0 \leqslant V_x, V_y, V_z \leqslant +10V$,	*
Max Safe Input	$V_x, V_y, V_z \leqslant \pm 18V$	*
Resistance		
X Terminal	100kΩ ±1%	*
Y Terminal	90kΩ ±10%	*
Z Terminal	100kΩ ±1%	*
External Adjustment of the Exponent, m		
Range for m <1 (Root)	$1/5 \leqslant m < 1$, $m = \frac{R_2}{R_1 + R_2}$	*
Range for m > 1 (Power)	$1 \leqslant m < 5$, $m = \frac{R_1 + R_2}{R_2}$	*
	$(R_1 + R_2) \leqslant 200\Omega$	*
Accuracy (Divide Mode, m = 1, $V_y = V_{REF}$)[2,3]		
Total Output Error @ +25°C (for specified input range)		
Typical (RTO)	±5mV ±0.3% of output	±1mV ±0.15% of output
Max Error (RTO)	±50mV	±25mV
Input Range ($V_z \leqslant V_x$)	0.01V to 10V, V_z	*
	0.1V to 10V, V_x	*
Over Specified Temp. Range	±1%	±1% max
Output Offset Voltage (Not Adjustable)		
Initial @ +25°C	±5mV	±2mV max
Offset vs Temp.	±1mV/°C	±1mV/°C max
Noise, 10Hz to 1kHz		
V_x = +10V	100μV rms	*
V_x = +0.1V	500μV rms	*
Bandwidth, V_y, V_z		
Small Signal (-3dB), 10%		
of dc Level	V_y or V_z	*
$V_y = V_z = V_x$ = 10V	100kHz	*
$V_y = V_z = V_x$ = 1V	20kHz	*
$V_y = V_z = V_x$ = 0.1V	1kHz	*
$V_y = V_z = V_x$ = 0.01V	400Hz	*
Full Output (V_y or V_z = 5V dc, ±5V ac)	(V_x) x (5kHz)	*
Power Supply Range		
Rated Performance	±15V dc @ 10mA	*
Operating	±(12 to 18)V dc	*
Temperature Range		
Rated Performance	0 to +70°C	-25°C to +85°C
Storage	-55°C to +125°C	-55°C to +125°C
Mechanical		
Case Size	1.5" x 1.5" x 0.62"	*
Mating Socket	AC1038	*

*Same specifications as 433J.

[1] Terminals short circuit protected to ground.

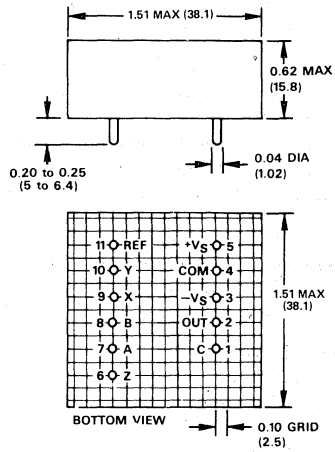
[2] Accuracy is specified in divide mode. Input range is 10mV to 10V for specified accuracy when connected as a multiplier.

[3] Error is defined as the difference between the measured output and the theoretical output for any given pair of specified input voltages.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

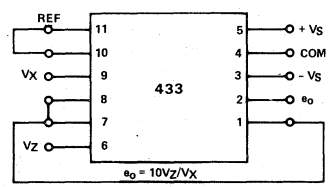


Mating Socket AC1038

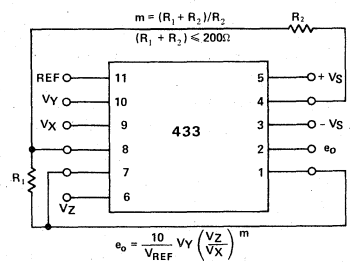
WIRING CONNECTIONS

Bottom View Shown in All Cases

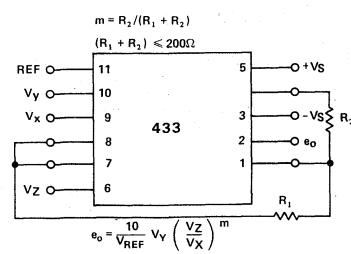
DIVIDE MODE (m = 1, $V_y = V_{REF}$)



POWERS m ⩾ 1



ROOTS m ⩽ 1



MODEL 433B – 0.25% DIVIDER, WIDE DYNAMIC RANGE

Probably the most impressive performance improvement owing to model 433's log/antilog circuit approach, is its ability to hold high divider accuracies over a wide 100:1 input signal range.

When using a conventional multiplier/divider as a divider, accuracy, offset drift, and noise performance are all degraded as the denominator is decreased.

For model 433, accuracy, offset drift, and noise performance are all virtually independent of denominator level as illustrated in Figure 2 and this performance is obtained with no external trims.

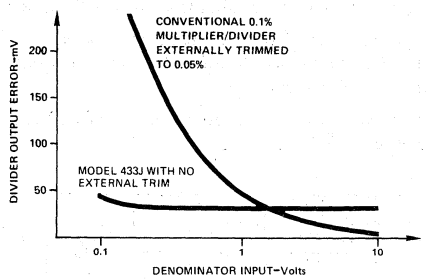


Figure 2. Comparison of Divider Error vs. Denominator Level for Model 433J and a Conventional Mult./Div.

FREQUENCY RESPONSE

A curve of amplitude vs. bandwidth for model 433 is shown in Figure 3. For all input terminals, the small signal frequency response (-3dB point) is signal level dependent, decreasing from 100kHz for a 10V input to 400Hz for a 10mV input. These small signal measurements are made by superimposing a 10% small signal amplitude on the dc level being characterized.

Full output for a ±5 volt signal superimposed on a 5V dc level is 50kHz for the multiplier, and V_X x 5kHz for the divider.

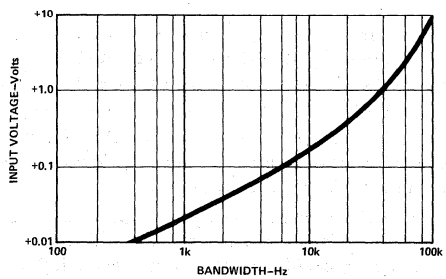


Figure 3. 433 Small Signal Bandwidth vs. Input Voltage

VARYING THE EXPONENT, m

Presented in Figure 4 is a family of curves which illustrates the effect of varying the exponent, m. All curves have been scaled for the full scale output of 10V by reducing the 433's transfer equation to $e_O = 10\ (V_Z/V_X)^m$. For applications where a continuous variation in m is desired, connections should be made as shown in Figure 5C. Model 433 features very small accuracy changes (≈0.1%) as m is adjusted over the entire range from 0.2 to 5.

Various values of m are programmed by two external resistors, R_1 and R_2. For values of $m < 1$ resistor connections are made

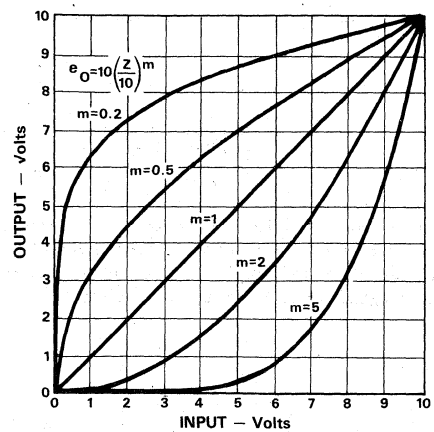


Figure 4. Varying the Exponent, m

to terminals, 1, 7, 8 as shown in Figure 5A. For values of $m > 1$, see Figure 5B. For $m = 1$, connect terminals 1, 7 and 8 together.

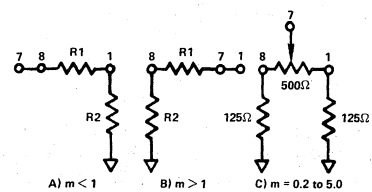


Figure 5. Resistor Programming for the Exponent, m

NOISE PERFORMANCE

The curves shown in Figure 6 are for output noise vs. signal level in a 1kHz BW for worst case conditions. These conditions exist when V_X is equal to V_Z and is varied over the specified range. It should be noted that for 0.1V inputs the effective gain is 100. To retain the full performance capability of model 433, all external noise sources should be isolated from the input terminals.

An exceptional advantage of the 433 over other means of dividing is revealed by these curves. That feature being that noise is virtually independent of signal level. For a 100:1 signal level change of the denominator, the output noise is changed only 3:1. Division by using a multiplier in the feedback loop exhibits a 100:1 increase in output noise for a denominator signal level change of 100:1.

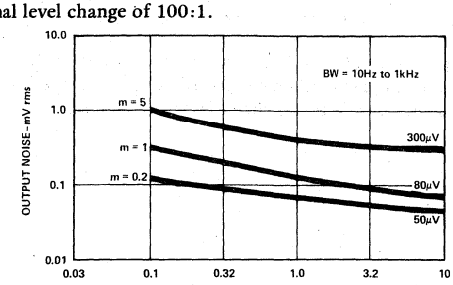


Figure 6. Model 433 Noise vs. Denominator for Various Exponents, m

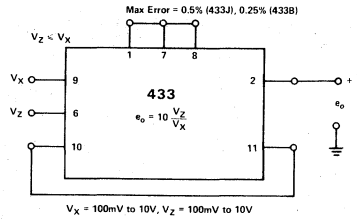


Figure 7. Divider

When connected as a divider as shown above, the 433 has less than ½% error (50mV) for input signals from 100mV to 10V. Output noise, offset drift and accuracy are all virtually independent of signal level and no trims are required.

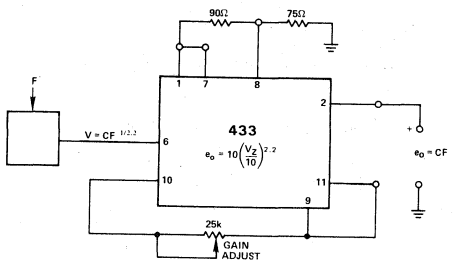


Figure 8. Transducer Linearization

A transducer's output may be linearized by utilizing the 433 as an exponentiator. In the example above, a transducer is used to convert a force, F, to a voltage, V. The desired relationship being V directly proportional to F; i.e., V = CF where C is constant.

The actual output for this example is proportional to F, but is a nonlinear relation which can be approximated by $CF^{1/2.2}$. Connecting the 433 as shown with m = 2.2 provides the desired relation of e_O = CF.

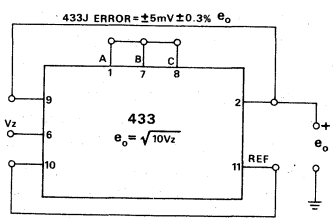


Figure 9. Square Root

The square root of a single variable may be obtained with no external components when connected as shown above. Noise performance is even better than that for the multiply or divide mode.

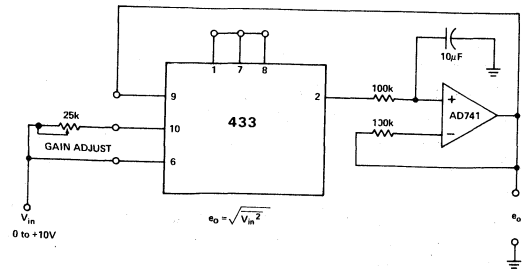
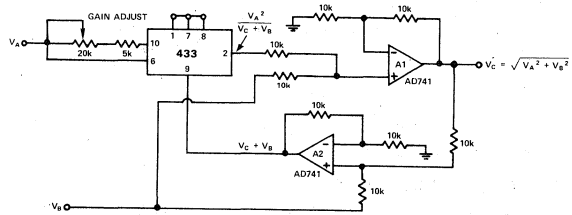


Figure 10. True rms

By combining the 433 with a simple filter, using an external op amp as shown above, the true rms value of a one quadrant input signal may be computed. Accuracy is not degraded by crest factor, provided the maximum input is 10V or less.

The 433 output is applied to an integrator to average the signal and is then fed back to the X input to obtain the square root of the mean square of the input.

Accuracy of 5mV + 0.1% of reading may be achieved over an input range of 500:1.



$V_C = \sqrt{V_A^2 + V_B^2}$

$V_C^2 = V_A^2 + V_B^2$

$V_A^2 = V_C^2 - V_B^2$

$V_A^2 = (V_C - V_B)(V_C + V_B)$

$\frac{V_A^2}{V_C + V_B} = (V_C - V_B)$

$V_C = \frac{V_A^2}{V_C + V_B} + V_B$

Figure 11. Vector Computation $V_C = \sqrt{V_A^2 + V_B^2}$

The vector computation circuit shown in Figure 11 illustrates the extreme versatility of model 433. Used with two inexpensive op amps the 433 is used as a basic building block, which in this case, provides the square root of the sum of the squares.

This application is based on the identity for the difference of squares. The derivation is shown by the equations above and the final equation for V_C is implemented.

Due to the excellent inherent accuracy of the above circuit (error = 0.1% of reading), matched resistors with a low T.C. should be used. Errors of only 0.1% of the theoretical output may be achieved over signal levels of +100mV to +10V.

The usefulness of model 433 extends beyond the illustrative examples shown above. Model 433 may also be used to generate basic trigonometric functions (sine, cosine, arctangent). Further detailed applications information on model 433 is provided in the Nonlinear Circuits Handbook, published by Analog Devices.

ANALOG DEVICES

High Accuracy, Two Quadrant Analog Divider

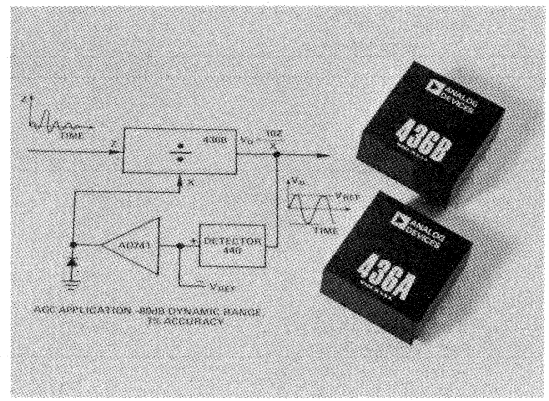
MODEL 436

FEATURES

- Two Quadrant: Numerator Range: ±10V
- High Accuracy: 0.5% max (436A), 0.25% max (436B) over 100:1 Dynamic Range
- No Trimming Required to Achieve Rated Accuracy
- 1000:1 Denominator Range: With External Trim
- Low Nonlinearity: 0.05% (436B)
- Low Harmonic Distortion: -66dB (436B)
- All Hermetically-Sealed Semiconductors
- Wide Operating Temperature Range, -25°C to +85°C

APPLICATIONS

- Linear Gain Control (80dB Range)
- Transducer Linearization
- Instrumentation Calculation
- Adaptive Process Control



GENERAL DESCRIPTION

Model 436 is a precision, two-quadrant variable transconductance analog divider featuring guaranteed accuracy of ±0.5% (model 436A) and ±0.25% (model 436B) over a 100:1 denominator signal range (100mV to 10V) with no external adjustments. With the use of optional external trimming, accuracy may be improved to ±0.05% (436B) over a 1000:1 denominator signal range (10mV to 10V). In addition to this excellent accuracy, model 436 offers a small signal bandwidth (-3dB) of 300kHz and typical numerator nonlinearity of less than ±0.05% (5Hz to 30kHz).

Through the use of hermetically-sealed semiconductors, the model 436 affords exceptional reliability over a wide operating temperature range (-25°C to +85°C). This compact (1.5" x 1.5" x 0.6") epoxy module provides further reliability by protecting the output against damage due to short circuits to ground. The model 436 is pin compatible with most modular multipliers. This allows the model 436 to replace inverted multiplier type dividers in existing sockets to give improved accuracy and increased dynamic range.

TWO QUADRANT OPERATION

Dividers are generally available as single and two-quadrant devices. Dividers that are formed by closing the loop around a four-quadrant transconductance multiplier are capable of operating in two quadrants. Unfortunately, because of the feedback around the multiplier, these dividers suffer from errors which increase directly as the denominator decreases. Even using 0.1% multipliers, these errors become large as the denominator becomes small and high performance is possible only over a limited range of input levels. This denominator dependency of divider errors can be greatly reduced by application of log-antilog techniques, as in the model 434 that has a 0.25% accuracy for denominators within 0.1 to 10V. However, while dividers that use log-antilog circuits are inherently more accurate than inverted multiplier devices, they are limited to single-quadrant operation by the nature of the log function.

The model 436 employs a unique log-antilog circuit to provide two-quadrant operation with high accuracy over a very wide range of denominators (refer to Figure 1).

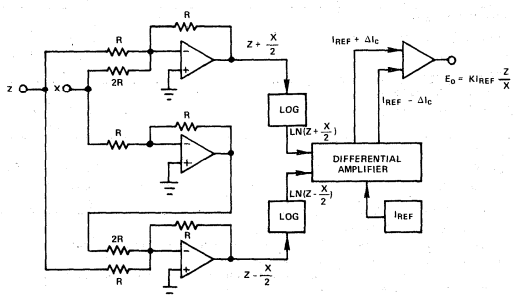


Figure 1. Model 436 Functional Block Diagram

For detailed information, contact factory.

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

MODEL		436A	436B
TRANSFER FUNCTION	$\|V_Z\| \leqslant V_X; V_X > 0$	$e_O = 10V_Z/V_X$	*
ACCURACY[1]			
Total Output Error, @ +25°C	$\|V_Z\| \leqslant 10V$		
No External Trim	$+0.1 \leqslant V_X \leqslant +10V$	±0.5%, max	±0.25%, max
External Trim	$+0.1 \leqslant V_X \leqslant +10V$	±0.3%, max	±0.1%, max
Over Temperature	$+0.1 \leqslant V_X \leqslant +10V$		
No External Trim	0 to +70°C	±2.0%, max	±1.0%, max
No External Trim	-25°C to +85°C	±4.0%, max	±2.0%, max
Vs. Supply Voltage		±0.02%/%	*
Warm Up Time to Rated Performance		5 Minutes	*
NONLINEARITY	$\|V_Z\| V_X$, $+0.1 \leqslant V_X \leqslant +10V$	±0.15% max (0.1% typ)	±0.1% max (0.05% typ)
RATED OUTPUT[2]			
Voltage		±10V, min	*
Current		±5mA, min	*
Resistance		0.1Ω	*
Capacitance Load		0 to 1000pF, min	*
INPUT SPECIFICATIONS			
Voltage, Numerator Signal (V_Z)	$\|V_Z\| \leqslant V_X$	±10V	*
Voltage, Denominator (V_X)	$V_X > 0$	+10V	*
Safe Input Voltage, V_Z and V_X		$\pm V_S$, max	*
Offset Voltage, @ +25°C, V_Z and V_X		±100μV	*
vs. Temperature	-25°C to +85°C, V_Z, V_X	±20μV/°C	*
vs. Supply Voltage, V_Z and V_X		±30μV/%	*
External Trim Adjustment Range, V_Z		±4.5mV	*
External Trim Adjustment Range, V_X		±1.5mV	*
Voltage Noise, 10Hz to 10kHz, V_X and V_Z		15μV, rms	*
INPUT IMPEDANCE			
Numerator, V_Z		9kΩ, ±2%	*
Denominator, V_X		25kΩ, ±1%	*
OUTPUT SPECIFICATIONS[3]			
Offset Voltage, @ +25°C, V_X = +10V		±10mV	*
vs. Temperature -25°C to +85°C, V_X = +10V		±500μV/°C	*
vs. Supply Voltage		±50μV/%	*
External Trim Adjustment Range		±20mV	*
Voltage Noise, 10Hz to 10kHz V_X = +10V		200μV, rms	*
10Hz to 300kHz, V_X = +10V		750μV, rms	*
FREQUENCY RESPONSE			
Small Signal, -3dB,	$+0.1 \leqslant V_X \leqslant +10V$	300kHz	*
Full Power	$+0.1 \leqslant V_X \leqslant +10V$	30kHz	*
Slew Rate	$+0.1 \leqslant V_X \leqslant +10V$	2V/μs	*
Settling Time, to ±0.5%, ±10 Volt Step, V_X = +10V		10μs	*
Settling Time, to ±0.5%, ±10 Volt Step, V_X = +0.1V		10μs	*
Overload Recovery, $+0.1 \leqslant V_X \leqslant +10V$		5μs	*
POWER SUPPLY[4]			
Voltage, Rated Performance		±15V dc	*
Voltage, Operating		±(12 to 18)V dc	*
Current, Quiescent		±9mA	*
TEMPERATURE RANGE			
Rated Performance		-25°C to +85°C	*
Storage		-55°C to +125°C	*
MECHANICAL			
Case Size		1.5" x 1.5" x 0.62"	*
Mating Socket		AC-1041	*
Weight, grams		36	*

*Specifications same as model 436A.

[1] Error is specified as a percentage of full scale output where full scale output is 10 volts.

[2] Output is protected for short circuits to ground, indefinite.

[3] Output offset is specified with no external trimming; optional 50kΩ potentiometer may be connected to zero the output offset voltage.

[4] Recommended power supply; model 904, ±15V @ 50mA output.

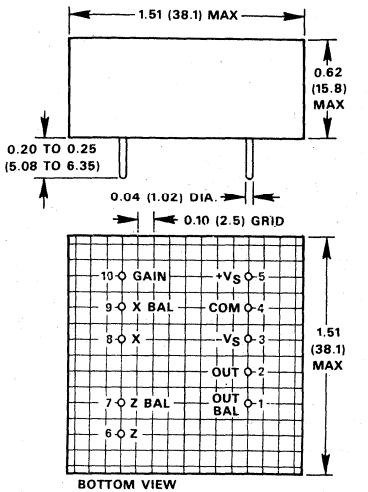
Specifications subject to change without notice.

NONLINEAR CIRCUITS HANDBOOK

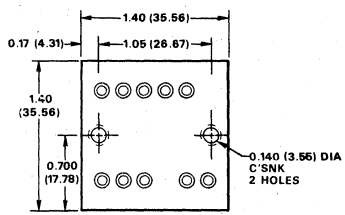
The Nonlinear Circuits Handbook, available from Analog Devices, is an invaluable source of information on principles, circuitry, performance specifications, testing and application of the class of devices designed for use in nonlinear applications. This text provides you with all the fundamentals and guidelines necessary for the proper selection and use of function modules.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



MATING SOCKET AC-1041



WIRING CONNECTIONS

Bottom View Shown in all Cases

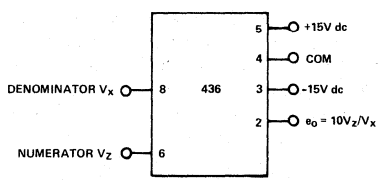


Figure 2. Divide Mode Connections

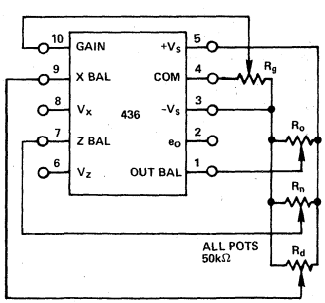


Figure 3. Optional Trim Connections

RMS-to-DC Converters

Contents

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General Information and Definitions of Specifications	7–4
442J/K/L 8MHz-Bandwidth rms-to-dc Converters	7–7

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Selection Guide
RMS-to-DC Converters

Model	Characteristics	Vol I Page	Vol II Page
AD536AJ/AK/AS	Monolithic IC rms/dB converter. Laser-wafer-trimmed for total max error ±2mV ±0.2% of reading (AD536AK), sine waves at 1kHz (20kHz typ), 0 to 7V rms. Crest factor of 7 for 1% additional error. ±3dB bandwidth 2MHz (1V<V_{IN}≤7V). Averaging time constant per μF of C_{ext}, 25ms/μF. Total-error tempco (±50μV ±0.005% rdg)/°C max (AK). Additional features include dB output with 60dB range, single-or dual-supply operation, and low power consumption – 1mA. AD536AJ/K are specified for 0 to +70°C, AD536AS for -55°C to +125°C.	7-7	–
AD636J/K	Monolithic IC rms/dB converter. Laser-wafer-trimmed for total max error ±0.2mV ±0.5% of reading (AD636K), 0 to 200mV rms. Crest factor of 6 for 0.5% additional error. ±3dB bandwidth 1.3MHz (200mV). Averaging time constant per μF of C_{ext}, 25ms/μF. Total-error tempco (±0.1μV ±0.005% rdg/°C) max. Additional features include dB output with 60dB range, single-or dual-supply operation, and low power consumption – 1mA.	7-13	–
442	A high performance true rms/dc converter featuring 8MHz bandwidth, low drift to ±3.5μV/°C ±0.01% of reading/°C maximum, and ±1% of reading error to 800kHz.	7-19	7-7

7

Orientation
RMS-to-DC Converters

The 442 is a high-accuracy wide-bandwidth true-rms-to-dc-conversion module. As the Selection Guide indicates, additional devices to perform rms-to-dc conversion, employing IC technology, may be found in Volume I. Devices of this class compute the instantaneous square of the input signal, average it, and take the square root of the result, to provide a dc voltage that is proportional to the rms of the input (and, in the case of the AD536A and AD636 ICs, an auxiliary dc voltage that is proportional to the *log* of the rms, for dB measurements).

Excellent pre-trimmed performance, improvable by simple optional trims, makes these devices ideal for all types of laboratory and OEM rms instrumentation where amplitude measurements must be made with high accuracy, independently of waveshape.

An alternative to rms that has been widely used in the past, principally for measurements on sine waves, is mean absolute-deviation, or "ac average." It is performed by taking the absolute value of (i.e., full-wave or half-wave rectifying) a signal, filtering it, and scaling it by the ratio of rms to m.a.d. for sine waves, 1.111, so that it reads correctly (for undistorted sine waves). Unfortunately, this ratio varies widely as a function of the waveform and will give grossly incorrect results in many cases. The table shows a few representative examples comparing rms with m.a.d.

Examples of applications include noise measurement – for example, thermal noise, transistor noise, and switch-contact noise. True-rms measurement is a technique that provides consistent theoretically valid measurements of noise amplitude (standard deviation) from different sources having different properties.

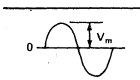
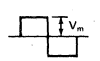
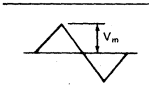
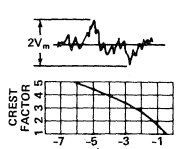
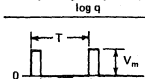
True-rms devices are also useful for measuring electrical signals derived from mechanical phenomena, such as strain, stress, vibration, shock, expansion, bearing noise, and acoustical noise. The electrical signals produced by these mechanical actions are often noisy, non-periodic, nonsinusoidal, and superimposed on dc levels, and require true-rms for consistent, valid, accurate measurements. RMS converters are also useful for accurate measurements on low-repetition-rate pulse-trains having high *crest factors* (ratio of peak to rms), and for measurements of the energy content of SCR waveforms at differing firing angles.

The basic approach used in these converters for computing the rms is to take the absolute value, square it, and divide by the fed-back output (using the logarithmic characteristics of transistor junctions), and filter the result. The resulting approximation

$$E_o = \text{Avg.}\left[\frac{V_{in}^2}{E_o}\right] \cong \sqrt{\text{Avg.}\,(V_{in}^2)}$$

is valid if the averaging time-constant is sufficiently long compared with the periods of the lowest-frequency ac components of the signal.

The simplest form of averaging involves a single-pole filter, using an external filtering capacitance. Increased values of capacitance for filtering will improve the accuracy for low frequency rms measurements and provide reduced ripple at the output, but at the cost of increased settling time. For fastest settling and minimum ripple, an additional stage of 2-pole filtering is useful. The additional filtering permits improvement of settling time or reduction of ripple (or both) because of substantial reduction of C_{ext}.

WAVEFORM		RMS	MAD	RMS/MAD	CREST FACTOR
	SINE WAVE	$\frac{V_m}{\sqrt{2}}$ 0.707 V_m	$\frac{2}{\pi}V_m$ 0.637 V_m	$\frac{\pi}{2\sqrt{2}}$ = 1.111	$\sqrt{2}$ = 1.414
	SYMMETRICAL SQUARE WAVE OR DC	V_m	V_m	1	1
	TRIANGULAR WAVE OR SAWTOOTH	$\frac{V_m}{\sqrt{3}}$	$\frac{V_m}{2}$	$\frac{2}{\sqrt{3}}$ = 1.155	$\sqrt{3}$ = 1.732
	GAUSSIAN NOISE CREST FACTOR IS THEORETICALLY UNLIMITED. q IS THE FRACTION OF TIME DURING WHICH GREATER PEAKS CAN BE EXPECTED TO OCCUR	RMS	$\sqrt{\frac{2}{\pi}}$ RMS = 0.798 RMS	$\sqrt{\frac{\pi}{2}}$ 1.253	C.F. / q 1 / 32% 2 / 4.6% 3 / 0.37% 3.3 / 0.1% 3.9 / 0.01% 4 / 63ppm 4.4 / 10ppm 4.9 / 1ppm 6 / 2x10⁻⁹
	PULSE TRAIN η / MARK/SPACE 1 / ∞ 0.25 / 0.3333 0.0625 / 0.0667 0.0156 / 0.0159 0.01 / 0.0101	$V_m\sqrt{\eta}$ V_m 0.5V_m 0.25V_m 0.125V_m 0.1V_m	$V_m\eta$ V_m 0.25V_m 0.0625V_m 0.0156V_m 0.01V_m	$\frac{1}{\sqrt{\eta}}$ 1 2 4 8 10	$\frac{1}{\sqrt{\eta}}$ 1 2 4 8 10

PERFORMANCE SPECIFICATIONS

Considerable information regarding rms-to-dc converter circuit design, performance, selection, and applications is to be found in the NONLINEAR CIRCUITS HANDBOOK.[1] In addition, useful applications information on auxiliary filtering can be found in the article "Measure RMS with Less Ripple in Less Time."[2]

The most-salient feature of a true rms-to-dc converter is that *it ideally has no error due to an indirect approximation to the rms.* Static errors are due only to scale-factor, linearity, and offset errors; dynamic errors are due to insufficient averaging time at the low end and finite bandwidth and slewing rate at the upper end. Linearity errors affect crest factor in midband. Dynamic errors are also a function of signal amplitude, due in part to the variation of bandwidth of the "log" transistors with signal level.

Total Error A specification for quick reference, this is the maximum deviation of the dc component of the output voltage from the theoretical output value over a specified range of signal amplitude and frequency. It is shown as the sum of a fixed error and a component proportional to the theoretical output ("% of reading"). It is specified for a sinusoidal input in a given frequency and amplitude range. The fixed error-component includes all offset errors and irreducible nonlinearities; the %-of-reading component includes the linear scale-factor error.

Total Error, external adjustment is the amount by which the output may differ from the theoretical value when the output offset and scale factor have been trimmed. Note that the fixed error-component cannot be reduced to zero, even though the output offset can be nulled at zero input. This is because of residual input offsets and inherent nonlinearities in the converter.

Total Error vs. Temperature is the average change of %-of-full-scale error component plus the average change of percent of reading error component per degree Celsius, over the rated temperature range.

Frequency for 1%-of-Reading Error is the minimum value of frequency (at the high end) at which the error increases from the midband value by 1% of reading. It is a function of peak-to-peak input amplitude.

Frequency for -3dB Reading Error is the minimum value of frequency (at the high end) at which the error may equal -30% of reading. It is a function of amplitude.

Crest Factor (a property of the signal) is the ratio of peak signal voltage to the ideal value of rms; the specified value of crest factor is that for which the error is maintained within specified limits at a given rms level for a worst-case — rectangular pulse — input signal.

Filter Time Constant and External Capacitor: The time constant of the internal averaging filter, and the increase of time constant per μF of added external capacitance.

Input: The voltage range over which specified operation is obtained, the maximum voltage for which the unit operates, the maximum safe input voltage, and the effective input resistance.

Output: The maximum output range for rated performance, the minimum current guaranteed available at full-scale output voltage, and the source resistance of the output circuit.

Power Supply: Power-supply range for specified performance, power-supply range for operation, and quiescent current drain.

Temperature Range: The range of temperature variation for operation within specifications. Temperature coefficients are determined by three-point measurements ($T_H - 25^\circ C$), ($25^\circ C - T_L$), when measured.

[1] *Nonlinear Circuits Handbook,* Analog Devices, Inc., 1974, 1976, 536pp, edited by D. H. Sheingold, $5.95; send check or complete MasterCard data to P.O. Box 796, Norwood, MA 02062

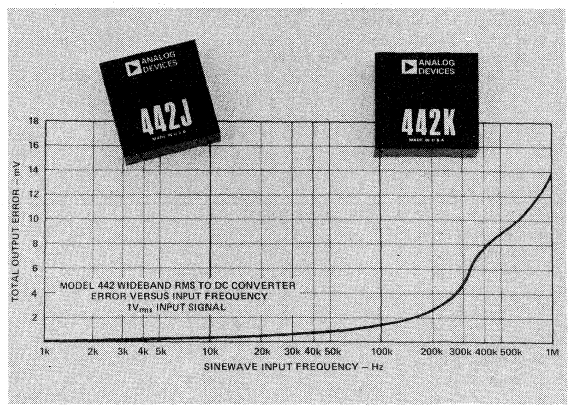
[2] ANALOG DIALOGUE 9-3, 1975, pp 21-22

Wideband, High Accuracy True rms-to-dc Converter

MODEL 442

FEATURES
- DC to 8MHz Response (-3dB)
- High Accuracy:
  - With No Ext. Trim: ±2mV ±0.15% of Rdg., max
  - With Ext. Trim: ±1mV ±0.05% of Rdg., max
- Low Drift: ±(35μV ±0.01% of Reading)/°C max, 442L
- Fast Settling Time: 5ms to 1%
- Small Size: 1.5" x 1.5" x 0.4"
- All Hermetically Sealed Semiconductors

APPLICATIONS
- Wideband rms Instrumentation
- Telephone, Telegraph & Modem Test Equipment
- Vibration Analysis
- Sound & Noise Level Instrumentation
- Mean Square Measurements



7

GENERAL DESCRIPTION

Model 442 is a high performance true rms-to-dc converter featuring 8MHz bandwidth, low drift to ±35μV/°C ±0.01% of reading/°C maximum, and ±1% reading error to 800kHz. Unlike competing designs, model 442 achieves its high accuracy over a very wide input signal range. With no external adjustment, accuracy is held to within ±2mV ±0.15% of reading for input signals of 0 to 2V$_{rms}$. If optional adjustments are performed, this accuracy can be improved to ±1mV ±0.05% of reading. Model 442 is designed to be used in high performance instrumentation where response to low level, high speed signals, is of greatest importance.

The compact, log-antilog circuit design of model 442 results in high accuracy measurements on sinewave signals and complex waveforms such as pulse trains. Reading error increases 0.2% for signals with crest factors up to 7. In addition, true rms measurement can be performed directly on signals containing both ac and dc components.

Model 442 is available in three low drift selections offering maximum drift performance over 0 to +70°C range; model 442L: ±(35μV ±0.01% of rdg.)/°C max; model 442K: ±(50μV ±0.01% of rdg.)/°C max; model 442J: ±(100μV ±0.01% of rdg.)/°C max.

WHERE TO USE MODEL 442

Excellent untrimmed performance along with simple, optional trims make model 442 the ideal component for all types of laboratory and OEM rms instrumentation where wideband measurements must be made with high accuracy. Model 442 is ideally suited for measuring thermal noise, transistor noise and switch contact noise. True rms measurement is the only technique to accurately measure system noise and thereby assist the designer in reducing this noise. Model 442 is also useful for measuring mechanical phenomena such as strain, stress, vibration, shock, expansion and contraction. The electrical signals produced by these mechanical actions are often noisy, nonperiodic, nonsinusoidal and superimposed on dc levels, therefore requiring true rms devices for accurate measurements.

Model 442 is also required for accurate measurements on low repetition rate pulse trains. For pulse trains with crest factors of 10, a 3dB bandwidth of 400 times the pulse rate is required to achieve 1% accuracy and 4000 times the pulse rate is needed for 0.1% accuracy.

Model 442 may also be connected (see Figure 3) to measure the MEAN SQUARE of a signal ($e_o = e_{in}^2/V_R$). The Mean Square of a random signal is equal to the variance (σ^2).

TOTAL ACCURACY

Total output error is specified as the sum of two components; a fixed term plus a percentage of output signal. Model 442 has a rated sinewave accuracy of ±1mV ±0.05% max (externally trimmed), which for a one volt rms sinewave, results in a ±1.5mV maximum error (±1mV fixed error plus ±0.5mV reading error). The fixed error component is comprised of output offsets and linearity errors. Both of these error terms have been minimized in the model 442 as a result of special output circuit design and sophisticated factory offset trim procedures. Output offset can be adjusted for minimum error by means of an external adjustment (see Figure 2). The % of reading error is attributed to nonlinearity and scale factor errors. Scale factor error may also be reduced by external adjustment of an optional 5kΩ potentiometer (see Figure 2).

For detailed information, contact factory.

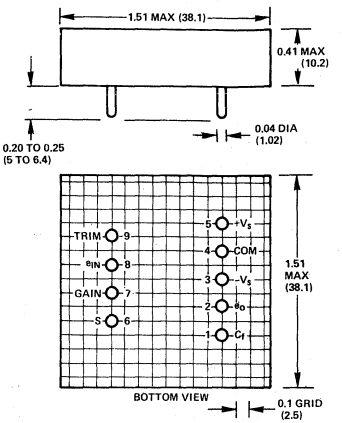
SPECIFICATIONS** (typical @ +25°C and V_S = ±15V dc, unless otherwise noted)

MODEL	442J	442K	442L
TRANSFER EQUATION	$e_O = \sqrt{avg\ (e_{in})^2}$	*	*
ACCURACY[1]			
Total Error, Sinewave Input, f ≤ 20kHz			
No External Adjustment			
Input Range: 0 to $2V_{rms}$	±2mV ±0.15% of Rdg., max	*	*
External Adjustment			
Input Range: 0 to $2V_{rms}$	±1mV ±0.05% of Rdg., max	*	*
$10mV_{rms}$ to $2V_{rms}$	±0.5mV ±0.05% of Rdg., max	*	*
Additional Error, Sinewave Input, 20kHz ≤ f ≤ 500kHz			
With or Without External Adjustment			
For Any Input Range	$(\pm 25\mu V \pm 0.0025\%\ of\ Rdg) \times \left(\frac{f(kHz) - 20kHz}{1kHz}\right)$, max	*	*
vs. Temperature (0 to +70°C), max	±100µV/°C plus ±0.01% of Rdg./°C	±50µV/°C plus ±0.01% of Rdg./°C	±35µV/°C plus ±0.01% of Rdg./°C
vs. Supply Voltage	±0.1mV/%	*	*
Warm-Up Time	5 minutes	*	*
FREQUENCY RESPONSE, SINEWAVE INPUT			
±1% Reading Error			
Input: $7V_{rms}$	500kHz	*	*
$2V_{rms}$	700kHz	*	*
$1V_{rms}$	800kHz	*	*
$0.2V_{rms}$	120kHz	*	*
$0.1V_{rms}$	80kHz	*	*
$0.01V_{rms}$	25kHz	*	*
-3dB Reading Error			
Input: $7V_{rms}$	5MHz	*	*
$2V_{rms}$	8MHz	*	*
$1V_{rms}$	7MHz	*	*
$0.2V_{rms}$	3MHz	*	*
$0.1V_{rms}$	2MHz	*	*
$0.01V_{rms}$	300kHz	*	*
Internal Filter Time Constant	1.5ms	*	*
External Filter Time Constant[2]	15ms/µF	*	*
Total Averaging Time Constant[2]	1.5ms + 15ms/µF	*	*
CREST FACTOR			
±0.2% Additional Reading Error	7	*	*
±0.5% Additional Reading Error	10	*	*
INPUT SPECIFICATIONS			
Voltage			
Signal Range	$\pm 10V_{peak}$ min	*	*
Safe Input	$\pm V_S$	*	*
Impedance	2.5kΩ ±10%	*	*
OUTPUT SPECIFICATIONS[3]			
Rated Output			
Voltage	+10.0V min	*	*
Current	+5mA min	*	*
Impedance	0.1Ω	*	*
Offset Voltage, @ +25°C	±2mV max	*	*
With External 20kΩ Trim Pot	Adjustable to Zero	*	*
POWER SUPPLY[4]			
Voltage, Rated Specifications	±15V dc	*	*
Voltage, Operating	±(6 to 18)V dc	*	*
Current, Quiescent	±12mA	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	*
Operating	-25°C to +85°C	*	*
Storage	-55°C to +125°C	*	*
CASE SIZE	1.5" x 1.5" x 0.4"	*	*

*Specifications same as model 442J.
**Contact sales office for complete 4 page data sheet.
[1] Error is specified as the sum of two components: a fixed term plus a percentage of output signal (reading). Refer to TOTAL ACCURACY.
[2] Connect optional filter capacitor between pin 1 and pin 2 (see Figure 2). Pin 1 is protected for shorts to ground and the positive supply voltage. Pin 1 is not protected for negative voltage greater than 1 volt.
[3] Protected for short circuit to ground and/or either supply voltage.
[4] Recommended power supply: Analog Devices' model 904.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



Weight: 40 grams

MATING SOCKET AC1016

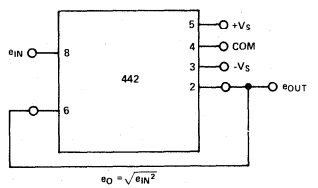


Figure 1. Wiring Connections for rms Measurements (No External Trim)

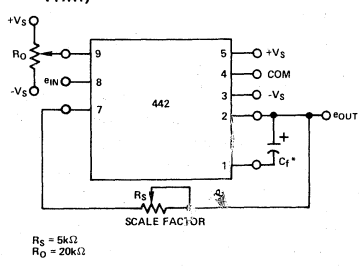


Figure 2. Optional External Adjustment for rms Measurements

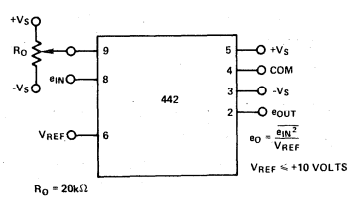


Figure 3. Wiring Connections for Mean Square Measurements with Adjustable Scale Factor (V_{REF})

Log-Antilog Amplifiers

Contents

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757N/P Log-Ratio Amplifier Module	8-11
759N/P Low-Cost, Widest-Bandwidth Log-Antilog Amplifier Module	8-7

Selection Guide
Log-Antilog Amplifiers

This Selection Guide includes both log/antilog amplifiers and log-ratio modules. The suffixes "N" and "P" refer to the specified polarity of input current or voltage when connected as a log amplifier, or the polarity of output voltage as an antilog amplifier. "N" designates *positive* voltage, "P" *negative*.

General information and definitions of specifications can be found in the following pages. All specifications are typical at rated supply and load, and $T_A = +25^{\circ}C$, unless noted otherwise.

Model	Characteristics	Vol I Page	Vol II Page
Model 755N/P Log-antilog amplifier	High performance: ±1% max log-conformity error for 6 decades of current (1nA to 1mA) and 4 decades of voltage (1mV to 10V), and 0.5% max conformity error for 4 decades of current (10nA to 100μA) and 3 decades of voltage (1mV to 1V), 1.5″ x 1.5″ x 0.4″ module. Antilog output range: 4 decades, 1mV to 10V, K = 1, 2, 2/3 V/decade, I_{ref} = 10μA (externally adjustable).	6-41	8-7
Model 759N/P Log-antilog amplifier	Small size and low cost: 1.13″ x 1.13″ x 0.4″ module, wide bandwidth 200kHz @ 1μA, ±2% max log-conformity error for 5 decades of current (10nA to 1mA) or 4 decades of voltage (1.0mV to 10V), and ±1% max conformity error for 4 decades of current (20nA to 200μA). Log operating range: 6 decades of current (1nA to 1mA) and 4 decades of voltage (1mV to 10V). Antilog output range: 4 decades (1mV to 10V), K = 1, 2, 2/3 V/decade, I_{ref} = 10μA (externally adjustable).	6-41	8-7
Model 757N/P Log-ratio module	Input dynamic range, 6 decades of current (1nA to 1mA), either channel, log conformity error ±1.0% max; for 4 decades (10nA to 100μA), log conformity error ±0.5% max. Log of voltage by using external resistors. K = 1 V/decade, ±1%, max, or externally programmable. Can be used for antilog operations.	6-43	8-11

In addition to the products in this Section, Analog Devices also manufactures digital-to-analog converters with logarithmic properties (e.g., AD7111), for use in digital control of gain and in the design of moderate-resolution A/D converters with wide dynamic range. They are to be found in Section 10 of Volume I.

Orientation
Log-Antilog Amplifiers

The devices catalogued in this section are complete, self-contained modules that provide output voltage proportional to the logarithm or the antilogarithm (exponential) of an input quantity. These modules operate on the instantaneous values of inputs from dc to an upper cutoff frequency below 1MHz.

LOGS AND LOG RATIOS

In the *logarithmic* mode, the ideal output equation is

$$E_o = -K \log_{10} \left(\frac{I_{in}}{I_{ref}}\right)$$

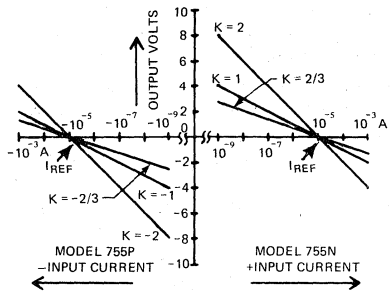
E_o can be positive or negative; it is zero when the ratio is unity, i.e., $I_{in} = I_{ref}$. K is the output scale constant; it is equal to the number of output volts corresponding to a decade* change of the ratio. In the 755 and 759 log amplifiers, K is pin-programmable to be either 1V, 2V, or 2/3V, or externally adjustable to any value $\geqslant$ 2/3V; in the model 757 log-ratio amplifier, K may be either a preset value of 1V, or an arbitrary value adjustable by an external resistance ratio.

I_{in} is a unipolar input current within a 6-decade range (1nA to 1mA); it may be applied directly, as a current, or derived from an input voltage via an input resistor (in which case, the ratio becomes $E_{in}/(R_{in}I_{ref}) = E_{in}/E_{ref}$. In models 755 and 759, the magnitude of I_{ref} is internally fixed at 10μA (E_{ref} = 0.1V) or externally adjusted; but model 757 is a *log-ratio* amplifier, in which both I_{in} and I_{ref} (or E_{in} and E_{ref}, using external scaling resistors) are input variables.

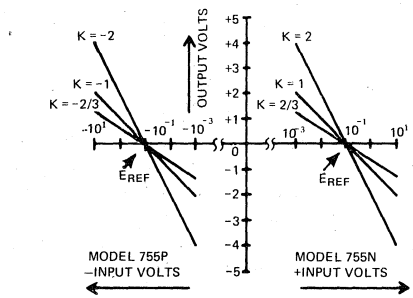
Each of the log amplifiers is available as a "P" or "N" option, depending on the polarity of the input voltage. Logarithms may be computed only for positive arguments, therefore the reference current must be of appropriate polarity to make the ratio positive. "N" indicates that the input current (or voltage) for the log mode is *positive;* "P" indicates that only *negative* voltage or current may be applied in the log mode. The polarity of K also differs: K is positive for "N" versions and negative for "P" versions. Thus, +10V applied to model 759N, with K = +1V, would produce an output voltage, $E_o = -1V \log (100) = -2V$; on the other hand, -10V applied to model 759P, with K = 1V, would produce an output voltage, $E_o = -(-1V) \log (100) = +2V$. The figure shows, in condensed form, the outputs of P and N log-amps, with differing K values, for voltage and current inputs.

Log amplifiers in the log mode are useful for applications requiring *compression* of wide-range analog input data, *linearization* of transducers having exponential outputs, and *analog computing*, ranging from simple translation of natural relationships in log form (e.g., computing absorbance as the log-ratio of input currents), to the use of logarithms in facilitating analog computation of terms involving arbitrary exponents and multi-term products and ratios.

*A *decade* is a 10:1 ratio, two decades is 100:1, etc. For example, if K = 2, and the ratio is 10, the magnitude of the output would be 2V, and its polarity would depend on whether the ratio were greater or less than unity. If the input signal then changed by a factor of 1000 (3 decades), the output would change by 6V.



Log of Current



Log of Voltage

Output vs. Input of Model 755N & 755P in Log Connection (Log Input Scales), Showing Voltages, and Polarity Relationships

ANTILOGS

In the *antilogarithmic* (exponential) mode, the ideal output equation is

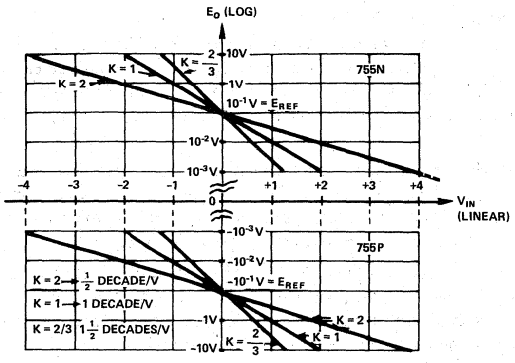
$$E_o = E_{ref} \exp_{10} (-E_{in}/K)$$

E_{in} can be positive or negative; when it is zero, $E_o = E_{ref}$. However, E_o is always of single polarity, positive for "N" versions, negative for "P" versions. Thus, for 759P, connected for K = -2V, if E_{in} = +4V, and E_{ref} = -0.1V, then

$E_o = -0.1V \cdot 10^{-4/-2}$, or -10V; if E_{in} = -4V, then

$E_o = -0.1V \cdot 10^{-(-4)/-2} = -1mV$. The figure on the next page shows, in condensed form, the outputs of P and N log amps, connected for antilogarithmic operation, with different K values.

Antilog amplifiers are useful for applications requiring *expansion* of compressed data, *linearization* of transducers having logarithmic outputs, *analog function fitting* or function generation, to obtain relationships or generate curves having voltage-programmable rates of growth or decay, and in *analog computing*, for such functions as compound multiplication and division of terms having differing exponents.



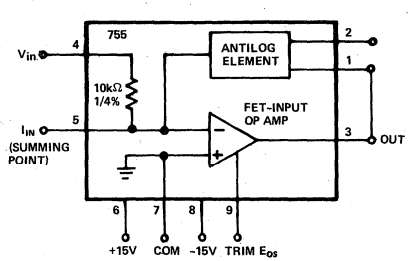
Antilog Operator Response Curves, Semilog Scale
$E_O = E_{REF}\ 10^{V_{IN}/-K}$

LOG-ANTILOG AMPLIFIER PERFORMANCE

Considerable information regarding log- and antilog-amplifier circuit design, performance, selection, and applications is to be found in the NONLINEAR CIRCUITS HANDBOOK[1]. Several salient points will be covered here, and specifications will be defined.

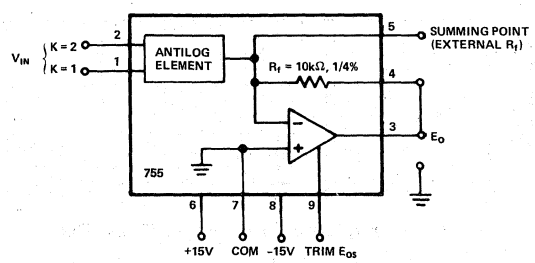
A log/antilog amplifier consists of an operational amplifier and an element with antilogarithmic transconductance (i.e., the voltage into the element produces a current that is an exponential function of the voltage). As the figure shows, for logarithmic operations, the input current is applied at the op-amp summing point, and the feedback circuit causes the amplifier output to produce whatever voltage is required to provide a feedback current that will exactly balance the input current.

In antilog operation, the input voltage is applied directly to the input of the antilog element, producing an exponential input current to the op-amp circuit. The feedback resistance transduces it to an output voltage.



a) Log/Antilog Amplifier Connected in the Log Mode (K = 1)

[1] *Nonlinear Circuits Handbook*, Analog Devices, Inc., 1974, 1976, 536pp, edited by D. H. Sheingold, $5.95; send check or complete MasterCard data to P.O. Box 796, Norwood MA 02062



b) Log/Antilog Amplifier Connected in the Exponential Mode

The wide range of log/exponential behavior is made possible by the exponential current-voltage relationship of transistor base-emitter junctions,

$$I = I_o(e^{qV/kT} - 1) \cong I_o e^{qV/kT}$$

and $V = (kT/q) \ln (I/I_o)$

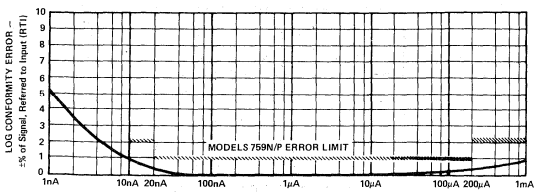
where I is the collector current, I_o is the extrapolated current for V = 0, V is the base-emitter voltage, q/k (11605° K/V) is the ratio of charge of an electron to Boltzmann's constant, and T is junction temperature kelvin. In log/antilog devices, two matched transistors are connected so as to subtract the junction voltages associated with the input and reference currents, making the ratio independent of I_o's variation with temperature.

$$\begin{aligned}\Delta V &= (kT/q) \ln (I_{in}/I_o) - (kT/q) \ln (I_{ref}/I_o)\\ &= (kT/q) (\ln I_{in} - \ln I_{ref}) + (kT/q) (\ln I_o - \ln I_o)\\ &= (kT/q) \ln (I_{in}/I_{ref})\end{aligned}$$

The temperature-dependence of gain is compensated for by a resistive attenuator that uses a temperature-sensitive resistor for compensation. The attenuator also produces amplification of K to the specified nominal values, e.g., from the basic 59mV/decade (kT/q) ln10 at room temperature) to 1V/decade.

Errors are introduced by the offset current of the amplifier, and the offset voltage, for voltage inputs; by inaccuracy of the reference current (or the effective reference voltage, for voltage inputs) in fixed-reference devices; and by inaccuracy of setting K. Additional errors are introduced by drift of these parameters with temperature. At any temperature, if these parameters are nulled out, there remains a final irreducible difference between the actual output and the theoretical output, called *log-conformity error*, which is manifested as a "nonlinearity" of the input-output plot on semilog paper. Best log conformity is realized away from the extremities of the rated signal range. For example, log-conformity error of model 755 is ±1% maximum, referred to the input, over the entire 6-decade range from 1nA to 1mA; but it is only ±0.5% maximum over the 4-decade range from 10nA to 100μA. A plot of log conformity error for model 759 is shown here.

Errors occurring at the input, and log-conformity errors, can only be observed at the output, but it is useful to refer them to the input (RTI). Equal percentage errors at the input, at what-



Log Conformity Error for Models 759N and 759P

ever input level, produce equal incremental errors at the output, for a given value of K. For example, if K = 1, and the RTI log-conformity error is +1%, the magnitude of the output error will be

$$\begin{aligned}\text{Error} &= \text{Actual output} - \text{ideal output}\\ &= 1V\cdot\log(1.01\ I/I_{ref}) - 1V\cdot\log(I/I_{ref})\\ &= 1V\cdot\log 1.01 = 0.0043V = 4.3mV\end{aligned}$$

If, in this example, the input range happens to be 5 decades, the corresponding output range will be 5 volts, and the 4.3mV log-conformity error, as a percentage of total *output* range, will be less than 0.1%. Because this ambiguity can prove confusing to the user, it is important that a manufacturer specify whether the error is referred to the input or the output. The table below indicates the conversion between RTI percentage and output error-magnitudes, for various percent errors, and various values of K.

LOG OUTPUT ERROR (mV)

% ERROR RTI	K = 1V	K = 2V	K = (2/3)V
0.1	0.43	0.86	0.28
0.5	2.2	4.3	1.4
1.0	4.3	8.6	2.9
2.0	8.6	17.	5.7
3.0	13.	26.	8.6
4.0	17.	34.	11.
5.0	21.	42.	14.
10.0	41.	83.	28.

For antilog operations, input and output errors are interchanged.

To arrive at the total error, an error budget should be made up, taking into account each of the error sources, and its contribution to the total error, over the temperature range of interest.

Dynamic response of log amps is a function of the input level. Small-signal bandwidths of ac input signals biased at currents above 1μA tend to be roughly comparable. However, below 1μA, bandwidth tends to be in rough proportion to current level. Similarly, rise time depends on step magnitude and direction – step changes in the direction of increasing current are responded to more quickly than step decreases of current.

DEFINITIONS OF SPECIFICATIONS

Log-Conformity Error When the parameters have been adjusted to compensate for offset, scale-factor, and reference errors, the *log-conformity error* is the deviation of the resulting function from a straight line on a semilog plot over the range of interest.

Offset Current (I_{os}) is the bias current of the amplifier, plus any stray leakage currents. This parameter can be a significant source of error when processing signals in the nanoampere region. Its contribution in antilog operation is negligible.

Offset Voltage (E_{os}) depends on the operational amplifier used for the log operation. Its effect is that of a small voltage in series with the input resistor. For current-logging operations, with high-impedance sources, its error contribution is negligible. However, for voltage logging, it modifies the value of V_{in}. Though it can be adjusted to zero at room temperature, its drift over the temperature range should be considered. In antilog operation, E_{os} appears at the output as an essentially constant voltage; its percentage effect on error is greatest for small outputs.

Reference Current (I_{ref}) is the effective internally-generated current-source output to which all values of input current are compared. I_{ref} tolerance appears as a dc offset at the output; it can be adjusted towards zero by adjusting the reference current, adding a voltage to the output by injecting a current into the scale-factor attenuator, or simply by adding a constant bias at the output's destination.

Reference Voltage (E_{ref}) is the effective internally generated voltage to which all input voltages are compared. It is related to I_{ref} by the equation: $E_{ref} = I_{ref}R_{in}$, where R_{in} is the value of input resistance. Typically, I_{ref} is less stable than R_{in}; therefore, practically all the tolerance is due to I_{ref}.

Scale Factor (K) is the voltage change at the output for a decade (i.e., 10:1) change at the input, when connected in the log mode. Error in scale factor is equivalent to a change in gain, or slope (on a semilog plot), and is specified in percent of the nominal value.

6-Decade, High Accuracy and Wideband Log, Antilog Amplifiers

MODELS 755N, 755P, 759N, 759P

FEATURES

High Accuracy: Models 755N, 755P
Wideband: Models 759N, 759P
Complete Log/Antilog Amplifiers: External Components Not Required
Temperature-Compensated Internal Reference
6 Decades Current Operation: 1nA to 1mA
1% max Error: 1nA to 1mA (755)
20nA to 200μA (759)
4 Decades Voltage Operation: 1mV to 10V
1% max Error: 1mV to 10V (755)
1mV to 2V (759)
Small Size: 1.1" X 1.1" X 0.4"



8

GENERAL DESCRIPTION

The models 755N, 755P and 759N, 759P are low cost dc logarithmic amplifiers offering conformance to ideal log operation over 6 decades of current (1nA to 1mA) and 4 decades of voltage (1mV to 10V). For high accuracy requirements, models 755N, 755P offer maximum nonconformity of 0.5%, from 10nA to 1mA, and 1mV to 1V. For wideband applications, the models 759N, 759P provide fast response (300kHz @ I_{SIG} = 10μA to 1mA) and feature maximum nonconformity of 1% from 20nA to 200μA, and 1mV to 2V. The models 755N and 759N compute the log of positive (+) input signals, while the models 755P, 759P compute the log of negative (-) signals.

Designed for ease of use, the models 755N/P and 759N/P are complete, temperature compensated log/antilog amplifiers packaged in a compact epoxy-encapsulated module. External components are not required for logging currents over the complete 6 decade range of 1μA to 1mA. Both the scale factor (K=2, 1, or 2/3 volt/decade) and log/antilog operation are selected by simple pin connection. In addition, both the internal 10μA reference current as well as the offset voltage may be externally adjusted to improve overall accuracy.

The models 755 and 759 are ideally suited as an alternative to in-house designs of OEM applications. Advanced design techniques and superior performance place the 755 and 759 ahead of competitive designs in terms of price, performance and package design.

APPLICATIONS

When connected in the current or voltage logging configuration, as shown in Figure 1, the models 755 and 759 may be used in several key applications. A plot of input current versus output voltage is also presented to illustrate the log amplifier's transfer characteristics.

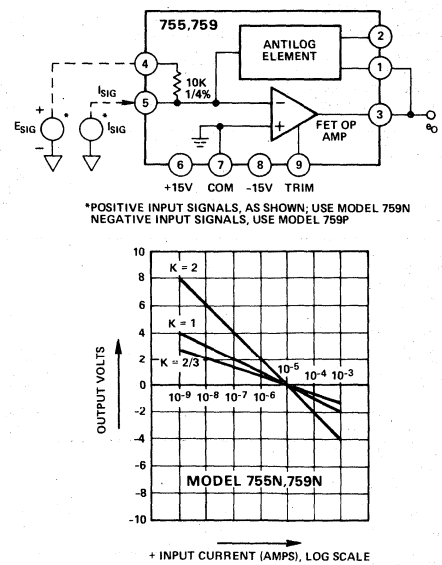


Figure 1. Functional Block Diagram and Transfer Function

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

MODEL	755N/P	759N/P
TRANSFER FUNCTIONS		
Current Mode	$e_O = -K\log_{10}\frac{I_{SIG}}{I_{REF}}$	*
Voltage Mode	$e_O = -K\log_{10}\frac{E_{SIG}}{E_{REF}}$	*
Antilog Mode	$e_O = E_{REF}\ 10^{-\left(\frac{E_{SIG}}{K}\right)}$	*
TRANSFER FUNCTION PARAMETERS		
Scale Factor (K) Selections[1, 2]	2, 1, 2/3 Volt/Decade	*
Error @ +25°C	±1% max	*
vs. Temperature (0 to +70°C)	±0.04%/°C max	*
Reference Voltage (E_{REF})[2]	0.1V	*
Error @ +25°C	±3% max	±4% max
vs. Temperature (0 to +70°C)	±0.1%/°C max	±0.05%/°C
Reference Current (I_{REF})[2]	10μA	*
Error @ +25°C	±3% max	*
vs. Temperature (0 to +70°C)	±0.1%/°C max	

MAXIMUM LOG CONFORMITY ERROR

I_{SIG} RANGE	E_{SIG} RANGE	RTI	RTO (K=1)	RTI	RTO (K=1)
1nA to 10nA	–	±1%	±4.3mV	±5%	±21mV
10nA to 20nA	–	±0.5%	±2.17mV	±2%	±8.64mV
20nA to 100μA	1mV to 1V	±0.5%	±2.17mV	±1%	±4.3mV
100μA to 200μA	1V to 2V	±1%	±4.3mV	±1%	±4.3mV
200μA to 1mA	2V to 10V	±1%	±4.3mV	±2%	±8.64mV

INPUT SPECIFICATIONS		
Current Signal Range		
Model 755N, 759N	+1nA to +1mA min	*
Model 755P, 759P	−1nA to −1mA min	*
Max Safe Input Current	±10mA max	*
Bias Current @ +25°C	(0, +) 10pA max	(0, +) 200pA max
vs. Temperature (0 to +70°C)	x2/+10°C	*
Voltage Signal Range (Log Mode)		
Model 755N, 759N	+1mV to +10V min	*
Model 755P, 759P	−1mV to −10V min	*
Voltage Signal Range, Antilog Mode Model 755N, 755P	$-2 \leqslant \frac{E_{SIG}}{K} \leqslant 2$	*
Offset Voltage @ +25°C (Adjustable to 0)	±400μV max	±2mV max
vs. Temperature (0 to +70°C)	±15μV/°C max	±10μV/°C
vs. Supply Voltage	±15μV/%	*
FREQUENCY RESPONSE, Sinewave		
Small Signal Bandwidth, −3dB		
I_{SIG} = 1nA	80Hz	250Hz
I_{SIG} = 1μA	10kHz	100kHz
I_{SIG} = 10μA	40kHz	200kHz
I_{SIG} = 1mA	100kHz	200kHz
RISE TIME		
Increasing Input Current		
10nA to 100nA	100μs	20μs
100nA to 1μA	7μs	3μs
1μA to 1mA	4μs	2.5μs
Decreasing Input Current		
1mA to 1μA	7μs	3μs
1μA to 100nA	30μs	10μs
100nA to 10nA	400μs	80μs
INPUT NOISE		
Voltage, 10Hz to 10kHz	2μV rms	10μV rms
Current, 10Hz to 10kHz	2pA rms	10pA rms
OUTPUT SPECIFICATIONS[3]		
Rated Output		
Voltage	±10V min	*
Current		
Log Mode	±5mA	*
Antilog Mode	±4mA	*
Resistance	0.5Ω	*
POWER SUPPLY[4]		
Rated Performance	±15Vdc	*
Operating	±(12 to 18)Vdc	*
Current, Quiescent	±7mA	±4mA
TEMPERATURE RANGE		
Rated Performance	0 to +70°C	*
Operating	−25°C to +85°C	*
Storage	−55°C to +125°C	*
CASE SIZE[5] (W x L x H)	1.5" x 1.5" x 0.4" (38 x 38 x 10.4)	1.125" x 1.125" x 0.4" (29 x 29 x 10.4)

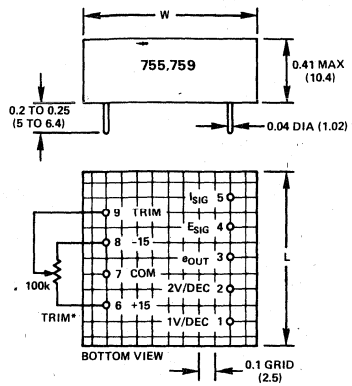
*Specifications same as 755N/P.

[1] Use terminal 1 for K = 1V/decade; terminal 2 for K = 2V/decade; terminals 1 or 2 (shorted together) for K = 2/3V/decade.
[2] Specification is + for models 755N, 759N; − for 755P, 759P.
[3] No damage due to any pin being shorted to ground.
[4] Recommended power supply, model 904, ±15V @ ±50mA output.
[5] Case size in inches (mm).

Specifications subject to change without notice.

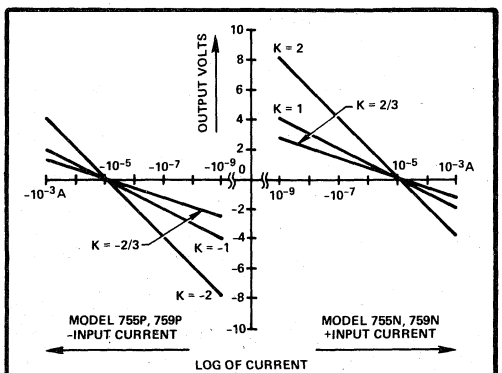
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

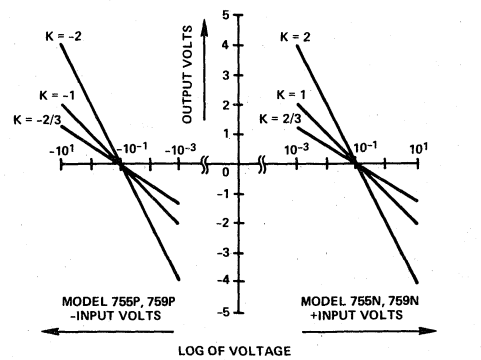


*Optional 100kΩ external trim pot. Input offset voltage may be adjusted to zero with trim pot connected as shown. With trim terminal 9 left open, input offset voltage will be ±0.4mV (755) or ±2mV (759) maximum.

MATING SOCKET AC1016



Plot of Output Voltage vs Input Current for Model 755 Connected in the Log Mode



Plot of Output Voltage vs Input Voltage for Models 755, 759 Connected in the Log Mode

Figure 2. Transfer Curves

PRINCIPLE OF OPERATION

Log operation is obtained by placing the antilog element in the feedback loop of the op amp as shown in Figure 1. At the summing junction, terminal 5, the input signal current to be processed is summed with the output current of the antilog element. To attain a balance of these two currents, the op amp provides the required output voltage to the antilog feedback element. Under these conditions the ideal transfer equation (K = 1) is:

$$e_{OUT} = 1V \log_{10} I_{SIG}/I_{REF}$$

The log is a mathematical operator which is defined only for numbers, which are dimensionless quantities. Since an input current would have the dimensions of amperes it must be referenced to another current, I_{REF}, the ratio being dimensionless. For this purpose a temperature compensated reference of 10μA is generated internally.

The scale factor, K, is a multiplying constant. For a change in input current of one decade (decade = ratio of 10:1), the output changes by K volts. K may be selected as 1V or 2V by connecting the output to pin 1 or 2, respectively. If the output is connected to both pins 1 and 2, K will be 2/3V.

REFERRING ERRORS TO INPUT

A unique property of log amplifiers is that a dc error of any given amount at the output corresponds to a constant percent of the input, regardless of input level. To illustrate this, consider the output effects due to changing the input by 1%.

The output would be:

$$e_{OUT} = 1V \log_{10} (I_{SIG}/I_{REF})(1.01) \text{ which is equivalent to:}$$

$$e_{OUT} = \underbrace{1V \log_{10} (I_{SIG}/I_{REF})}_{\text{Initial Value}} \quad \underbrace{\pm 1V \log_{10} (1.01)}_{\text{Change}}$$

The change in output, due to a 1% input change is a constant value of ±4.3mV. Conversely, a dc error at the output of ±4.3mV is equivalent to a change at the input of 1%. An abbreviated table is presented below for converting between errors referred to output (R.T.O.), and errors referred to input (R.T.I.).

	ERROR R.T.O.		
ERROR R.T.I.	K = 1	K = 2	K = 2/3
0.1%	0.43mV	0.86mV	0.28mV
0.5	2.17	4.34	1.45
1.0	4.32	8.64	2.88
3.0	12.84	25.68	8.56
4.0	17.03	34.06	11.35
5.0	21.19	42.38	14.13
10.0	41.39	82.78	27.59

Table 1. Converting Output Error in mV to Input Error in %

SOURCES OF ERROR

Log Conformity Error – Log conformity in logarithmic devices is a specification similar to linearity in linear devices. Log conformity error is the difference between the value of the transfer equation and the actual value which occurs at the output of the log module, after scale factor, reference and offset errors are eliminated to taken into account. The best linearity performance for the models 755, 759 are obtained in the 5 decades from 10nA to 1mA. To obtain optimum performance, the input data should be scaled to this range.

Offset Voltage – The offset voltage, E_{os}, of models 755, 759 is the offset voltage of the internal FET amplifier. This voltage appears as a small dc offset voltage in series with the input terminals. For current logging applications, its error contribution is negligible. However, for log voltage applications, best performance is obtained by an offset trim adjustment.

Bias Current – The bias current of models 755, 759 is the bias current of the internal FET amplifier. This parameter can be a significant source of error when processing signals in the nanoamp region. For this reason, the bias current for model 755 is 10pA, maximum, and 200pA maximum for model 759.

Reference Current – I_{REF} is the internally generated current source to which all input currents are compared. I_{REF} tolerance errors appear as a dc offset at the output. The specified value of I_{REF} is ±3% referred to the input, and, from Table 1, corresponds to a dc offset of ±12.84mV for K = 1. This offset is independent of input signal and may be removed by injecting a current into terminal 1 or 2.

Reference Voltage – E_{REF} is the effective internally generated voltage to which all input voltages are compared. It is related to I_{REF} through the equation:
$E_{REF} = I_{REF} \times R_{IN}$, where R_{IN} is an internal 10kΩ, precision resistor. Virtually all tolerance in E_{REF} is due to I_{REF}. Consequently, variations in I_{REF} cause a shift in E_{REF}.

Scale Factor – Scale factor is the voltage change at the output for a decade (i.e., 10:1) change at the input, when connected in the log mode. Error in scale factor is equivalent to a change in gain, or slope, and is specified in per cent of the nominal value. An external adjustment may be performed if fine trimming is desired for improved accuracy.

OPTIONAL EXTERNAL ADJUSTMENTS FOR LOG OPERATION

Trimming E_{OS} – The amplifier's offset voltage, E_{OS}, may be trimmed for improved accuracy with the models 755, 759 connected in its log circuit. To accomplish this, a 100kΩ, 10 turn pot is connected as shown in Figure 3. The input terminal, Pin 4, is connected to ground. Under these conditions the output voltage is:

$$e_{OUT} = -K \log_{10} E_{OS}/E_{REF}$$

To obtain an offset voltage of 100μV or less, for K = 1, the trim pot should be adjusted until the output voltage is between +3 and +4 volts for models 755N, 759N, and -3V to -4V for models 755P, 759P.

For other values of K, the trim pot should be adjusted for an output of e_{OUT} = 3 x K to 4 x K where K is the scale factor.

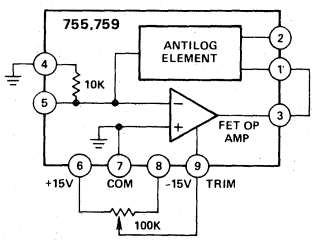


Figure 3. Trimming E_{OS} in Log Mode

Reference Current or Reference Voltage – The reference current or voltage of models 755, 759 may be shifted by injecting a constant current into the unused scale factor terminal (Pin 1 or Pin 2). The current injected will shift the reference one decade, in accordance with the expression: $I_I = 66\mu A \log 10\mu A/I_{REF}$ (755), $I_I = 330\mu A \log 10\mu A/I_{REF}$ (759), where I_I = current to be injected and I_{REF} = the desired reference current.

By changing I_{REF}, there is a corresponding change in E_{REF} since, $E_{REF} = I_{REF} \times R_{IN}$. An alternate method for rescaling E_{REF} is to connect an external R_{IN}, at the I_{IN} terminal (Pin 5) to supplant the 10kΩ supplied internally (leaving it unconnected). The expression for E_{REF} is then, $E_{REF} = R_{IN} I_{REF}$. Care must be taken to choose R_{IN} such that $(e_{SIG}\ max)/R_{IN} \leq 1mA$.

Scale Factor (K) Adjustment – Scale factor may be increased from its nominal value by inserting a series resistor R_S between the output terminal, Pin 3, and either terminal 1 or 2. The table below should be consulted when making these scale factor changes.

RANGE OF K	CONNECT SERIES R TO PIN	VALUE OR R_S	NOTE
2/3V to 1.01V	1	R x (K – 2/3)	use pins 1, 2
1.01V to 2.02V	1	R x (K – 1)	use pin 1
>2.02V	2	R x (K – 2)	use pin 2

R = 15kΩ (755); 3kΩ (759)

Table 2. Resistor Selection Chart for Shifting Scale Factor

ANTILOG OPERATION

The models 755 and 759 may be used to develop the antilog of the input voltage when connected as shown in Figure 4. The antilog transfer function (an exponential), is:

$$e_{OUT} = E_{REF}\ 10^{-e_{IN}/K} \qquad [-2 \leq e_{IN}/K \leq 2]$$

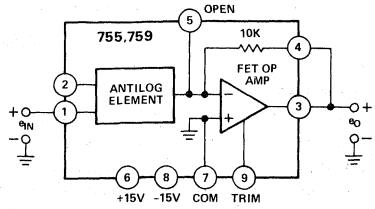


Figure 4. Functional Block Diagram

Principle of Operation – The antilog element converts the voltage input, appearing at terminal 1, to a current which is proportional to the antilog of the applied voltage. The current-to-voltage conversion is then completed by the feedback resistor in a closed-loop op amp circuit.

A more complete expression for the antilog function is:

$$e_{OUT} = E_{REF}\ 10^{-e_{IN}/K} + E_{OS}$$

The terms K, E_{OS}, and E_{REF} are those described previously in the LOG section.

Offset Voltage (E_{OS}) Adjustment – Although offset voltage of the antilog circuit may be balanced by connecting it in the log mode, and using the technique described previously, it may be more advantageous to use the circuit of Figure 5. In this configuration, offset voltage is equal to $e_{OUT}/100$. Adjust for the desired null, using the 100k trim pot. After adjusting, turn power off, remove the external 100Ω resistor, and the jumper from Pin 1 to +15V. For 755P, 759P use the same procedure but connect Pin 1 to -15V.

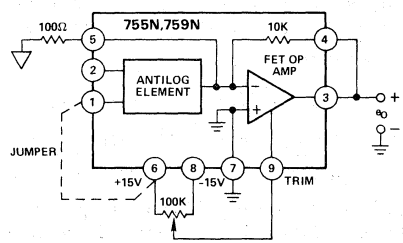


Figure 5. Trimming E_{OS} in Antilog Mode

Reference Voltage (E_{REF}) Adjustment – In antilog operation, the voltage reference appears as a multiplying constant. E_{REF} adjustment may be accomplished by connecting a resistor, R, from Pin 5 to Pin 3, in place of the internal 10kΩ. The value of R is determined by:

$$R = E_{REF}\ \text{desired}/10^{-5}\ A$$

Scale Factor (K) Adjustment – The scale factor may be adjusted for all values of K greater than 2/3V by the techniques described in the log section. If a value of K less than 2/3V is desired for a given application, an external op amp would be required as shown in Figure 6. The ratio of the two resistors is approximately:

$$R1/R_G = (1/K - 1) \text{ where K = desired scale factor}$$

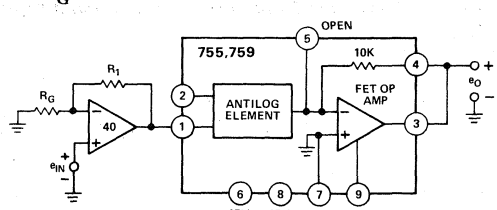


Figure 6. Method for Adjusting K< 2/3V

6-Decade, High Accuracy Log Ratio Amplifiers

MODEL 757N, 757P

FEATURES
- 6 Decade Operation – 1nA to 1mA
- 1/2% Log Conformity – 10nA to 100μA
- Symmetrical FET Inputs
- Voltage or Current Operation
- Temperature Compensated

APPLICATIONS
- Absorbence Measurements
- Log Ratios of Voltages or Currents
- Data Compression
- Transducer Linearization



8

GENERAL DESCRIPTION

Model 757 is a complete, temperature compensated, dc-coupled log ratio amplifier. It is comprised of two input channels for processing signals spanning up to 6 decades in dynamic range (1nA to 1mA). By virtue of its symmetrical FET input stages, the 757 can accommodate this 6 decade signal range at either channel. Log conformity is maintained to within 1/2% over 4 decades of input (10nA to 100μA) and to within 1% over the full input range. Unlike other log ratio designs, model 757 does not restrict the relative magnitude of the two signal inputs to achieve rated performance. Either input can be operated within the specified range regardless of the signal level at the other channel.

The model 757 log-ratio amplifier design makes available both input amplifier summing junctions. As a result, it can directly interface with photo diodes operating in the short-circuit current mode without the need of additional input circuitry.

The excellent performance of model 757 can be further improved by means of external scale factor and output offset adjustments. A significant feature of model 757 not found on competing devices is that, when the offset adjustment is used to establish a fixed bias at the output, the output offset level does not vary as a function of input signal magnitude. On other designs, the sensitivity of output offset to input levels results in output effects resembling log conformity errors.

Model 757 can operate with either current or voltage inputs. Its excellent performance makes it ideally suited for log ratio applications such as blood analysis, chromatography, chemical analysis of liquids and absorbence measurements.

CURRENT LOG RATIO

Current log ratio is accomplished by model 757 when two currents, I_{SIG} and I_{REF}, are applied directly to the input terminals (see Figure 1). The two log amps process these signals providing

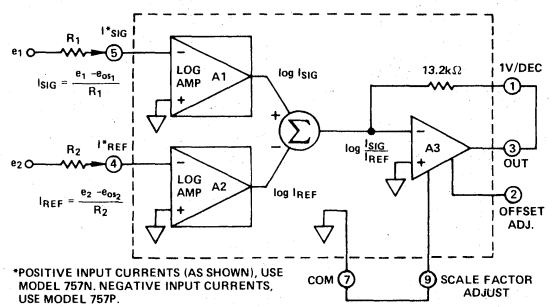


Figure 1. Functional Block Diagram of Model 757

voltages which are proportional to the log of their respective inputs. These voltages are then subtracted and applied to an output amplifier. The scale factor, when connected as shown, is 1V/dec. However, higher scale factors may be achieved by connecting external scale factor adjusting resistors. (See section on optional adjustments and trims.)

VOLTAGE LOG RATIO

The principle of operation for voltage log ratio is identical to that of current log ratio after the voltage signal has been converted to a current. To accomplish this conversion, an external resistor is attached from the voltage signal to the appropriate input current terminal of the 757. Input currents are then determined by:

$$I_{SIG} = \frac{e_1 - e_{os_1}}{R_1}, \quad I_{REF} = \frac{e_2 - e_{os_2}}{R_2}$$

e_{os_1} = Input Offset Voltage (I_{SIG} Channel)

e_{os_2} = Input Offset Voltage (I_{REF} Channel)

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise noted)

MODEL	757N/P
TRANSFER FUNCTION [1]	
Current Mode	$e_o = -K \log_{10} \frac{I_{SIG}}{I_{REF}}$
Voltage Mode	$e_o = -K \log_{10} \left[\frac{(e_1 - e_{os_1})}{(e_2 - e_{os_2})} \times \frac{R_2}{R_1} \right]$
ACCURACY	
Log Conformity [2]	
I_{SIG}, I_{REF} = 10nA to 100μA	±0.5%, max
I_{SIG}, I_{REF} = 1nA to 1mA	±1%, max
Scale Factor (1V/Dec)	(+0, -2%) max
vs. Temperature (0 to +70°C)	±0.04%/°C max
INPUT SPECIFICATIONS — Both Input Channels	
Current	
Signal Range, Rated Performance	
Model 757N	+1nA to +1mA min
Model 757P	-1nA to -1mA min
Max Safe	±10mA max
Bias Current, @ +25°C	(0, +) 10pA max
vs. Temperature (0 to +70°C)	x2/+10°C
Offset Voltage, @ +25°C	±1mV max
vs. Temperature (0 to +70°C)	
I_{SIG} Channel	±25μV/°C max
I_{REF} Channel	±25μV/°C max
vs. Supply Voltage	±5μV/%
FREQUENCY RESPONSE, Sinewave	
Small Signal Response (-3dB)	
Signal Channel	
I_{SIG} = 1nA	250Hz
I_{SIG} = 1μA	25kHz
I_{SIG} = 100μA	40kHz
Reference Channel	
I_{REF} = 1nA	100Hz
I_{REF} = 1μA	25kHz
I_{REF} = 100μA	40kHz

RISE TIME	Signal Channel (I_{REF} = 10μA)	Reference Channel (I_{SIG} = 10μA)
Increasing Input Current		
1nA to 10nA	250μs	80μs
10nA to 100nA	50μs	40μs
100nA to 1μA	30μs	30μs
1μA to 100μA	25μs	25μs
Decreasing Input Current		
100μA to 1μA	25μs	25μs
1μA to 100nA	30μs	30μs
100nA to 10nA	100μs	40μs
10nA to 1nA	600μs	70μs

INPUT NOISE	
Voltage (10Hz to 10kHz)	3μV rms
Current (10Hz to 10kHz)	0.1pA rms
OUTPUT SPECIFICATIONS	
Rated Output	
Voltage	±10V min
Current	±5mA min
Resistance	0.1Ω
Offset Voltage [3] (K = 1V/Decade)	±15mV max
vs. Temperature (0 to +70°C)	±0.3mV/°C
vs. Supply	±5μV/V
POWER SUPPLY [4]	
Rated Performance	±15V dc
Operating	±(12 to 18)V dc
Current, Quiescent	±8mA
TEMPERATURE RANGE	
Rated Performance	0 to +70°C
Operating	-25°C to +85°C
Storage	-55°C to +125°C
MECHANICAL	
Case Size	1.5" x 1.5" x 0.4"
Weight	21 grams

[1] For model 757N, K = +1V/Decade and input currents must be positive. For model 757P, K = -1V/Decade and input currents must be negative. (Input currents are defined as positive when flowing into the input terminals, 4 and 5. Refer to TRANSFER CURVES.)

[2] The log conformity error is referred to input (RTI). 1% error RTI is equivalent to 4.3mV of error at the output for K = 1V/Dec.

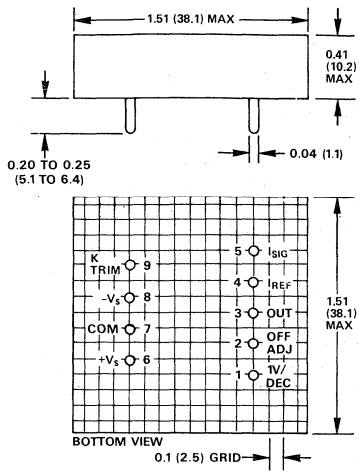
[3] Externally adjustable to zero.

[4] Recommended power supply: Analog Devices model 904, ±15V @ 50mA.

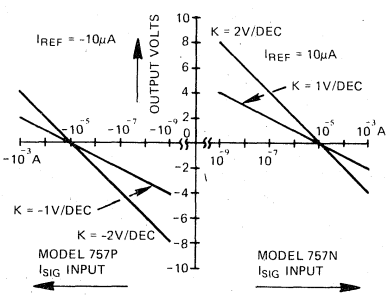
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



TRANSFER CURVES



Log mode output voltage vs. input current for I_{REF} = 10μA.

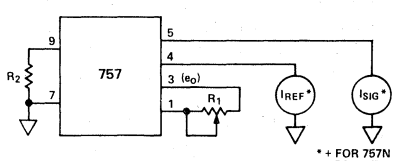


Figure 2. Scale Factor Adjustment

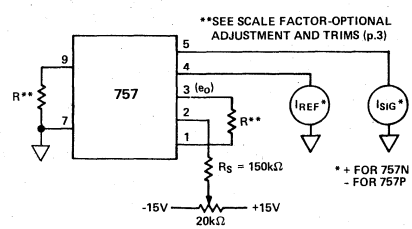


Figure 3. Output Voltage Offset Adjustments

OPTIONAL ADJUSTMENTS AND TRIMS

Scale Factor – A one volt per decade scale factor is available when pin 1 is tied to 3 and pin 7 is connected to 9. Higher scale factors are possible by using a potentiometer, R_1, between pins 1 and 3 and a resistor, R_2, between pins 7 to 9 as shown in Figure 2. The value of the required resistor is (13.2kΩ) (K-1) where K is the desired scale factor. The approximate potentiometer value is also (13.2kΩ) (K-1). The scale factor adjustment procedure is as follows:

1. Connect the appropriate value of resistor between pins 7 and 9.
2. Set I_{REF} = 1μA, I_{SIG} = 10μA. Measure e_O.
3. Set I_{REF} = 1μA, I_{SIG} = 100μA. Adjust R_1 until the difference in e_O corresponding to steps 2 and 3 is K volts.
4. Repeat steps 2 and 3 until the change in e_O = K volts.

Output Voltage Offset – Output voltage offset must be adjusted after the desired scale factor is established as indicated above. To adjust the offset, inject equal dc input currents into the reference and signal channels. The value of the input currents should approximate the average input current levels expected to be encountered in normal operation. Adjust the potentiometer shown in Figure 3 until the output voltage is zero.

LOG CONFORMITY

Log conformity in logarithmic devices is a specification similar to linearity in linear devices. Log conformity error is the difference between the theoretical value of the log of a ratio and the actual value that appears at the output of the log-ratio module after scale factor errors have been eliminated. Measurement of this error is made after initially zeroing the module at unity-ratio and adjusting the desired scale factor.

Figure 4 shows the log conformity performance of model 757 over a 6 decade input range. Log conformity for each channel does not vary noticeably as the current is varied in the other channel.

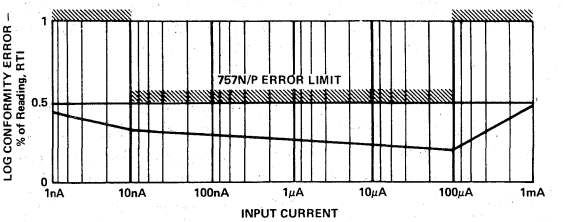


Figure 4. Log Conformity Error for Model 757. Curve is for Either Input Channel with Current Held Constant at 10μA On Other Channel.

FREQUENCY CHARACTERISTICS

Figure 5 shows a plot of small signal response (-3dB) as a function of input signal current. The graph demonstrates the frequency response performance for each input channel over the range of 1nA to 1mA, independent of current on the other channel.

As shown in the graph, the reference channel is faster than the signal channel at low input levels. If an application requires higher speed in the input signal channel than in the reference channel, then the channels can be interchanged with a resulting polarity reversal of the output signal

$$\log \frac{I_{SIG}}{I_{REF}} = \log I_{SIG} - \log I_{REF} = -\log \frac{I_{REF}}{I_{SIG}} .$$

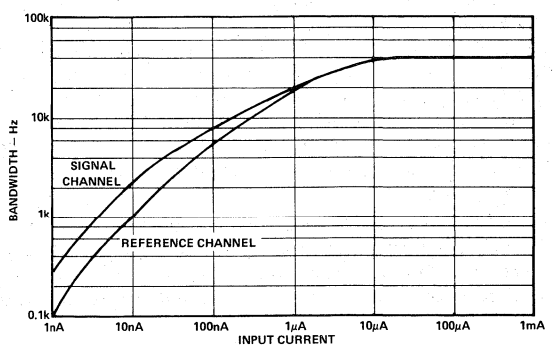


Figure 5. Small Signal Bandwidth (-3dB) vs. Input Signal Level

APPLICATIONS

Data Compression – Processing signals with wide dynamic range is a common problem in instrumentation and data transmission. For example, digitizing an analog signal with a range of 10nA to 100μA with 1% accuracy requires a 20 bit A/D converter. (Required resolution = 1/100 x 1/10,000 = $1/10^6 \cong 1/2^{20}$).

By using the 757 with I_{REF} adjusted to 10nA and K set for 5/4 V/decade, the input data can be compressed into a 5 volt output range. For a 1% resolution of any signal, the allowable output error is 4.32mV x K. Log conformity contributes 2.17mV x K (0.5%) over this range. The remaining error with K = 5/4 is 2.69mV and should correspond to less than the LSB of the converter. With a 5 volt output range 2.69mV corresponds just over the LSB of an 11-bit converter. Thus the 757 module can compress the data for use with a 12 bit A/D (such as Analog Devices AD574JD) to obtain the desired 1% resolution.

Absorbence Measurements – Critical properties of materials which are of particular interest in the fields of chemistry, medicine, spectrometry and pollution control are characterized by absorbence. The relationship between absorbence, A, and light intensity, I, is: $A = \log I_O/I_T$ where I_O = intensity of incident light, and I_T = intensity of transmitted light.

Figure 6 shows the 757 log-ratio module used in such a photometer application. Two inputs represent the intensities of light transmitted through space and through a medium that absorbs light. The absorbence of the medium is given by the formula

$$A = \log \frac{I_{SIGNAL}}{I_{REFERENCE}}$$

where I_{SIGNAL} and $I_{REFERENCE}$ are the currents representing the light intensities.

The transducers used in this application are photodiodes, which provide a short-circuit current proportional to the intensity of applied light. The lowest value of absorbence is determined by the value of I_{REF}, since when $I_{SIG} = I_{REF}$, A = 0. The output of the log-ratio module is externally trimmed to 1V/decade and applied to the input of a 3½-digit DPM through the scaling network R1 and R2.

Model 757 was chosen for this design because it makes available both amplifier summing junctions. When the photodiodes are connected to the summing junctions, they are operated in the short-circuit mode, that is, with zero volts across the diodes. Short-circuit loading is necessary, because accuracy of the photodiodes can be degraded several percent when operated with as little as 100mV across the diode junction.

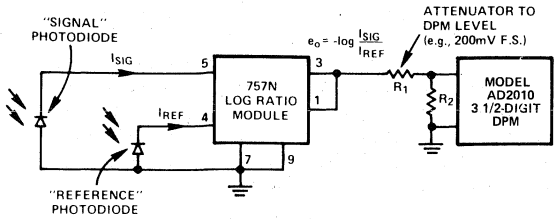


Figure 6. Model 757N Applied to Absorbence Measurements

INTERCONNECTION GUIDELINES

Model 757 is a complete log ratio amplifier that requires no additional frequency compensation for proper operation.

Input Capacitance – Model 757 is able to operate with 1000pF at both input terminals. Therefore, the 757 can be used in applications requiring long cable lengths between the module and the signal transducers.

Input-to-Output Capacitance – When using a log ratio module the user should take care in system configurations to avoid excessive stray capacitance between input and output terminals. Such precautions include avoiding running input and output signal lines close together. If long cable runs are required where inputs and output are closely bundled together, it is advisable to enclose the inputs and/or output in separate, grounded electrostatic shields. By observing simple rules of good circuit layout, problems with oscillations that may result from excessive input-to-output capacitance can easily be avoided. Model 757 can accommodate up to 100pF of input-to-output capacitance without oscillation.

Leakage Resistance – Since model 757 can operate at extremely low input current levels, precautions must be taken to prevent current leakage into the input terminals. Such leakage can cause errors when small input or reference currents are used. This problem may arise on printed circuit layouts if the inputs are run too close to the power supply busses. Providing an etched guard around the input lines, connected to analog signal ground will also reduce unwanted current leakage.

Transducers & Signal Conditioners

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•New product since *1980 Data-Acquisition Components and Subsystems Catalog*

9

Selection Guide
Transducers & Signal Conditioners

SELECTION GUIDE – TEMPERATURE TRANSDUCERS

Model	Characteristics	Vol I Page	Vol II Page
AD590I/J/K/L/M	IC, 2-terminal, TO-52 can or miniature flatpack, −55°C to +150°C (218K to 423K) operating range, linear current output, 1μA/K, laser-trimmed for high accuracy; Output current independent of supply voltage.	9-5	9-7
AC2626J/K/L/M	Stainless-steel temperature probe using AD590, same temperature range and electrical characteristics as the AD590, 3/16″ outside diameter, 6- or 4-inch standard lengths, includes 3 feet of Teflon-coated lead wire, 2s response in stirred water, sensor electrically isolated from sheath (±200V breakdown—case to leads).	–	9-5

SELECTION GUIDE – SIGNAL CONDITIONERS

		CURRENT (4 TO 20mA) OUT							
		I TO I		V TO I	TRANSMITTERS				
		2B24	2B20	2B22	2B52	2B53	2B57	2B58	2B59
Input Sensor	Thermocouple				•	•			
	RTD[1]							•	•
	AD590/AC2626 Temperature Sensor						•		
	Resistance Bridge								
Input Signal	Millivolts				•	•			
	Volts		•	•					
	4 to 20mA	•							
Output	0 to ±5V								
	0 to ±10V								
	0 to 20mA		•						
	4 to 20mA	•	•	•	•	•	•	•	•
	10 to 50mA	•							
	±15V Power								
Special Features	Transducer Excitation						•	•	•
	Open Input Detection				•	•	•		
	Cold Junction Compensation				•	•			
	Input/Output Isolation	•		•	•				
	Channel to Channel Isolation								
	Signal Filter				•	•	•		
	Linearization							•	
	Common Mode Rejection >140dB				•				
Power Required	Loop Powered	•		•[2]	•	•	•	•	•
	+14V to +32V		•	•					
	±15V								
	115V 60Hz Line								
Mechanical	Module		•	•			•		•
	Metal Case	•			•	•	•	•	
	Input Screw Terminals	•			•	•		•	
	Output Screw Terminals	•			•	•		•	
	#22 AWG Input/Output Leads								•
Volume II Page		9-25	9-9	9-13	9-35	9-35	9-47	9-51	9-53

[1] Resistance Temperature Detector.
[2] Provides 4 to 20mA out or may modulate Loop Power.

COMPARED TO TRADITIONAL TEMPERATURE SENSORS FOR -55°C TO +150°C

	AD590/AC2626	RTD	THERMOCOUPLE	THERMISTOR
Linear	•	•		
High Level	•			•
Excitation Insensitive	•		•	
Linearization Required		•	•	•
Remote Sensing Applications	•			
Low Cost	•		•	•

		VOLTAGE OUT							
		MILLIVOLTS IN							
		SINGLE-CHANNEL			MULTI-CHANNEL				
		2B30	2B31	2B50	2B34	2B54	2B55	2B56	2B35
Input Sensor	Thermocouple			•	•	•			
	RTD[1]								
	AD590/AC2626 Temperature Sensor								
	Resistance Bridge		•		•				
Input Signal	Millivolts	•	•	•	•	•			
	Volts						•	•	
	Line Power								•
Output	0 to ±5V			•	•	•	•		
	0 to ±10V	•	•					•	
	0.1 to 10mA								•
	4 to 20mA								
	10 to 50mA								
	±15V Power								•
Special Features	Transducer Excitation		•		•[1]				•
	Open Input Detection			•		•	•		
	Cold Junction Compensation			•				•	
	Input/Output Isolation			•		•	•		•
	Channel to Channel Isolation					•	•		
	Signal Filter	•	•	•	•	•	•		
	Linearization								
	Common Mode Rejection >140dB	•	•	•		•	•		
Power Required	Loop Powered								
	+14V to +32V								
	±15V	•	•	•	•	•	•	•	
	115V 60Hz Line								•
Mechanical	Module	•	•	•	•	•	•	•	•
	Metal Case								
	Input Screw Terminals			•					
	Output Screw Terminals								
	#22 AWG Input/Output Leads								
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[1] Resistance Temperature Detector.

Orientation
Transducers & Signal Conditioners

In this section are listed a wide variety of cost-effective *analog-to-analog* signal conditioners for laboratory and industrial applications, and a set of linear high-output-level semiconductor temperature transducers, manufactured by Analog Devices.

The signal conditioners are intended to provide a variety of system interfaces for signals originating from input transducers or destined for output transducers.

They accept low or high-level signal inputs from millivolts to volts, low- or high-level current inputs from microamperes to 4-to-20mA loops, and direct inputs from transducers, such as strain gages and other bridge devices, RTDs, thermocouples, thermistors, and semiconductor temperature sensors. One of these modules (2B35) is a triple-output power supply that accepts ac line voltage and provides voltage and programmable current excitation for transducers and signal conditioners.

Outputs from these devices include 0-to-20mA, 4-to-20mA and 10-to-50mA transmitter loop current, and normalized voltage at ±5V or ±10V levels for inputs to analog and digital data-acquisition systems. Most of the devices that operate with current loops derive their power directly from the loop supply.

The many useful functions of these devices include—and often combine—voltage-to-current conversion; input-to-output and channel-to-channel isolation; current-to-current conversion; amplification, offsetting, and filtering; transducer voltage and current excitation; all-solid-state isolation, gain, filtering, protection, and multiplexing; thermocouple open-input detection and cold-junction compensation; RTD linearizing.[1]

SELECTION GUIDE

These many functions are sorted out and arranged for easy access in the Selection Guide, so that a device having the desired combination of performance characteristics can be readily found. Device types, classified in broad categories, are ranged horizontally across the top of the chart, and more than two dozen attributes are listed vertically; a bullet (●) is placed at any intersection for which the attribute matches the device.

As an example of how to use the chart, if you want to interface to a thermocouple, look along the horizontal line labeled "Thermocouple" in the Input Sensor grouping. You will find four bullets, indicating four possibly suitable devices, two under the label "4-to-20mA current transmitters," and two under "Voltage Output" (with a choice of single- or multi-channel devices). If you are interested in a current-loop transmitter, and compare the bulleted features of the 2B52 and 2B53, it is easy to find that there is a choice between an isolator and a lower-cost directly coupled device, and that both are housed in metal with easy to use screw terminals. At this point you may turn to the indicated page to compare performance on the data sheet, starting the process of considering the specific device(s) for your application.

THAT'S NOT ALL

Besides the signal conditioners in this section, this databook has technical data on many other products that perform signal-conditioning functions. They are to be found in these sections of this Volume:

Isolation Amplifiers.

D/A Converters (DACs having 4-to-20mA output current, isolation, and other useful features: DAC1420/DAC1422/DAC1423).

Data-Acquisition Subsystems (including programmable-gain amplifiers, differential inputs, etc.).

Digital Panel Instruments (with isolation, low-level signal-handling capability, digital readout and BCD system output: scanning multi-channel voltmeters, intelligent thermocouple thermometers, low-cost digital thermometers, etc.).

Microcomputer Interface Boards (with input multiplexing and programmable gain, 4-to-20mA output options, etc.).

μMAC-4000 Single-Board Intelligent Measurement-and-Control Subsystems (with direct sensor inputs, isolation, signal conditioning, microcomputer-based linearization, ASCII 20mA/RS-232C communications, on-board power supply, and digital I/O).

MACSYM Complete BASIC-Programmable Minicomputer-Based Measurement-And-Control SYsteMs (with a wide selection of input signal conditioning cards and direct connection to sensor field wiring).

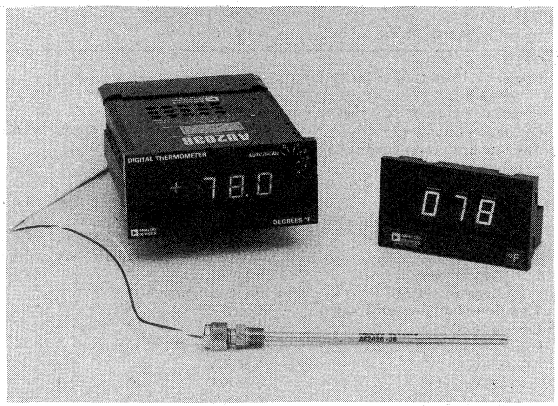
[1] Many of these issues are discussed in *Transducer Interfacing Handbook, a guide to analog signal conditioning,* published by Analog Devices, Inc., 1980, $14.50, available from P.O. Box 796, Norwood MA 02062.

ANALOG DEVICES

General Purpose Temperature Probe

AC2626

FEATURES
Linear Current Output: 1μA/K
Wide Range: -55°C to +150°C
Laser Trimmed Sensor (AD590) to ±1.0°C Calibration Accuracy (AC2626L)
Excellent Linearity: ±0.4°C Over Full Range (AC2626L)
6 Inch or 4 Inch Standard, Stainless Steel Sheath
3/16 Inch in Outside Diameter
3 Feet Teflon Coated Lead Wire
Wide Power Supply Range +4V to +30V
Low Cost
Fast Response: 2 Seconds (In Stirred Water)
Sensor Isolated From Sheath



9

PRODUCT DESCRIPTION

The AC2626 is a stainless steel tubular probe measuring 3/16 inch (4.76mm) in outside diameter and is available in 6 inch (152.4mm) or 4 inch (101.6mm) lengths. Based on the new AD590F, the probe is available in linearity grades of 0.4°C, 0.8°C or 1.5°C.

The probe is designed for both liquid and gaseous immersion applications as well as temperature measurements in refrigeration or any general temperature monitoring application.

For taking measurements in pipes or other closed vessels, the AC2629 compression fitting is available. The AC2629 may be applied anywhere along the probe and is supplied in two materials. The low cost AC2629B is constructed of brass and the higher priced AC2629SS is made of stainless steel.

PRODUCT HIGHLIGHTS

The AC2626 is based on the AD590 temperature transducer, a two terminal integrated circuit which produces an output current linearly proportional to absolute temperature.

Costly linearization circuitry, precision voltage amplifiers, resistance measuring circuitry and cold junction compensation are not needed in applying the AC2626.

Due to the high impedance current output of the AD590, the AC2626 is particularly useful in remote sensing applications, because of its insensitivity to voltage drops over lines. The output characteristics also make the AC2626 easy to multiplex.

In addition to temperature measurement, applications include temperature compensation, biasing proportional to absolute temperature, flow rate measurement, level detection of fluids and anemometry.

DIRECT INTERFACE PRODUCTS

For display and/or control applications, two companion products are available. The AD2038, 6 channel digital thermometer, and the AD2040, low cost temperature indicator, were designed to be used in conjunction with the AC2626.

1. The AD2038 is a low cost, ac line powered 6 channel digital scanning thermometer designed to interface to printers, computers, serial data transmitters, etc., for display, control, logging or transmission of multi-point temperature data. Channel selection is made via three methods: manual, using the switch provided on the front; auto/scan, where the AD2038 cycling on an internal clock can continually scan the six input channels or external selection, where control inputs provided on the rear connector enable channel selection via external BCD coding.
2. The AD2040 is a low cost, 3 digit temperature indicator. An internal precision voltage reference, resistor network and span and zero adjusts allow the AD2040 to read out directly in °C, °F, K or R. User selectable readout as well as all other connections, i.e., +5V dc power and AC2626 interface are all made via the terminal block on the rear.

APPLICATION HINTS

1. Under all operating conditions, a minimum 4V dc must be present across the AC2626.
2. Use of twisted pair wiring is recommended, particularly for remote applications or in high noise environments. Shielded wire is desirable in severe noise environments.
3. For the lowest cost impact, the J and K grades are recommended. Where probe interchangeability is desired, grade L is recommended.

SPECIFICATIONS (typical @ +25°C and +5V unless otherwise specified)

MODEL	AC2626J	AC2626K	AC2626L
ABSOLUTE MAXIMUM RATINGS[1]			
Forward Voltage (V_S)	+44V	*	*
Reverse Voltage (V_S)	-20V	*	*
Breakdown Voltage (Case to Leads)	±200V	*	*
Rated Performance Temp. Range	-55°C to +150°C	*	*
Storage Temperature Range	-60°C to +160°C	*	*
POWER SUPPLY			
Operating Voltage Range	+4V to +30V	*	*
OUTPUT			
Nominal Current Output @ +25°C (298.2°K)	298.2µA	*	*
Nominal Temperature Coefficient	1µA/°C	*	*
Calibration Error @ +25°C	±5.0°C max	±2.5°C max	±1.0°C max
Absolute Error (over rated performance temperature range)			
Without External Calibration Adjustment	±10.0°C max	±5.5°C max	±3.0°C max
With +25°C Calibration Error Set to Zero	±3.0°C max	±2.0°C max	±1.6°C max
Nonlinearity	±1.5°C max	±0.8°C max	±0.4°C max
Repeatability[2]	0.1°C	*	*
Long Term Drift[3]	0.1°C max/month	*	*
Time Constant[4] (in stirred water)	2 sec.	*	*
Current Noise	40pA$\sqrt{Hz}$	*	*
Power Supply Rejection			
+4V≤V_S≤+5V	0.5µA/V	*	*
+5V≤V_S≤+15V	0.2µA/V	*	*
+15V≤V_S≤+30V	0.1µA/V	*	*
Electrical Turn-On Time	20µs	*	*
+ Lead Color	yellow	orange	blue

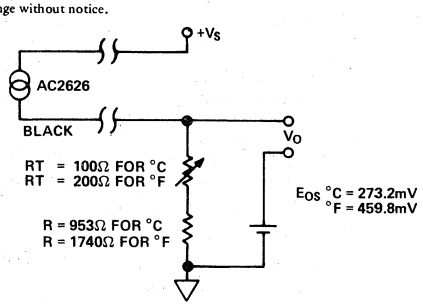
ORDERING GUIDE

AC2626
- GRADE: J, K, L — ENTER
- LENGTH: 4, 6 — ENTER

AC2629
- BRASS: B
- TYPE 316 STAINLESS: SS — ENTER

NOTES
[1] Maximum safe recommended pressure: 7500psi (5.17×10^4 Kpa).
[2] Maximum deviation between +25°C readings after temperature cycling between -55°C and +150°C; guaranteed, not tested.
[3] Conditions: constant +5V, constant +125°C; guaranteed, not tested.
[4] The time constant is defined as the time required to reach 63.2% of an instantaneous temperature change.
*Specifications same as AC2626J.
Specifications subject to change without notice.

CALIBRATION



For most applications, a single point calibration is sufficient. With the probe at a known temperature, adjust R_T so that V_O corresponds to the known temperature.

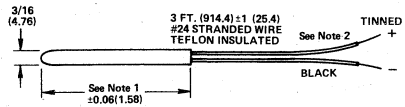
If more detailed information is desired, see the AD590 data sheet and application note.

MECHANICAL OUTLINE

Dimensions shown in inches and (mm)

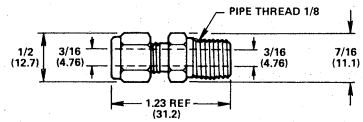
AC2626

3/16 STAINLESS STEEL TUBING
FILLED WITH THERMALLY CONDUCTIVE EPOXY



AC2629

STAINLESS STEEL TYPE 316
COMPRESSION FITTING (See Note 3)



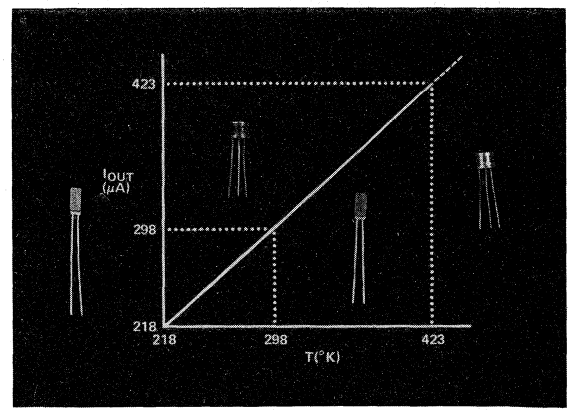
NOTE 1 Probes are available in 4-inch or 6-inch lengths.
NOTE 2 + lead wire is color coded: J, yellow; K, orange; L, blue.
NOTE 3 When assembling compression fitting (AC2629) to probe, tighten the 1/2" nut 3/4's of a turn from finger tight.

ANALOG DEVICES

Two-Terminal IC Temperature Transducer

AD590*

FEATURES
Linear Current Output: 1μA/°K
Wide Range: -55°C to +150°C
Probe Compatible Ceramic Sensor Package
Two-Terminal Device: Voltage In/Current Out
Laser Trimmed to ±0.5°C Calibration Accuracy (AD590M)
Excellent Linearity: ±0.3°C Over Full Range Range (AD590M)
Wide Power Supply Range: +4V to +30V
Sensor Isolation from Case
Low Cost



9

PRODUCT DESCRIPTION

The AD590 is a two-terminal integrated circuit temperature transducer which produces an output current proportional to absolute temperature. For supply voltages between +4V and +30V the device acts as a high impedance, constant current regulator passing 1μA/°K. Laser trimming of the chip's thin film resistors is used to calibrate the device to 298.2μA output at 298.2°K (+25°C).

The AD590 should be used in any temperature sensing application below +150°C in which conventional electrical temperature sensors are currently employed. The inherent low cost of a monolithic integrated circuit combined with the elimination of support circuitry makes the AD590 an attractive alternative for many temperature measurement situations. Linearization circuitry, precision voltage amplifiers, resistance measuring circuitry and cold junction compensation are not needed in applying the AD590.

In addition to temperature measurement, applications include temperature compensation or correction of discrete components, biasing proportional to absolute temperature, flow rate measurement, level detection of fluids and anemometry. The AD590 is available in chip form making it suitable for hybrid circuits and fast temperature measurements in protected environments.

The AD590 is particularly useful in remote sensing applications. The device is insensitive to voltage drops over long lines due to its high impedance current output. Any well-insulated twisted pair is sufficient for operation hundreds of feet from the receiving circuitry. The output characteristics also make the AD590 easy to multiplex: the current can be switched by a CMOS multiplexer or the supply voltage can be switched by a logic gate output.

***Covered by Patent No. 4,123,698**

PRODUCT HIGHLIGHTS

1. The AD590 is a calibrated two terminal temperature sensor requiring only a dc voltage supply (+4V to +30V). Costly transmitters, filters, lead wire compensation and linearization circuits are all unnecessary in applying the device.
2. State-of-the-art laser trimming at the wafer level in conjunction with extensive final testing insures that AD590 units are easily interchangeable.
3. Superior interference rejection results from the output being a current rather than a voltage. In addition, power requirements are low (1.5mW's @ 5V @ +25°C). These features make the AD590 easy to apply as a remote sensor.
4. The high output impedance (>10MΩ) provides excellent rejection of supply voltage drift and ripple. For instance, changing the power supply from 5V to 10V results in only a 1μA maximum current change, or 1°C equivalent error.
5. The AD590 is electrically durable: it will withstand a forward voltage up to 44V and a reverse voltage of 20V. Hence, supply irregularities or pin reversal will not damage the device.
6. The device is hermetically sealed in both a ceramic sensor package and in to TO-52 package. MIL-STD-883 processing to level B is available and, for large unit volumes, special accuracy requirements over limited temperature ranges can be satisfied by selections at final test. The device is also available in chip form.

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be found in Volume I, page 9-5.

SPECIFICATIONS (typical @ +25°C and V_S = 5V unless otherwise noted)

MODEL	AD590I	AD590J	AD590K	AD590L	AD590M
ABSOLUTE MAXIMUM RATINGS					
Forward Voltage (E+ to E–)	+44V	*	*	*	*
Reverse Voltage (E+ to E–)	–20V	*	*	*	*
Breakdown Voltage (Case to E+ or E–)	±200V	*	*	*	*
Rated Performance Temperature Range[1]	–55°C to +150°C	*	*	*	*
Storage Temperature Range[1]	–65°C to +155°C	*	*	*	*
Lead Temperature (Soldering, 10 sec)	+300°C	*	*	*	*
POWER SUPPLY					
Operating Voltage Range	+4V to +30V	*	*	*	*
OUTPUT					
Nominal Current Output @ +25°C (298.2°K)	298.2μA	*	*	*	*
Nominal Temperature Coefficient	1μA/°K	*	*	*	*
Calibration Error @ +25°C	±10.0°C max	±5.0°C max	±2.5°C max	±1.0°C max	±0.5°C max
Absolute Error[2] (over rated performance temperature range)					
Without External Calibration Adjustment	±20.0°C max	±10.0°C max	±5.5°C max	±3.0°C max	±1.7°C max
With +25°C Calibration Error Set to Zero	±5.8°C max	±3.0°C max	±2.0°C max	±1.6°C max	±1.0°C max
Nonlinearity	±3.0°C max	±1.5°C max	±0.8°C max	±0.4°C max	±0.3°C max
Repeatability[3]	±0.1°C max	*	*	*	*
Long Term Drift[4]	±0.1°C/month max	*	*	*	*
Current Noise	40pA$\sqrt{\text{Hz}}$	*	*	*	*
Power Supply Rejection					
+4V ≤ V_S ≤ +5V	0.5μA/V	*	*	*	*
+5V ≤ V_S ≤ +15V	0.2μA/V	*	*	*	*
+15V ≤ V_S ≤ +30V	0.1μA/V	*	*	*	*
Case Isolation to Either Lead	$10^{10}\Omega$	*	*	*	*
Effective Shunt Capacitance	100pF	*	*	*	*
Electrical Turn-On Time[5]	20μs	*	*	*	*
Reverse Bias Leakage Current[6] (Reverse Voltage = 10V)	10pA	*	*	*	*
PACKAGE OPTION[7]					
"H" Package: TO-52	AD590IH	AD590JH	AD590KH	AD590LH	AD590MH
"F" Package: Flat Pack (F2A)	AD590IF	AD590JF	AD590KF	AD590LF	AD590MF

*Specifications same as AD590I

[1] The AD590 has been used at –100°C and +200°C for short periods of measurement with no physical damage to the device. However, the absolute errors specified apply to only the rated performance temperature range.

[2] See section in Volume I on temperature sensor specifications for explanation of error components. Note that ±1°C error is the equivalent of ±1μA error.

[3] Maximum deviation between +25°C readings after temperature cycling between –55°C and +150°C; guaranteed not tested.

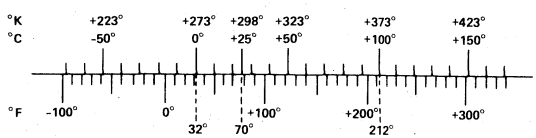
[4] Conditions: constant +5V, constant +125°C; guaranteed, not tested.

[5] Does not include self heating effects.

[6] Leakage current doubles every 10°C.

[7] See Section 20 for package outline information, Volume I.

Specifications subject to change without notice.



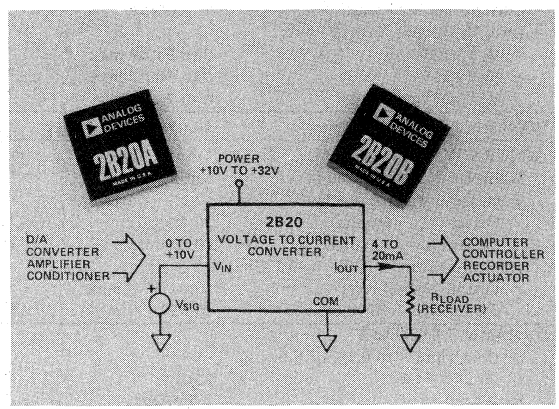
TEMPERATURE SCALE CONVERSION EQUATIONS

$$^\circ C = \frac{5}{9}(^\circ F - 32) \qquad ^\circ K = ^\circ C + 273.15$$

$$^\circ F = \frac{9}{5}\,^\circ C + 32 \qquad ^\circ R = ^\circ F + 459.7$$

High Performance, 4-20mA Output Voltage-to-Current Converter

MODEL 2B20



FEATURES

- Complete, No External Components Needed
- Small Size: 1.1″ x 1.1″ x 0.4″ Module
- Input: 0 to +10V; Output: 4 to 20mA
- Low Drift: 0.005%/°C max; Nonlinearity: 0.005% max (2B20B)
- Wide Temperature Range: -25°C to +85°C
- Single Supply: +10V to +32V
- Meets ISA Std 50.1 for Type 3, Class L and U, Nonisolated Current Loop Transmitters

APPLICATIONS

- Industrial Instrumentation and Control Systems
- D/A Converter – Current Loop Interface
- Analog Transmitters and Controllers
- Remote Data Acquisition Systems

GENERAL DESCRIPTION

Model 2B20 is a complete, modular voltage-to-current converter providing the user with a convenient way to produce a current output signal which is proportional to the voltage input. The nominal input voltage range is 0 to +10V. The output current range is 4 to 20mA into a grounded load.

Featuring low drift (0.005%/°C max, 2B20B) over the -25°C to +85°C temperature range and single supply operation (+10V to +32V), model 2B20 is available in two accuracy grades. The 2B20B offers precision performance with nonlinearity error of 0.005% (max) and guaranteed low offset error of ±0.1% max and span error of ±0.2% max, without external trims. The 2B20A is an economical solution for applications with lesser accuracy requirements, featuring nonlinearity error of 0.025% (max), offset error of ±0.4% (max), span error of ±0.6% (max), and span stability of 0.01%/°C max.

The 2B20 is contained in a small (1.1″ x 1.1″ x 0.4″), rugged, epoxy encapsulated package. For maximum versatility, two signal input (V_{IN1} and V_{IN2}) and two reference input (REF_{IN1} and REF_{IN2}) terminals are provided. Utilizing terminals V_{IN1} and REF_{IN1} eliminates the need for any external components, since offset and span are internally calibrated. If higher accuracy (up to ±0.01%) is required, inputs V_{IN2} and REF_{IN2} with series trim potentiometers may be utilized.

APPLICATIONS

Model 2B20 has been designed for applications in process control and monitoring systems to transmit information between subsystems or separated system elements. The 2B20 can serve as a transmission link between such elements of process control system as transmitters, indicators, controllers, recorders, computers, actuators and signal conditioners.

In a typical application, model 2B20 may act as an interface between the D/A converter output of a microcomputer based system and a process control device such as a variable position valve. Another typical application of the 2B20 may be as a current output stage of a proportional controller to interface devices such as current-to-position converters and current-to-pneumatic transducers.

DESIGN FEATURES AND USER BENEFITS

Process Signal Compatibility: To provide output signal compatibility, the 2B20 meets the requirements of the Instrument Society of America Standard S50.1, "Compatibility of Analog Signals for Electronic Industrial Process Instruments" for Type 3, Class L and U, nonisolated current loop transmitters.

External Reference Use: For increased flexibility, when ratiometric operation is desired, the 2B20 offers a capability of connecting an external reference (i.e., from multiplying D/A converter) to the REF_{IN2} terminal.

Wide Power Supply Range: A wide power supply range (+10V to +32V dc) allows for operation with either a +12V battery, a +15V powered data acquisition system, or a +24V powered process control instrumentation.

SPECIFICATIONS (typical @ +25°C and V_S = +15V, unless otherwise noted)

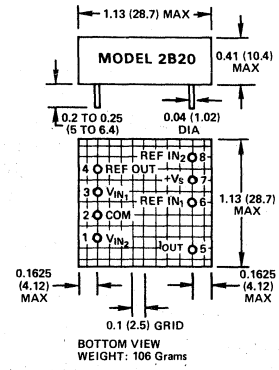
Model	2B20A	2B20B
INPUT SPECIFICATIONS		
Voltage Signal Range	0 to +10V	*
Input Impedance	10kΩ	*
OUTPUT SPECIFICATIONS		
Current Output Range[1]	4 to 20mA	*
Load Resistance Range[2]		
V_S = +12V	0 to 350Ω max	*
V_S = +15V	0 to 500Ω max	*
V_S = +24V	0 to 950Ω max	*
NONLINEARITY (% of Span)	±0.025% max	±0.005% max
ACCURACY[3]		
Warm-Up Time to Rated Specs	1 minute	*
Total Output Error @ +25°C[3,4]		
Offset (V_{IN} = 0 volts)	±0.4% max	±0.1% max
Span (V_{IN} = +10 volts)	±0.6% max	±0.2% max
vs. Temperature (-25°C to +85°C)		
Offset (V_{IN} = 0 volts)	±0.01%/°C max	±0.005%/°C max
Span (V_{IN} = +10 volts)	±0.01%/°C max	±0.005%/°C max
DYNAMIC RESPONSE		
Settling Time – to 0.1% of F.S. for 10V Step	25μs	*
Slew Rate	2.5mA/μs	*
REFERENCE INPUT[5]		
Voltage	+2.5V dc	*
Input Impedance	10kΩ	*
POWER SUPPLY		
Voltage, Rated Performance	+15V dc	*
Voltage, Operating	+10V to +32V dc max	*
Supply Change Effect (% of Span)[6]		
on Offset	±0.005%/V	*
on Span	±0.005%/V	*
Supply Current	6mA + I_{LOAD}	*
TEMPERATURE RANGE		
Rated Performance	-25°C to +85°C	*
Storage	-55°C to +125°C	*
CASE SIZE	1.125" X 1.125" X 0.4"	*

*Specifications same as 2B20A.
[1] Current output sourced into a grounded load over a supply voltage range of +10V to +32V.
[2] See Figure 1 for the maximum load resistance value over the power supply range.
[3] Accuracy is guaranteed with no external trim adjustments when REF_{IN} is connected to REF_{OUT}.
[4] All accuracy is specified as % of output span where output span is 16mA (±0.1% = ±0.016mA output error).
[5] Reference input is normally connected to the reference output (+2.5V dc).
[6] Optional trim pots may be used for calibration at each supply voltage.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



MATING SOCKET: AC1016

LOAD RESISTANCE RANGE

The load resistance is the sum of the resistances of all connected receivers and the connection lines. The 2B20 operating load resistance is power supply dependent and will decrease by 50 ohms for each 1 volt reduction in the power supply. Similarly, it will increase by 50 ohms per volt increase in the power supply, but must not exceed the safe voltage capability of the unit.

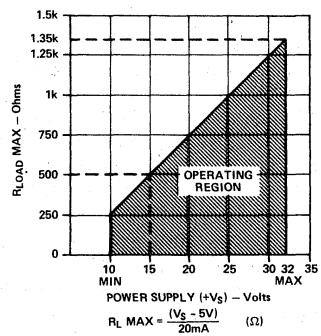


Figure 1. Maximum Load Resistance vs. Power Supply

PRINCIPLE OF OPERATION

The design of the 2B20 is comprised of high performance op amps, precision resistors and a high stability voltage reference to develop biasing and output drive capability. The 2B20 is designed to operate from a single positive power supply over a wide range of +10V to +32V dc and accepts a single ended, 0 to +10V voltage input. The internal reference has nominal output voltage of +2.5V (REF_{OUT}) and is used to develop 4mA output current for a zero volts input when REF_{IN} is connected to REF_{OUT}.

The output stage of the 2B20 utilizes a sensing resistor in the feedback loop, so the output current is linearly related to the voltage input and independent of the load resistance. There is no minimum resistance for the loads driven by the 2B20; it can drive even a short circuit with no damage to the unit. The maximum resistance of the load as seen by the unit (resistance of the load plus the resistance of the connecting wire) is limited. The maximum external loop resistance, R_L, is given by:

$$R_L\ (\Omega)\ \text{max} = \left(\frac{+V_S - 5V}{20mA}\right)$$

Figure 1 shows the operating region of the 2B20. The load must be returned to power supply common. The voltage appearing between I_{OUT} (pin 5) and COM (pin 2) should not exceed $V_{max} = +V_S - 5V$. Exceeding this value (up to +32V dc) will not damage the unit, but it will result in a loss of linearity.

The basic connections of the 2B20 are shown in Figure 2.

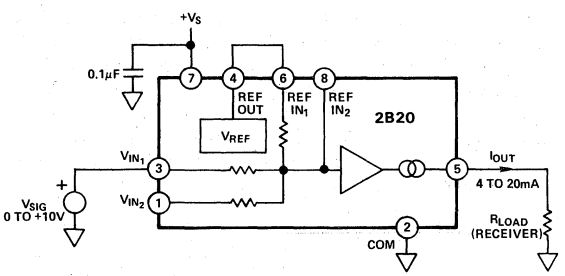


Figure 2. Basic Connections Diagram

OPTIONAL CALIBRATION AND TRIM PROCEDURE

Model 2B20's factory trimmed offset error is ±0.1% max and span error is ±0.2% max (2B20B). In most applications, further trimming will not be required. If it is necessary to obtain calibrated accuracy of up to ±0.01%, or, if a high signal source resistance (with respect to 10kΩ) introduces calibration error, inputs V_{IN2} and REF_{IN2} and optional trim pots should be used with V_{IN1} and REF_{IN1} open. To perform external trims, connect 500Ω potentiometers in series with V_{IN2} (span trim) and REF_{IN2} (offset trim) as shown in Figure 3. Adjust span pot, monitoring voltage drop across R_{LOAD}, to obtain an output voltage of 5.000V (I_{OUT}=20mA) for a +10V input. Next, with 0 volts input, adjust offset pot to obtain 1.000V output (I_{OUT}=4mA). Check both offset and span and retrim if necessary after each adjustment.

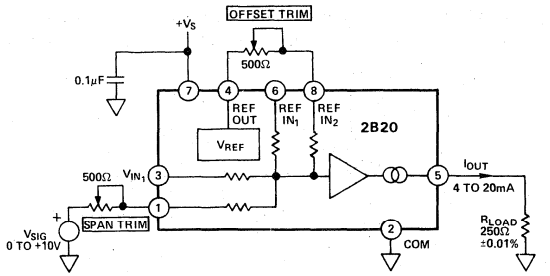


Figure 3. Model 2B20 Connections Using Optional Offset and Span Trims

CONNECTING THE 2B20 FOR 0 TO 10mA OUTPUT

The 2B20 may be utilized in applications requiring 0 to 10mA current output for a 0 to 10V input voltage range. To obtain 0mA output for 0V input, REF_{IN1} (pin 6) and REF_{IN2} (pin 8) terminals should be left open. A typical output current error for a zero volts input (without trimming) is 0.1mA. The 2B20 span calibration may be adjusted by a 1kΩ potentiometer in series with the V_{IN2} input. Basic connections of the 2B20 used to obtain a 0 to 10mA output are shown in Figure 4a.

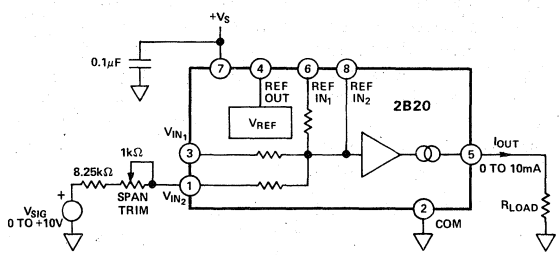


Figure 4a. Model 2B20 Connected for 0 to 10mA Output Range

CONNECTING THE 2B20 FOR 0 TO 20mA OUTPUT

The 2B20 may also be configured for use in applications requiring 0 to 20mA output for a 0 to +10 volt input range. REF_{IN1} (pin 6) is left open, and REF_{IN2} (pin 8) is connected to V_{IN_2} (pin 1) through a 32.4kΩ resistor. The typical output current error for 0V input (without trimming) is 0.1mA. The 2B20 span may be adjusted by a 2kΩ potentiometer in series with the V_{IN2} input to provide 9% FSR adjustment range. Basic connections for 0-20mA operation are shown in Figure 4b.

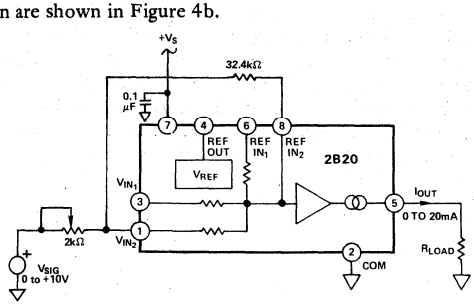


Figure 4b. Model 2B20 Connected for 0 to 20mA Output Range

OUTPUT PROTECTION

In many industrial applications, it may be necessary to protect the 4 to 20mA output from accidental shorts to ac line voltages. The circuit shown in Figure 5 can be used for this purpose. The maximum permissible load resistance will be lowered by a fuse resistance value when protection circuitry is utilized.

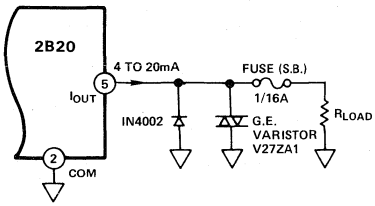


Figure 5. Output Protection Circuitry Connections

APPLICATIONS

Interfacing Voltage Output D/A Converters: The 2B20 is well suited in applications requiring 4 to 20mA output from D/A converters. The voltage necessary to power the current loop can be derived from the same +15V supply that is used to power the converter. The D/A converter, such as the 12-bit AD DAC80, should be connected for operation on the unipolar 0 to +10V output range. This is shown in Figure 6. After the load resistor connection has been made, the current loop can be calibrated using the offset and span adjustment potentiometers associated with the 2B20 (or the AD DAC80). First, a digital input code of all ones is loaded into the D/A, and the offset adjustment potentiometer is adjusted for a current output of exactly 4mA. Then, a digital code of all 0s is loaded into the D/A, and the span adjustment potentiometer is adjusted for a voltage across the load that corresponds to a current of 20mA −1LSB = 19.9961mA.

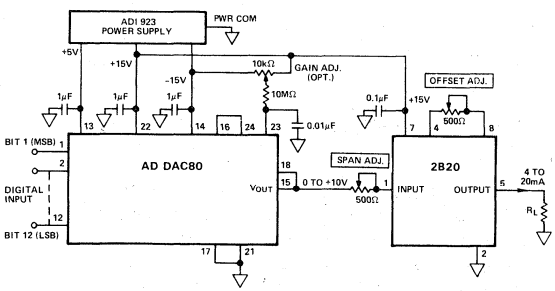


Figure 6. AD DAC80 – 4 to 20mA Current Loop Interface

Interfacing Current Output D/A Converters: To interface current output D/A converters, such as the AD562, a circuit configuration illustrated in Figure 7 should be used. Since the AD562 is designed to operate with an external +10V reference, the same external reference may be utilized by the 2B20 for ratiometric operation. The output of the AD562 is used to drive the summing junction of an operational amplifier to produce an output voltage. Using the internal feedback resistor of the AD562 provides a 0 to +10V output voltage range suitable to drive the 2B20.

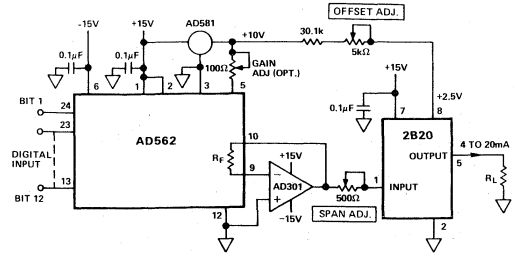


Figure 7. 12-Bit – 4 to 20mA Current Loop Interface

Microcomputer – Current Loop Interface: Figure 8 shows a typical application of the 2B20 in a multichannel microcomputer analog output system. When a microcomputer is to control a final control element, such as a valve positioner, servomechanism or motor, an analog output board with 4 to 20mA outputs is often necessary. The output boards typically have from one to eight channels, each with its own D/A converter. The 2B20, in a compact package, allows for an easy installation without any additional components and offers a 12-bit system compatible performance.

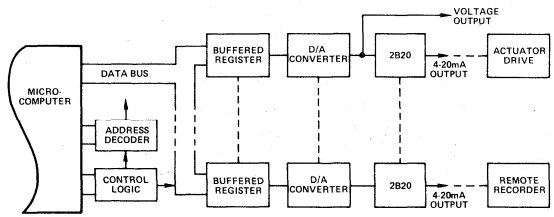


Figure 8. Microcomputer Analog Output Subsystem

Pressure Control System: In Figure 9, model 2B20 is used in a proportional pressure control system. The 3-15psi working pressure of a system is monitored with a pressure transducer interfaced by the model 2B31 signal conditioner. The high level voltage output of the 2B31 is converted to a 4 to 20mA to provide signal to the limit alarm and proportional control circuitry. A current-to-position converter controlling a motorized valve completes the pressure-control loop.

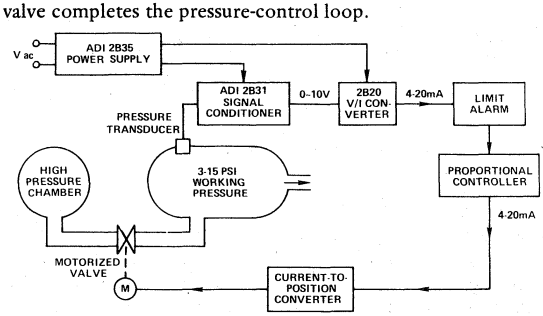


Figure 9. Proportional Pressure Control System

Isolated 4 to 20mA Output: For applications requiring up to ±1500V dc input to output isolation, consider using Analog Devices' model 2B22 isolated voltage-to-current converter.

High Performance, Isolated Voltage-to-Current Converter

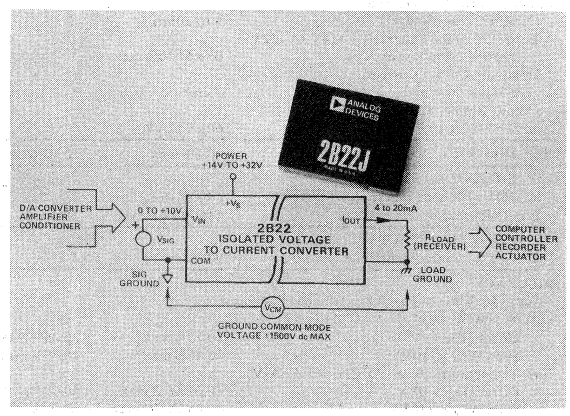
MODEL 2B22

FEATURES

Wide Input Range: 0 to +1V to 0 to +10V
Standard Output Range: 4 to 20mA
High CMV Input/Output Isolation: 1500V dc Continuous
Low Nonlinearity: 0.05% max, 2B22L
Low Span Drift: 0.005%/°C max, 2B22L
Single Supply: +14V to +32V
Meets IEEE Std 472: Transient Protection (SWC)
Meets ISA Std 50.1: Isolated Current Loop Transmitters

APPLICATIONS

Industrial Instrumentation and Process Control
Ground Loop Elimination
High Voltage Transient Protection
D/A Converter — Current Loop Interface
Analog Transmitters and Controllers
Remote Data Acquisition Systems



GENERAL DESCRIPTION

Model 2B22 is a high performance, compact voltage-to-current converter offering 1500V dc input to output isolation in interfacing standard process signals. The input stage of the model 2B22 is single resistor programmable to accept voltage ranges from 0 to +1V to 0 to +10V. The isolated output current range is 4 to 20mA, and the 2B22 can be operated with 0 to 1000Ω grounded or floating loads.

Using modulation techniques with transformer isolation for reliable performance, the 2B22 is available in three accuracy selections offering guaranteed nonlinearity error (2B22L: ±0.05% max, 2B22K: ±0.1% max, and 2B22J: ±0.2% max) and guaranteed low span drift: ±0.005%/°C max, ±0.01%/°C max, and ±0.015%/°C max, respectively. The internally trimmed span and offset errors are ±0.1% max for the 2B22L and ±0.25% max for the 2B22J/2B22K. Both span and offset are adjustable by the optional external potentiometers.

Featuring a wide range, single supply operation (+14V to +32V), the 2B22 provides isolated +28V loop power and is capable of delivering rated current into an external 0 to 1000Ω load resistance. The unique output stage configuration also allows the user to utilize an optional external loop power supply to interface systems designed for a two-wire operation.

APPLICATIONS

Model 2B22 has been specifically designed for high accuracy applications in process control and monitoring systems to offer complete galvanic isolation and protection against damage from transients and fault voltages in transmitting information between subsystems or separated system elements. The 2B22 meets the requirements of the Instrument Society of America Std. 50.1 "Compatibility of Analog Signals for Electronic Industrial Process Instruments" for Type 4, Class U isolated current loop transmitters.

In the industrial environment, model 2B22 can serve as a transmission link between such system elements as transmitters, indicators, controllers, recorders, computers, actuators and signal conditioners. In data acquisition and control systems, the 2B22 may act as an isolated interface between the D/A converter output of a microcomputer and standard 4 to 20mA analog loops.

DESIGN FEATURES AND USER BENEFITS

High Reliability: Model 2B22 is a conservatively designed, compact, epoxy encapsulated module capable of reliable operation in harsh environments. To assure high reliability, the 2B22 has a calculated MTBF of over 270,000 hours and has been designed to meet the IEEE Standard for Transient Voltage Protection (472-1974: Surge Withstand Capability).

Process Signal Compatibility: The versatile input stage design with a single resistor gain adjustment enables the 2B22 to accept any one of the standard inputs—0-1V, 0-10V, 1-5V; or 1-5mA, 4-20mA, 10-50mA; and provide standard, isolated 4-20mA output.

Isolated Loop Power: Internal 28V dc loop supply, completely isolated from the input power terminals (±1500V dc isolation), provides the capability to drive 0 to 1000Ω loads and eliminates the need for an external dc/dc converter.

SPECIFICATIONS (typical @ +25°C and V_S = +15V unless otherwise noted)

Model	2B22J	2B22K	2B22L
INPUT SPECIFICATIONS			
Voltage Signal Range, G = 1.6mA/V	0 to +10V	*	*
G = 16mA/V	0 to +1V	*	*
Gain Range	1.6 to 16mA/V	*	*
Maximum Safe Input	+15V	*	*
Input Impedance	10MΩ	*	*
OUTPUT SPECIFICATIONS			
Current Output Range	4 to 20mA	*	*
Load Resistance Range, V_S = +14V to +32V, Internal Loop Power	0 to 1000Ω max	*	*
Maximum Output Current, @ Input Overload	25mA	*	*
Output Ripple, 100Hz Bandwidth G = 1.6mA/V	60μA pk-pk	*	*
NONLINEARITY (% of Span)	±0.2% max	±0.1% max	±0.05% max
CMV, INPUT TO OUTPUT			
ac, 60Hz, 1 Minute Duration	1500V rms	*	*
Continuous, ac or dc	±1500V pk max	*	*
CMR, INPUT TO OUTPUT			
60Hz, 1kΩ Source Imbalance	90dB	*	*
ACCURACY[1]			
Warm Up Time to Rated Performance 5 Minutes			
Total Output Error @ +25°C[1,2]			
Offset (V_{IN} = 0V)	±0.25% max	±0.25% max	±0.1% max
Span (V_{IN} = +10V)	±0.25% max	±0.25% max	±0.1% max
vs. Temperature (0 to +70°C, G = 1.6mA/V)			
Offset (V_{IN} = 0V)	±0.01%/°C max	±0.005%/°C max	±0.0025%/°C max
Span (V_{IN} = +10V)	±0.015%/°C max	±0.01%/°C max	±0.005%/°C max
vs. Temperature (0 to +70°C)			
Offset (V_{IN} = 0V, G = 1.6mA/V to 16mA/V)	±0.01%/°C	±0.005%/°C	±0.0025%/°C
Span (G = 1.6mA/V to 16mA/V)[3]	±0.015%/°C	±0.01%/°C	±0.005%/°C
DYNAMIC RESPONSE			
Settling Time – to 0.1% of F.S. for 10V Step	300μs	*	*
Slew Rate	0.06mA/μs	*	*
REFERENCE INPUT			
Voltage	+2.5V dc	*	*
Input Impedance	6kΩ	*	*
OSCILLATOR			
Frequency, Internal Oscillator	100kHz ± 10%	*	*
External Sync Input			
Frequency	100kHz ± 10% max	*	*
Waveform	Square wave, 50% duty cycle	*	*
Voltage	20V p-p	*	*
POWER SUPPLY			
Voltage, Rated Performance	+15V dc	*	*
Voltage, Operating	+14V to +32V dc	*	*
Supply Current (at Full Scale Output)			
Using Internal Loop Power	100mA	*	*
Using External Loop Power	50mA	*	*
Supply Change Effect (% of Span)			
on Offset (V_{IN} = 0V)	±0.0005%/V	*	*
on Span (V_{IN} = +10V)	±0.0005%/V	*	*
TEMPERATURE RANGE			
Rated Pertormance	0 to +70°C	*	*
Operating	-25°C to +75°C	*	*
Storage	-55°C to +85°C	*	*
CASE SIZE	2.2" X 3" X 0.6"	*	*

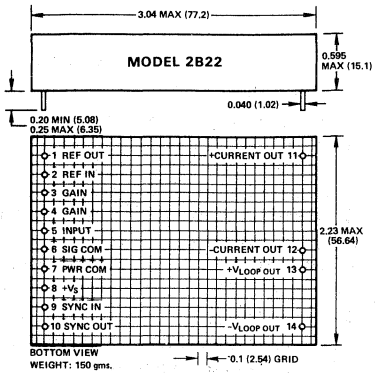
*Specifications same as 2B22J.

NOTES
[1] Accuracy is guaranteed at G = 1.6mA/V with no external trim adjustments when connected as shown in Figure 1.
[2] All accuracy is % of span where span is 16mA (±0.1% = ±0.016mA error).
[3] Span T.C. for gains higher than 1.6mA/V is R_G dependent – a low T.C. (±10ppm/°C) R_G is recommended for best performance.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

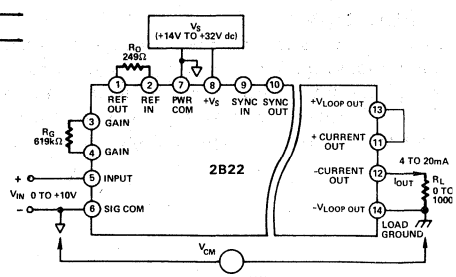
Dimensions shown in inches and (mm).



MATING SOCKET: AC1579

INTERCONNECTION DIAGRAM

Model 2B22 can be applied directly to achieve rated performance as shown in Figure 1 below. The input stage gain of 1.6mA/V, to convert a 0 to +10V signal into a 4 to 20mA output current, is obtained with the values shown. A single polarity power supply (+14V to +32V dc) should be connected to pin 8. To eliminate ground loops, the user should ensure that the signal return (common) lead does not carry the power supply current. Power common (pin 7) and signal common (pin 6) should be tied at the power supply common terminal. The voltage difference between pins 6 and 7 should not exceed 0.2V. An internal dc-dc converter provides isolated output loop power (pins 13 and 14), which is connected externally to the current output terminals (pins 11 and 12) and a load resistance. The standard 4 to 20mA current output signal is delivered into any external load between zero and 1000Ω.



NOTE: Resistors R_O and R_G are 1%, 50ppm/°C Metal Film Type. Values shown are for G = 1.6mA/V. For G = 16mA/V, use 10ppm/°C R_G and 50ppm/°C R_O.

Figure 1. Basic Connections

FUNCTIONAL DESCRIPTION

The high performance of model 2B22 is derived from the carrier isolation technique which is used to transfer both signal and power between the V/I converter's input circuitry and the output stage. High CMV isolation is achieved by the transformer coupling between the input amplifier, modulator section and the current output circuitry. The block diagram for model 2B22 is shown in Figure 2 below.

The 2B22 produces an isolated 4 to 20mA output current which is proportional to the voltage input and independent of the load resistance. The input amplifier operates single-ended and accepts a positive voltage within 0 to +10V range. Gain can be set from 1.6mA/V to 16mA/V by changing the gain resistor R_G to accommodate input ranges from 0 to +1V (G = 16mA/V) to 0 to +10V (G = 1.6mA/V). The transfer function is $I_{OUT} = (4mA + G \times V_{IN})$.

An internal, high stability reference has nominal output voltage of +2.5V (REF OUT) and is used to develop a 4mA output current for a 0 volts input. The terminals REF OUT (pin 1) and REF IN (pin 2) should be connected via the offset setting resistor R_O. For ratiometric operation, an external reference voltage can be connected to the REF IN terminal.

The 2B22 is designed to operate from a single positive power supply over a wide range of +14V to +32V dc. An internal dc-dc converter provides isolated +28V loop power which is independent of $+V_S$. The maximum resistance of the load R_L (resistance of the receivers plus the resistance of the connecting wire) is 1000Ω. Since the loop power is derived from the input side, the current capability of the power supply ($+V_S$) must be 100mA min to supply full output signal current.

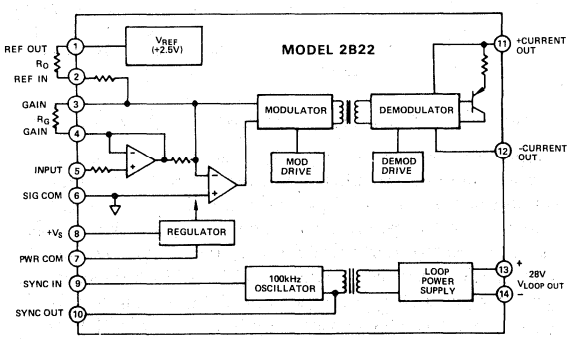


Figure 2. Block Diagram – Model 2B22

OPTIONAL TRIM ADJUSTMENTS

Model 2B22 is factory calibrated for a 0 to +10V input range (G = 1.6mA/V). As shipped, the 2B22 meets its listed specifications without use of any external trim potentiometers. Additional trim adjustment capability, to reduce span and offset errors to ±0.05% max, is easily provided as shown in Figure 3. The span and offset trim pots are adjusted while monitoring the voltage drop across a precision (or known) load resistor. The following trim procedure is recommended:

1. Connect model 2B22 as shown in Figure 3.
2. Apply V_{IN} = 0 volts and adjust R_O (Offset Adjust) for V_{OUT} = +2V ± 4mV.
3. Apply V_{IN} = +10.00V and adjust R_G (Span Adjust) for V_{OUT} = +10V ± 4mV.

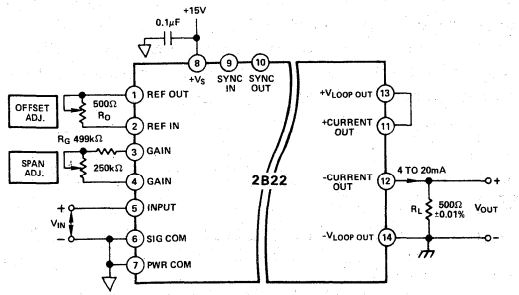


Figure 3. Optional Span and Offset Adjustment

GAIN AND OFFSET SETTING

The gain of the 2B22 is a scale factor setting that establishes the nominal conversion relationship to accommodate +1V to +10V full scale inputs (V_{IN}). The value of the gain setting resistor R_G is determined by: $R_G(k\Omega) = 6.314SF/(10.1 - SF)$ where SF is a scale factor equal to the value of V_{IN} F.S. Example: to convert a 0 to +1V input to the 4 to 20mA output, SF = 1 and R_G = 693Ω. Due to device tolerances, allowance should be made to vary R_G by ±5% using the potentiometer.

The value of the offset resistor R_O is independent from the gain setting and given by the relationship: $R_O(k\Omega) = 2.5(V_{REF} - 2.4)$ where V_{REF} is the reference voltage applied. For example, the reference provided by the 2B22 is +2.5V and therefore R_O = 250Ω. The accuracy of the R_O calculation from from the above formula is ±5%. When an external reference operation is desired (i.e. for ratiometric operation), connect the reference voltage via R_O to pin 2 and leave pin 1 open.

EXTERNAL LOOP POWER OPERATION

For maximum versatility, the 2B22's output stage is designed to operate from the optional, isolated external loop power supply. This feature allows the user to interface systems wired for a two-wire operation. As shown in Figure 4, the same wiring is used for loop power and output. The load resistance is connected in series with an external dc power supply (+6V to +32V), and the current drawn from the supply is the 4 to 20mA output signal. The input stage of the 2B22 still requires $+V_S$ power, but the current drain from $+V_S$ is limited to 50mA. Use of an external loop power may require gain and offset trimming to obtain specified accuracy. The maximum series load resistance depends on the loop supply voltage as shown in Figure 4.

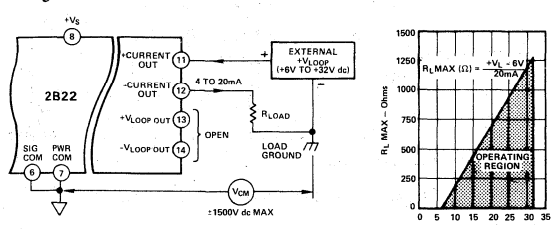


Figure 4. Optional External Loop Power Operation

SYNCHRONIZING MULTIPLE 2B22'S

In applications where multiple 2B22's are used in close proximity, radiated individual oscillator frequencies may cause "beat frequency" related output errors. These errors can be eliminated by synchronizing multiple units by connecting the SYNC OUT (pin 10) terminal to the SYNC IN (pin 9) terminal of the adjacent 2B22. The SYNC OUT terminal of this "slaved" unit can be used to drive another adjacent 2B22 (Figure 5). For best accuracy, each 2B22 should be retrimmed when synchronizing connections are used.

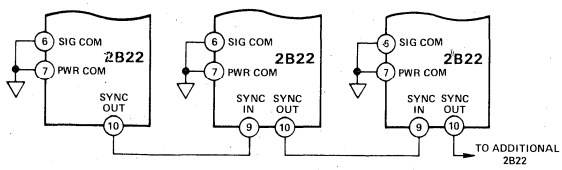


Figure 5. Multiple 2B22's Synchronization

OUTPUT PROTECTION

The current output terminals (pins 11 and 12) are protected from shorts up to +32V dc but in many industrial applications, it may be necessary to protect the 4 to 20mA output from accidental shorts to ac line voltages. The circuit shown in Figure 6 can be used for this purpose. The maximum permissible load resistance will be lowered by a fuse resistance value when protection circuitry is utilized.

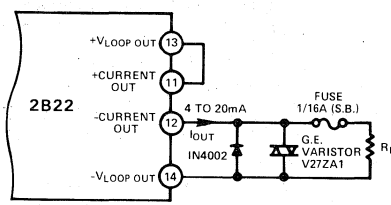


Figure 6. Output Protection Circuitry Connections

APPLICATIONS IN INDUSTRIAL MEASUREMENT AND CONTROL SYSTEMS

Process Signal Isolator: In process control applications, model 2B22 can be applied to interface standard process signals (e.g. 1 to 5mA, 4 to 20mA, 10 to 50mA, 1 to 5V) and convert them to isolated 4 to 20mA output. A typical hook-up of model 2B22 is illustrated in Figure 7, showing input resistor R_C converting the current from a remote loop to a voltage input, and a span adjustment resistor R_G. A value of R_C should be selected to develop a minimum of +1V signal with full scale input current applied. For example, a 50Ω resistor converts the 4 to 20mA current input to a 200mV to 1V voltage input, which the 2B22 isolates and converts to a 4 to 20mA output. The reference input (pin 2) is not connected since the process signal provides a desired offset.

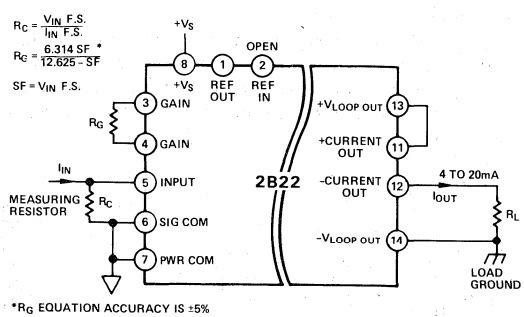


Figure 7. Process Signal Current Isolator

Isolated D/A Converter: Model 2B22 offers total ground isolation and protection from high voltage transients in interfacing D/A converters to standard 4 to 20mA current loops. This requirement is common in a microcomputer-based control system. The voltage necessary to power the current loop can be derived from the same +15V supply that is used to power the D/A converter. The D/A converter, such as the 12-bit AD DAC80, should be connected for operation on the unipolar 0 to +10V output range. This is shown in Figure 8. After the load resistor connection has been made, the current loop can be calibrated using the offset and span adjustment potentiometers associated with the 2B22. First, a digital input code of all one's is loaded into the D/A, and the offset adjustment potentiometer is adjusted for a current output of exactly 4mA. Then, a digital code of all zero's is loaded into the D/A, and the span adjustment potentiometer is adjusted for a voltage across the load that corresponds to a current of 20mA less 1LSB (19.9961mA).

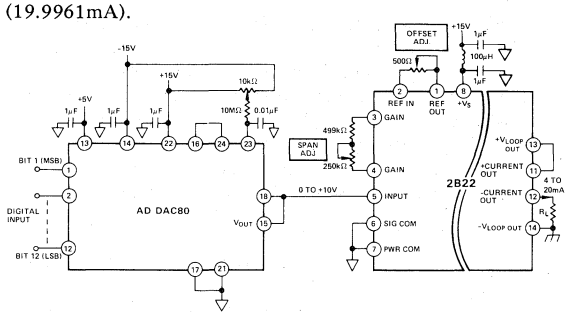


Figure 8. D/A Converter – Isolated 4 to 20mA Interface

Pressure Transmitter: In Figure 9, model 2B22 is used in a pressure transmitter application to provide complete input-output isolation and avoid signal errors due to ground loop currents. The process pressure is monitored with a strain gage type pressure transducer interfaced by the Analog Devices' model 2B30 transducer conditioner. The bridge excitation and system power is provided by the model 2B35 triple output power supply. The high level voltage output of the 2B30 is converted to the isolated 4 to 20mA current for transmission to a remote recorder or indicator.

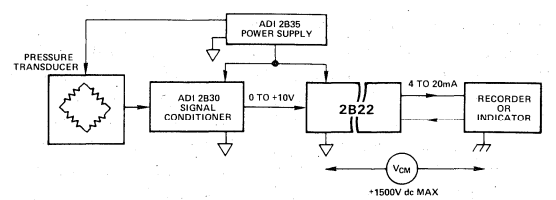


Figure 9. Isolated Pressure Transmitter

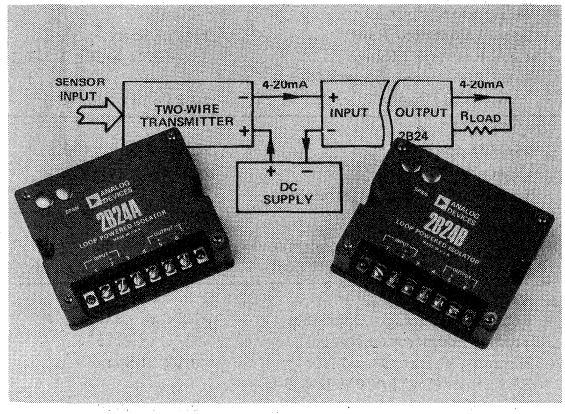
ANALOG DEVICES

Loop Powered Isolator

MODEL 2B24

FEATURES
Self-Powered
Wide Input Range: 1-50mA (2B24B)
High CMV Isolation: ±1500V pk; CMR: 120dB
High Accuracy: ±0.1%
RFI/EMI Immunity
Low Cost

APPLICATIONS
Ground Loop Elimination
Transient Voltage Protection



9

GENERAL DESCRIPTION

The model 2B24 is a low cost, loop-powered isolator designed to accept input current in the range of 1-50mA and provide an isolated output current proportional to the input. The 2B24 is powered by the input signal and does not require an external power supply.

Two basic models are available for signal ranges of 4-20mA (2B24A) and 4-20mA or 10-50mA (2B24B). Both feature high accuracy (±0.1%), high input to output isolation (±1500V pk, continuous), and high CMR (120dB). Other features include low input signal loop burden, low sensitivity to variations in load, as well as excellent stability (±0.01%/°C) over a wide ambient temperature range (-30°C to +85°C).

A rugged metal enclosure, suitable for field mounting, offers environmental protection and screw terminal input and output connections. This enclosure may be either surface or relay track mounted.

APPLICATIONS

The 2B24 is designed to eliminate ground loop problems and high common mode noise interference in process control, monitoring and factory automation systems. It is especially useful for providing individual isolation of many current loop outputs operating from a common source of dc power.

OPERATION

The 2B24 is factory calibrated to accuracy of ±0.1% of span. A user accessible span trim potentiometer providing ±3% adjustment range permits precise field calibration. This may be accomplished by connecting normal operating load resistance and adjusting SPAN for a 20.00mA output when an input is 20.00mA.

A wide range of load resistance (up to 600Ω @ 20mA and 240Ω @ 50mA) may be accommodated by the 2B24. The transmitter supplying power to the 2B24 must be capable of furnishing the necessary input voltage for the given load and desired maximum output current.

DESIGN FEATURES AND USER BENEFITS

High Isolation: Input to output isolation eliminates ground loops and allows ±1500V potential difference between the input and the output.

Loop Powered: All power required for the 2B24 is derived from the process loop, eliminating the need for an external supply and therefore reducing installation cost.

High Noise Rejection: The 2B24 features internal filtering to eliminate errors caused by EMI/RFI and line noise pickup.

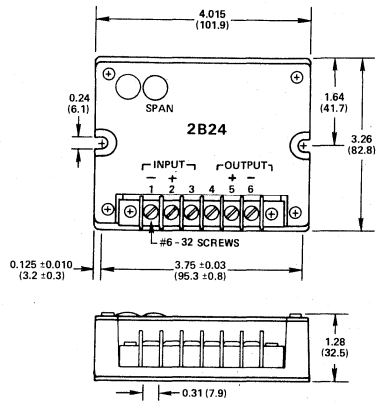
SPECIFICATIONS (typical @ +25°C and I_{IN} = 20mA unless otherwise noted)

Model	2B24A	2B24B
INPUT SPECIFICATIONS		
Input Signal	4-20mA	4-20mA, 10-50mA
Maximum Input Range	1-30mA	1-50mA
Input Voltage Requirement[1]	3.5V+ I_{OUT} RL	*
OUTPUT SPECIFICATIONS		
Output Signal	4-20mA	4-20mA, 10-50mA
Maximum Output Range	1-30mA	1-50mA
Span Adjustment Range	±3% of Span	*
Load Resistance Range	0 to 600Ω @ 20mA	0 to 240Ω @ 50mA
Load Resistance Change Effect per 10Ω Change	±0.15% of Span	*
ACCURACY		
Total Output Error[2]	±0.1% @ R_L = 300Ω	±0.1% @ R_L = 120Ω
Linearity	±0.05% @ R_L = 300Ω	±0.05% @ R_L = 120Ω
Span Stability vs. Temperature	±0.01%/°C	*
ISOLATION		
CMV, Input to Output, Continuous	±1500V pk	*
Common Mode Rejection @ 60Hz	120dB @ R_L = 300Ω	120dB @ R_L = 120Ω
ENVIRONMENTAL		
Temperature Range, Operating	-30°C to +85°C	*
Storage Temperature Range	-55°C to +125°C	*
Humidity Effect, Span Error[3]	±0.2% of Span	*
RFI Effect (5W @ 470MHz @ 3 ft.) Error	±0.5% of Span	*
PHYSICAL		
Case Size	4" X 3.25" X 1.25"	*
Weight	8.5 oz (240g)	*

NOTES
[1] Includes 3.5V plus voltage drop across output load.
[2] Accuracy is specified as a percent of output span and includes combined effects of repeatibility, hysteresis, and linearity.
[3] Per MIL-STD-202, Method 103.
*Specifications same as 2B24A.
Specifications subject to change without notice.

OUTLINE DIMENSIONS (MAX)

Dimensions shown in inches and (mm).



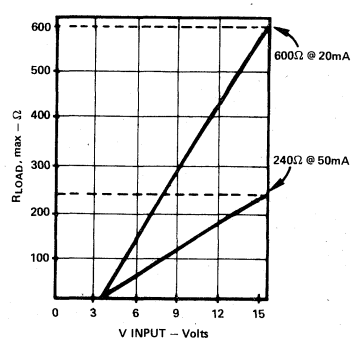


Figure 2. Required V_{INPUT} vs. R_{LOAD} (max) - 2B24A & B

BASIC APPLICATIONS

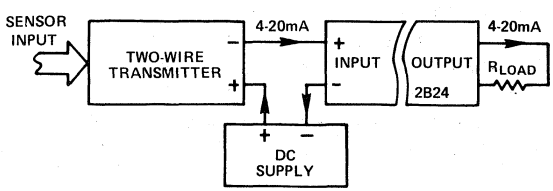


Figure 1a. Two-Wire Transmitter Application

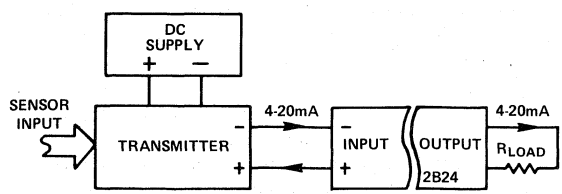


Figure 1b. Four-Wire Transmitter Application

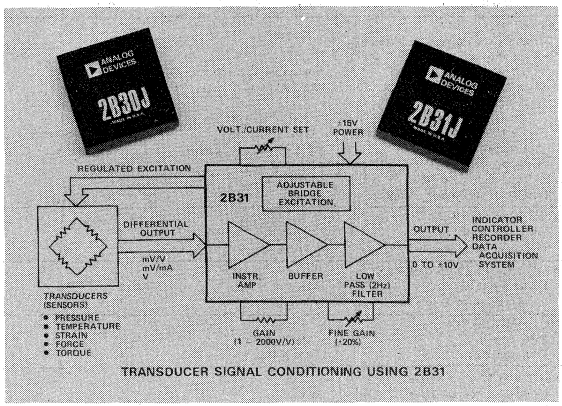
ANALOG DEVICES

High Performance, Economy Strain Gage/RTD Conditioners

MODELS 2B30 AND 2B31

FEATURES
- Complete Signal Conditioning Function
- Low Drift: 0.5μV/°C max ("L"); Low Noise: 1μV p-p max
- Wide Gain Range: 1 to 2000V/V
- Low Nonlinearity: 0.0025% max ("L")
- High CMR: 140dB min (60Hz, G = 1000V/V)
- Input Protected to 130V rms
- Adjustable Low Pass Filter: 60dB/Decade Roll-Off (from 2Hz)
- Programmable Transducer Excitation: Voltage (4V to 15V @ 100mA) or Current (100μA to 10mA)

APPLICATIONS
- Measurement and Control of:
  - Pressure, Temperature, Strain/Stress, Force, Torque
- Instrumentation: Indicators, Recorders, Controllers
- Data Acquisition Systems
- Microcomputer Analog I/O



TRANSDUCER SIGNAL CONDITIONING USING 2B31

9

GENERAL DESCRIPTION

Models 2B30 and 2B31 are high performance, low cost, compact signal conditioning modules designed specifically for high accuracy interface to strain gage-type transducers and RTD's (resistance temperature detectors). The 2B31 consists of three basic sections: a high quality instrumentation amplifier; a three-pole low pass filter, and an adjustable transducer excitation. The 2B30 has the same amplifier and filter as the 2B31, but no excitation capability.

Available with low offset drift of 0.5μV/°C max (RTI, G = 1000V/V) and excellent linearity of 0.0025% max, both models feature guaranteed low noise performance 1μV p-p max, and outstanding 140dB common mode rejection (60Hz, CMV = ±10V, G = 1000V/V) enabling the 2B30/2B31 to maintain total amplifier errors below 0.1% over a 20°C temperature range. The low pass filter offers 60dB/decade roll-off from 2Hz to reduce normal-mode noise bandwidth and improve system signal-to-noise ratio. The 2B31's regulated transducer excitation stage features a low output drift (0.015%/°C max) and a capability of either constant voltage or constant current operation.

Gain, filter cutoff frequency, output offset level and bridge excitation (2B31) are all adjustable, making the 2B30/2B31 the industry's most versatile high-accuracy transducer-interface modules. Both models are offered in three accuracy selections, J/K/L, differing only in maximum nonlinearity and offset drift specifications.

APPLICATIONS

The 2B30/2B31 may be easily and directly interfaced to a wide variety of transducers for precise measurement and control of pressure, temperature, stress, force and torque. For applications in harsh industrial environments, such characteristics as high CMR, input protection, low noise, and excellent temperature stability make 2B30/2B31 ideally suited for use in indicators, recorders, and controllers.

The combination of low cost, small size and high performance of the 2B30/2B31 offers also exceptional quality and value to the data acquisition system designer, allowing him to assign a conditioner to each transducer channel. The advantages of this approach over low level multiplexers include significant improvements in system noise and resolution, and elimination of crosstalk and aliasing errors.

DESIGN FEATURES AND USER BENEFITS

High Noise Rejection: The true differential input circuitry with high CMR (140dB) eliminating common-mode noise pickup errors, input filtering minimizing RFI/EMI effects, output low pass filtering (f_c=2Hz) rejecting 50/60Hz line frequency pickup and series-mode noise.

Input and Output Protection: Input protected for shorts to power lines (130V rms), output protected for shorts to ground and either supply.

Ease of Use: Direct transducer interface with minimum external parts required, convenient offset and span adjustment capability.

Programmable Transducer Excitation: User-programmable adjustable excitation source-constant voltage (4V to 15V @ 100mA) or constant current (100μA to 10mA) to optimize transducer performance.

Adjustable Low Pass Filter: The three-pole active filter (f_c=2Hz) reducing noise bandwidth and aliasing errors with provisions for external adjustment of cutoff frequency.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V unless otherwise noted)

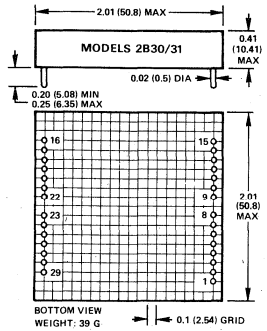
MODEL	2B30J 2B31J	2B30K 2B31K	2B30L 2B31L
GAIN[1]			
Gain Range	1 to 2000V/V	*	*
Gain Equation	G = (1 + 94kΩ/R_G) [20kΩ/(R_F + 16.2kΩ)]	*	*
Gain Equation Accuracy	±2%	*	*
Fine Gain (Span) Adjust. Range	±20%	*	*
Gain Temperature Coefficient	±25ppm/°C max (±10ppm/°C typ)	*	*
Gain Nonlinearity	±0.01% max	±0.005% max	±0.0025% max
OFFSET VOLTAGES[1]			
Total Offset Voltage, Referred to Input			
Initial, @ +25°C	Adjustable to Zero (±0.5mV typ)	*	*
Warm-Up Drift, 10 Min., G = 1000	±5μV RTI	*	*
vs. Temperature			
G = 1V/V	±150μV/°C max	±75μV/°C max	±50μV/°C max
G = 1000V/V	±3μV/°C max	±1μV/°C max	±0.5μV/°C max
At Other Gains	±(3 ± 150/G)μV/°C max	±(1 ± 75/G)μV/°C max	±(0.5 ± 50/G)μV/°C max
vs. Supply, G = 1000V/V	±25μV/V	*	*
vs. Time, G = 1000V/V	±3μV/month	*	*
Output Offset Adjust. Range	±10V	*	*
INPUT BIAS CURRENT			
Initial @ +25°C	+200nA max (100nA typ)	*	*
vs. Temperature (0 to +70°C)	−0.6nA/°C	*	*
INPUT DIFFERENCE CURRENT			
Initial @ +25°C	±5nA	*	*
vs. Temperature (0 to +70°C)	±40pA/°C	*	*
INPUT IMPEDANCE			
Differential	100MΩ‖47pF	*	*
Common Mode	100MΩ‖47pF	*	*
INPUT VOLTAGE RANGE			
Linear Differential Input	±10V	*	*
Maximum Differential or CMV Input Without Damage	130V rms	*	*
Common Mode Voltage	±10V	*	*
CMR, 1kΩ Source Imbalance			
G = 1V/V, dc to 60Hz[1]	90dB	*	*
G = 100V/V to 2000V/V, 60Hz[1]	140dB min	*	*
dc[2]	90dB min (112 typ.)	*	*
INPUT NOISE			
Voltage, G = 1000V/V			
0.01Hz to 2Hz	1μV p-p max	*	*
10Hz to 100Hz[2]	1μV p-p	*	*
Current, G = 1000			
0.01Hz to 2Hz	70pA p-p	*	*
10Hz to 100Hz[2]	30pA rms	*	*
RATED OUTPUT[1]			
Voltage, 2kΩ Load[3]	±10V min	*	*
Current	±5mA min	*	*
Impedance, dc to 2Hz, G = 100V/V	0.1Ω	*	*
Load Capacitance	0.01μF max	*	*
DYNAMIC RESPONSE (Unfiltered)[2]			
Small Signal Bandwidth			
−3dB Gain Accuracy, G = 100V/V	30kHz	*	*
G = 1000V/V	5kHz	*	*
Slew Rate	1V/μs	*	*
Full Power	15kHz	*	*
Settling Time, G = 100, ±10V Output Step to ±0.1%	30μs	*	*
LOW PASS FILTER (Bessel)			
Number of Poles	3	*	*
Gain (Pass Band)	+1	*	*
Cutoff Frequency (−3dB Point)	2Hz	*	*
Roll-Off	60dB/decade	*	*
Offset (at 25°C)	±5mV	*	*
Settling Time, G = 100V/V, ±10V Output Step to ±0.1%	600ms	*	*
BRIDGE EXCITATION (See Table 1)			
POWER SUPPLY[4]			
Voltage, Rated Performance	±15V dc	*	*
Voltage, Operating	±(12 to 18)V dc	*	*
Current, Quiescent	±15mA	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	*
Operating	−25°C to +85°C	*	*
Storage	−55°C to +125°C	*	*
CASE SIZE	2″ x 2″ x 0.4″ (51 x 51 x 10.2mm)	*	*

*Specifications same as 2B30J/2B31J.
[1] Specifications referred to output at pin 7 with 3.75k, 1%, 25ppm/°C fine span resistor installed and internally set 2Hz filter cutoff frequency.
[2] Specifications referred to the unfiltered output at pin 1.
[3] Protected for shorts to ground and/or either supply voltage.
[4] Recommended power supply ADI model 902-2 or model 2B35 transducer power supply (for 2B30).

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

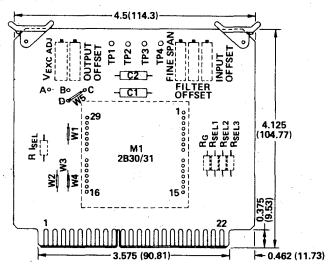


PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	OUTPUT 1 (UNFILTERED)	16	EXC SEL 1
2	FINE GAIN (SPAN) ADJ.	17	I SEL
3	FINE GAIN (SPAN) ADJ.	18	$V_{EXC\ OUT}$
4	FILTER OFFSET TRIM	19	$I_{EXC\ OUT}$
5	FILTER OFFSET TRIM	20	SENSE HIGH (+)
6	BANDWIDTH ADJ. 3	21	EXC SEL 2
7	OUTPUT 2 (FILTERED)	22	REF OUT
8	BANDWIDTH ADJ. 2	23	SENSE LOW (−)
9	BANDWIDTH ADJ. 1	24	REGULATOR +$V_{R\ IN}$
10	R_{GAIN}	25	REF IN
11	R_{GAIN}	26	−V_S
12	−INPUT	27	+V_S
13	INPUT OFFSET TRIM	28	COMMON
14	INPUT OFFSET TRIM	29	OUTPUT OFFSET TRIM
15	+ INPUT		

Note: Pins 16 thru 25 are not connected in Model 2B30

MOUNTING CARDS AC1211, AC1213



AC1211/AC1213 CONNECTOR DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
A	REGULATOR +$V_{R\ IN}$	1	EXC SEL 1
B	SENSE LOW (−)	2	I SEL
C	REF OUT	3	$V_{EXC\ OUT}$
D	REF IN	4	$I_{EXC\ OUT}$
E		5	SENSE HIGH (+)
F		6	EXC SEL 2
H		7	OUTPUT OFFSET TRIM
J		8	
K	−V_S	9	−V_S
L	+V_S	10	+V_S
M		11	
N	COMMON	12	COMMON
P		13	
R	FINE GAIN ADJ.	14	
S	FINE GAIN ADJ.	15	
T	FILTER OFFSET TRIM	16	
U	FILTER OFFSET TRIM	17	R_{GAIN}
V	OUTPUT 2 (FILTERED)	18	R_{GAIN}
W	−INPUT	19	OUTPUT 1 (UNFILTERED)
X	INPUT OFFSET TRIM	20	BANDWIDTH ADJ. 1
Y	INPUT OFFSET TRIM	21	BANDWIDTH ADJ. 3
Z	+ INPUT	22	BANDWIDTH ADJ. 2

The AC1211/AC1213 mounting card is available for the 2B30/2B31. The AC1211/AC1213 is an edge connector card with pin receptacles for plugging in the 2B30/2B31. In addition, it has provisions for installing the gain resistors and the bridge excitation, offset adjustment and filter cutoff programming components. The AC1211/AC1213 is provided with a Cinch 251-22-30-160 (or equivalent) edge connector. The AC1213 includes the adjustment pots; no pots are provided with the AC1211.

FUNCTIONAL DESCRIPTION

Models 2B30 and 2B31 accept inputs from a variety of full bridge strain gage-type transducers or RTD sensors and convert the inputs to conditioned high level analog outputs. The primary transducers providing direct inputs may be 60Ω to 1000Ω strain gage bridges, four-wire RTD's or two- or three-wire RTD's in the bridge configuration.

The 2B30 and 2B31 employ a multi-stage design, shown in Figure 1, to provide excellent performance and maximum versatility. The input stage is a high input impedance (10^8 Ω), low offset and drift, low noise differential instrumentation amplifier. The design is optimized to accurately amplify low level (mV) transducer signals riding on high common mode voltages (±10V), with wide (1-2000V/V), single resistor (R_G), programmable gain to accommodate 0.5mV/V to 36mV/V transducer spans and 5Ω to 2000Ω RTD spans. The input stage contains protection circuitry for accidental shorts to power line voltage (130V rms) and RFI filtering circuitry.

The inverting buffer amplifier stage provides a convenient means of fine gain trim (0.8 to 1.2) by using a 10kΩ potentiometer (R_F); the buffer also allows the output to be offset by up to ±10V by applying a voltage to the noninverting input (pin 29). For dynamic, high bandwidth measurements—the buffer output (pin 1) should be used.

The three-pole active filter uses a unity-gain configuration and provides low-pass Bessel-type characteristics-minimum overshoot response to step inputs and a fast rise time. The cutoff frequency (-3dB) is factory set at 2Hz, but may be increased up to 5kHz by addition of three external resistors (R_{SEL_1} - R_{SEL_3}).

INTERCONNECTION DIAGRAM AND SHIELDING TECHNIQUES

Figure 1 illustrates the 2B31 wiring configuration when used in a typical bridge transducer signal conditioning application. A recommended shielding and grounding technique for preserving the excellent performance characteristics of the 2B30/2B31 is shown.

Because models 2B30/2B31 are direct coupled, a ground return path for amplifier bias currents must be provided either by direct connection (as shown) or by an implicit ground path having up to 1MΩ resistance between signal ground and conditioner common (pin 28). The sensitive input and gain setting terminals should be shielded from noise sources for best performance, especially at high gains. To avoid ground loops, signal return or cable shield should never be grounded at more than one point.

The power supplies should be decoupled with 1μF tantalum and 1000pF ceramic capacitors as close to the amplifier as possible.

TYPICAL APPLICATION AND ERROR BUDGET ANALYSIS

Models 2B30/2B31 have been conservatively specified using min-max values as well as typicals to allow the designer to develop accurate error budgets for predictable performance. The error calculations for a typical transducer application, shown in Figure 1 (350Ω bridge, 1mV/V F.S., 10V excitation), are illustrated below.

Assumptions: 2B31L is used, G = 1000, ΔT = ±10°C, source imbalance is 100Ω, common mode noise is 0.25V (60Hz) on the ground return.

Absolute gain and offset errors can be trimmed to zero. The remaining error sources and their effect on system accuracy (worst case) as a % of Full Scale (10V) are listed:

Error Source	Effect on Absolute Accuracy % of F.S.	Effect on Resolution % of F.S.
Gain Nonlinearity	±0.0025	±0.0025
Gain Drift	±0.025	
Voltage Offset Drift	±0.05	
Offset Current Drift	±0.004	
CMR	±0.00025	±0.00025
Noise (0.01 to 2Hz)	±0.01	±0.01
Total Amplifier Error	±0.09175 max	±0.01275 max
Excitation Drift	±0.15 (±0.03 typ)	
Total Output Error (Worst Case)	±0.24175 max (±0.1 typ)	±0.0127 max

The total worst case effect on absolute accuracy over ±10°C is less than ±0.25% and the 2B31 is capable of 1/2 LSB resolution in a 12 bit, low input level system. Since the 2B31 is conservatively specified, a typical overall accuracy error would be lower than ±0.1% of F.S.

In a computer or microprocessor based system, automatic recalibration can nullify gain and offset drifts leaving noise, nonlinearity and CMR as the only error sources. A transducer excitation drift error is frequently eliminated by a ratiometric operation with the system's A/D converter.

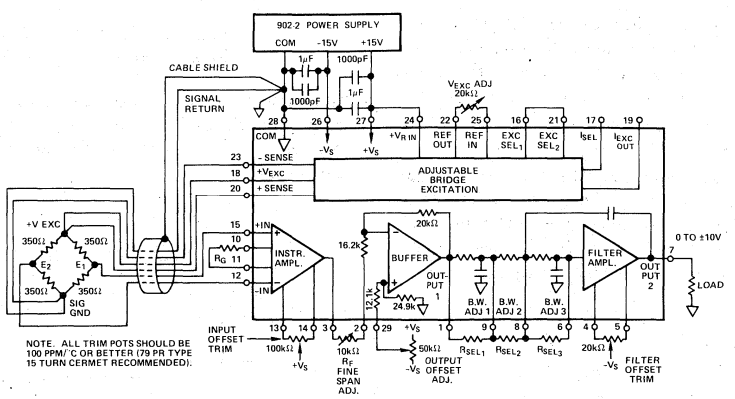


Figure 1. Typical Bridge Transducer Application Using 2B31

BRIDGE EXCITATION (2B31)

The bridge excitation stage of the model 2B31 is an adjustable output, short circuit protected, regulated supply with internally provided reference voltage (+7.15V). The remote sensing inputs are used in the voltage output mode to compensate for the voltage drop variations in long leads to the transducer. The regulator circuitry input (pin 24) may be connected to $+V_S$ or some other positive dc voltage (pin 28 referenced) within specified voltage level and load current range. User-programmable constant voltage or constant current excitation mode may be used. Specifications are listed below in Table 1.

MODEL	2B31J	2B31K	2B31L
Constant Voltage Output Mode			
Regulator Input Voltage Range	+9.5V to +28V	*	*
Output Voltage Range	+4V to +15V	*	*
Regulator Input/Output Voltage Differential	3V to 24V	*	*
Output Current[1]	0 to 100mA max	*	*
Regulation, Output Voltage vs. Supply	0.05%/V	*	*
Load Regulation, I_L = 1mA to I_L = 50mA	0.1%	*	
Output Voltage vs. Temperature (0 to +70°C)	0.015%/°C max 0.003%/°C typ	*	*
Output Noise	1mV rms	*	*
Reference Voltage (Internal)	7.15V ±3%	*	*
Constant Current Output Mode			
Regulator Input Voltage Range	+9.5V to +28V	*	*
Output Current Range	100μA to 10mA	*	*
Compliance Voltage	0 to 10V	*	*
Load Regulation	0.1%	*	*
Temperature Coefficient (0 to +70°C)	0.003%/°C	*	*
Output Noise	1μA rms	*	*

[1] Output Current derated to 33mA max for 24V regulator input/output voltage differential.

Table 1. Bridge Excitation Specifications

OPERATING INSTRUCTIONS

Gain Setting: The differential gain, G, is determined according to the equation:

$$G = (1 + 94k\Omega/R_G)\ [20k\Omega/(R_F + 16.2k\Omega)]$$

where R_G is the input stage resistor shown in Figure 1 and R_F is the variable 10kΩ resistor in the output stage. For best performance, the input stage gain should be made as large as possible, using a low temperature coefficient (10ppm/°C) R_G, and the output stage gain can then be used to make a ±20% linear gain adjustment by varying R_F.

Input Offset Adjustment: To null input offset voltage, an optional 100kΩ potentiometer connected between pins 13 and 14 (Figure 1) can be used. With gain set at the desired value, connect both inputs (pins 12 and 15) to the system common (pin 28), and adjust the 100kΩ potentiometer for zero volts at pin 3. The purpose of this adjustment is to null the internal amplifier offset and it is not intended to compensate for the transducer bridge unbalance.

Output Offset Adjustment: The output of the 2B30/2B31 can be intentionally offset from zero over the ±10V range by applying a voltage to pin 29, e.g., by using an external potentiometer or a fixed resistor. Pin 29 is normally grounded if output offsetting is not desired. The optional filter amplifier offset null capability is also provided as illustrated in Figure 1.

Filter Cutoff Frequency Programming: The low pass filter cutoff frequency may be increased from the internally set 2Hz by the addition of three external resistors connected as shown in Figure 1. The values of resistors required for a desired cutoff frequency, f_c, above 5Hz are obtained by the equation below:

$$R_{SEL_1} = 11.6 \times 10^6/(2.67f_c - 4.34);$$

$$R_{SEL_2} = 27.6 \times 10^6/(4.12f_c - 7)$$

$$R_{SEL_3} = 1.05 \times 10^6/(0.806f_c - 1.3)$$

where R_{SEL} is in ohms and f_c in Hz. Table 2 gives the nearest 1% R_{SEL} for several common filter cutoff (-3dB) frequencies.

f_c (Hz)	R_{SEL1} (kΩ) (Pin 1 to 9)	R_{SEL2} (kΩ) (Pin 9 to 8)	R_{SEL3} (kΩ) (Pin 8 to 6)
2	Open	Open	Open
5	1270.000	2050.00	383.000
10	523.000	806.00	154.000
50	90.000	137.00	26.700
100	44.200	68.10	13.300
500	8.660	13.30	2.610
1000	4.320	6.65	1.300
5000	0.866	1.33	0.261

Table 2. Filter Cutoff Frequency vs. R_{SEL}

Voltage Excitation Programming: Pin connections for a constant voltage output operation are shown in Figure 2. The bridge excitation voltage, V_{EXC}, is adjusted between +4V to +15V by the 20kΩ (50ppm/°C) R_{VSEL} potentiometer. For ratiometric operation, the bridge excitation can be adjusted by applying an external positive reference to pin 25 of the 2B31. The output voltage is given by: $V_{EXC\ OUT} = 3.265V_{REF\ IN}$. The remote sensing leads should be externally connected to the excitation leads at the transducer or jumpered as shown in Figure 2 if sensing is not required.

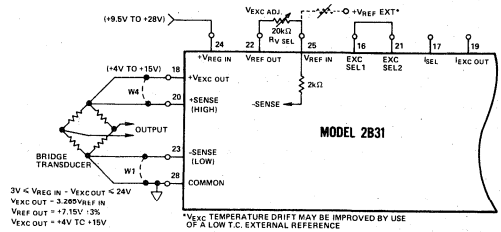


Figure 2. Constant Voltage Excitation Connections

Current Excitation Programming: The constant current excitation output can be adjusted between 100μA to 10mA by two methods with the 2B31. Figure 3 shows circuit configuration for a current output with the maximum voltage developed across the sensor (compliance voltage) constrained to +5V. The value of programming resistor R_{ISEL} may be calculated from the relationship: $R_{ISEL} = (V_{REG\ IN} - V_{REF\ IN})/I_{EXC\ OUT}$.

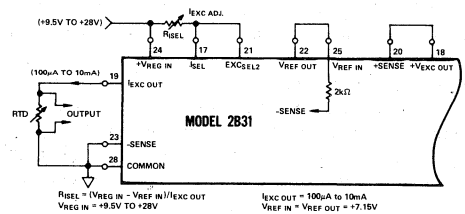


Figure 3. Constant Current Excitation Connections (V_{COMPL} = 0 to +5V)

A compliance voltage range of 0 to +10V can be obtained by connecting the 2B31 as shown in Figure 4. The 2kΩ potentiometer R_{ISEL} is adjusted for desired constant current excitation output.

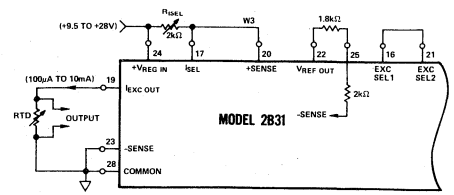


Figure 4. Constant Current Excitation Connections (V_{COMPL} = 0 to +10V)

APPLICATIONS

Strain Measurement: The 2B30 is shown in Figure 5 in a strain measurement system. A single active gage (120Ω, GF = 2) is used in a bridge configuration to detect small changes in gage resistance caused by strain. The temperature compensation is provided by an equivalent dummy gage and two high precision 120Ω resistors complete the bridge. The 2B35 adjustable power supply is set to a low +3V excitation voltage to avoid the self-heating error effects of the gage and bridge elements. System calibration produces a 1V output for an input of 1000 microstrains. The filter cutoff frequency is set at 100Hz.

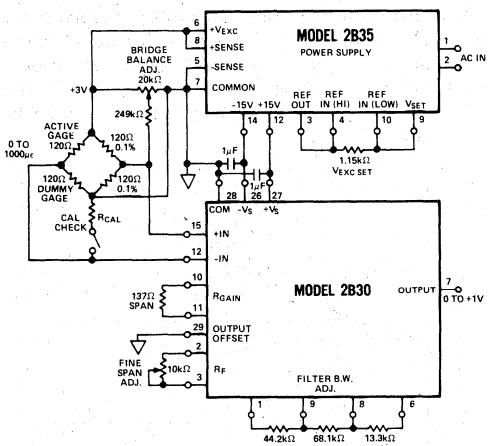


Figure 5. Interfacing Half-Bridge Strain Gage Circuit

Pressure Transducer Interface: A strain gage type pressure transducer (BLH Electronics, DHF Series) is interfaced by the 2B31 in Figure 6. The 2B31 supplies regulated excitation (+10V) to the transducer and operates at a gain of 333.3 to achieve 0-10V output for 0-10,000 p.s.i. at the pressure transducer. Bridge Balance potentiometer is used to cancel out any offset which may be present and the Fine Span potentiometer adjustment accurately sets the full scale output. Depressing the calibration check pushbutton switch shunts a system calibration resistor (R_{CAL}) across the transducer bridge to give an instant check on system calibration.

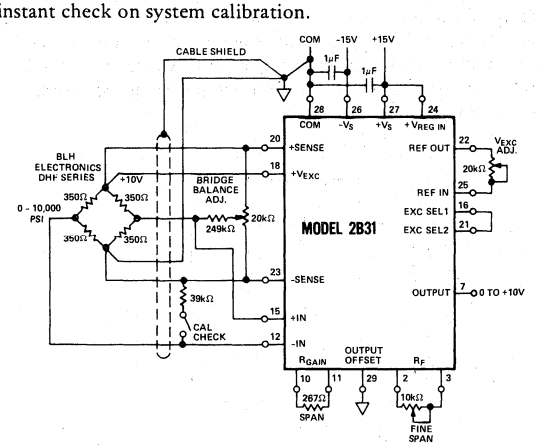


Figure 6. Pressure Transducer Interface Application

Platinum RTD Temperature Measurement: In Figure 7 model 2B31 provides complete convenient signal conditioning in a wide range (-100°C to +600°C) RTD temperature measurement system. YSI - Sostman four-wire, 100Ω platinum RTD (PT139AX) is used. The four wire sensor configuration, combined with a constant current excitation and a high input impedance offered by the 2B31, eliminates measurement errors resulting from voltage drops in the lead wires. Offsetting may be provided via the 2B31's offset terminal. The gain is set by the gain resistor for a +10V output at +600°C.

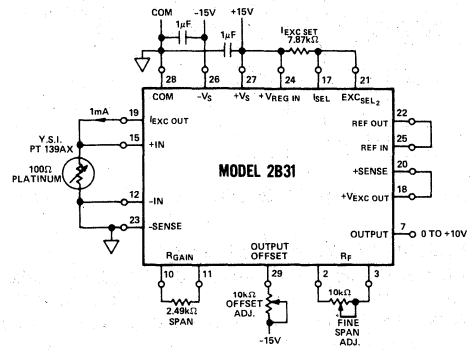


Figure 7. Platinum RTD Temperature Measurement

Interfacing Three-Wire Sensors: A bridge configuration is particularly useful to provide offset in interfacing to a platinum RTD and to detect small, fractional sensor resistance changes. Lead compensation is employed, as shown in Figure 8, to maintain high measurement accuracy when the lead lengths are so long that thermal gradients along the RTD leg may cause changes in line resistance. The two completion resistors (R1, R2) in the bridge should have a good ratio tracking (±5ppm/°C) to eliminate bridge error due to drift. The single resistor (R3) in series with the platinum sensor must, however, be of very high absolute stability. The adjustable excitation in the 2B31 controls the power dissipated by the RTD itself to avoid self-heating errors.

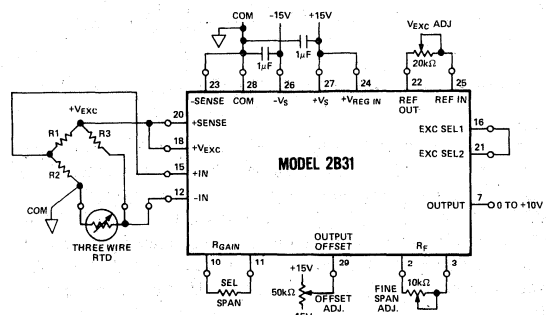


Figure 8. Three-Wire RTD Interface

Linearizing Transducer Output: To maximize overall system linearity and accuracy, some strain gage-type and RTD transducer analog outputs may require linearization. A simple circuit may be used with the 2B31 to correct for the curvature in the input signal. Consult factory for the application assistance.

Data Acquisition System: Figure 9 shows a typical application of the 2B30/2B31 in a low level, high speed microcomputer based data acquisition system. The advantages of this configuration are improvement in CMR enhanced by a low pass filter/channel provided by the 2B31, elimination of aliasing errors and crosstalk noise between input channels, improvement in system noise and resolution, and optimized, individual bridge excitation source for each channel.

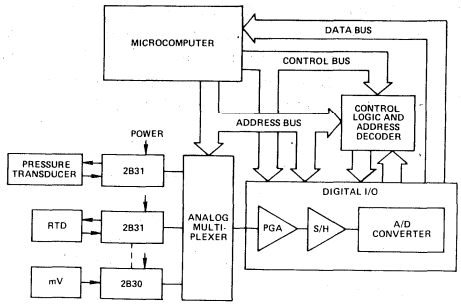


Figure 9. Use of the 2B30/2B31 in Data Acquisition System

PERFORMANCE CHARACTERISTICS

Input Offset Voltage Drift: Models 2B30/2B31 are available in three drift selections: ±0.5, ±1 and ±3μV/°C (max, RTI, G = 1000V/V). Total input drift is composed of two sources (input and output stage drifts) and is gain dependent. Figure 10 is a graph of the worst case total voltage offset drift vs. gain for all versions.

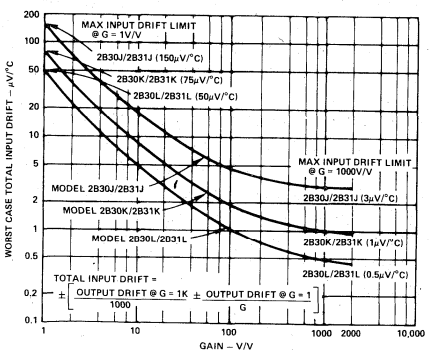


Figure 10. Total Input Offset Drift (Worst Case) vs. Gain

Gain Nonlinearity and Noise: Nonlinearity is specified as a percent of full scale (10V), e.g. 0.25mV RTO for 0.0025%. Three maximum nonlinearity selections offered are: ±0.0025%, ±0.005% and ±0.01% (G = 1 to 2000V/V). Models 2B30/2B31 offer also an excellent voltage noise performance by guaranteeing maximum RTI noise of 1μV p-p (G = 1000V/V, $R_S \leq 5k\Omega$) with noise bandwidth reduced to 2Hz by the low pass filter.

Low Pass Filter: The three pole Bessel-type active filter attenuates unwanted high-frequency components of the input signal above its cutoff frequency (-3dB) with 60dB/decade roll-off. With a 2Hz filter, attenuation of 70dB at 60Hz is obtained, settling time is 600ms to 0.1% of final value with less than 1% overshoot response to step inputs. Figure 11 shows the filter response.

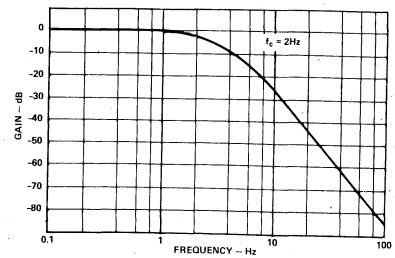


Figure 11. Filter Amplitude Response vs. Frequency

Common Mode Rejection: CMR is rated at ±10V CMV and 1kΩ source imbalance. The CMR improves with increasing gain. As a function of frequency, the CMR performance is enhanced by the incorporation of low pass filtering, adding to the 90dB minimum rejection ratio of the instrumentation amplifier. The effective CMR at 60Hz at the output of the filter (f_c = 2Hz) is 140dB min. Figure 12 illustrates a typical CMR vs. Frequency and Gain.

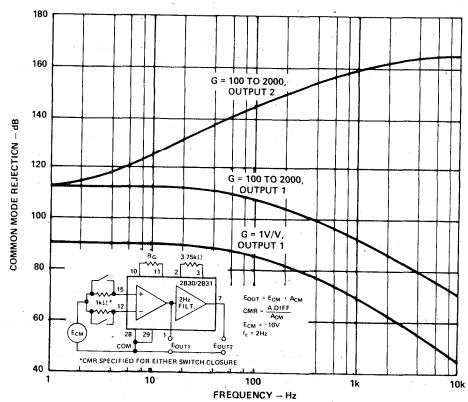


Figure 12. Common Mode Rejection vs. Frequency and Gain

Bridge Excitation (2B31): The adjustable bridge excitation is specified to operate over a wide regulator input voltage range (+9.5V to +28V). However, the maximum load current is a function of the regulator circuit input-output differential voltage, as shown in Figure 13. Voltage output is short circuit protected and its temperature coefficient is ±0.015% V_{OUT}/°C max (±0.003%/°C typ). Output temperature stability is directly dependent on a temperature coefficient of a reference and for higher stability requirements, a precision external reference may be used.

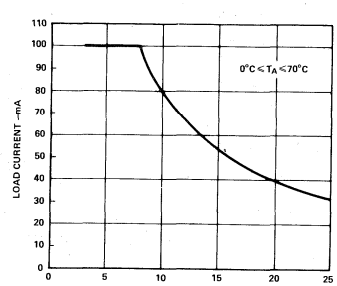


Figure 13. Maximum Load Current vs. Regulator Input-Output Voltage Differential

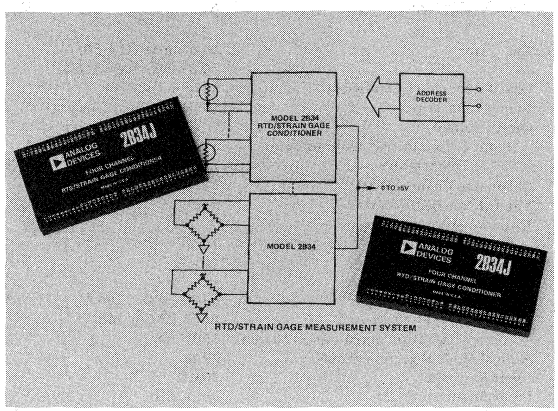
ANALOG DEVICES

Four Channel RTD/Strain Gage Conditioner

MODEL 2B34

FEATURES
- Low Input Offset Drift: ±1.0μV/°C
- Low Gain Drift: ±25ppm/°C
- Low Nonlinearity: ±0.01% max (±0.005% typ)
- Differential Input Protection: ±130V rms
- Channel Multiplexing: 3000 chan/sec Scanning Speed
- Solid State Reliability
- Internal RTD Excitation/Lead Wire Compensation

APPLICATIONS
- Multichannel Signal Conditioning
- Data Acquisition
- Industrial Process Monitoring



9

GENERAL DESCRIPTION

The model 2B34 is a four channel signal conditioner providing input protection, multiplexing, and amplification in a single, low cost package. A multi-purpose device, the 2B34 is designed to effectively condition low level signals (±30mV to ±100mV) such as those produced by RTD and strain gage sensors. The superior design of the 2B34 provides low input drift (±1.0μV/°C), high common mode rejection (94dB @ 60Hz), and extremely stable gain (±25ppm/°C). Other features include low nonlinearity (±0.01% max), excitation and lead wire compensation for RTD inputs, and a wide operating temperature range (-25°C to +85°C).

APPLICATIONS

The 2B34 is a superior alternative to the relay multiplexing technique used in multichannel data acquisition systems, computer interface systems, and measurement and control instrumentation. Advantages over relay circuits include functional versatility, superior signal conditioning, and solid state speed and reliability.

DESIGN FEATURES AND USER BENEFITS

Solid State Design: Complete solid state construction offers both high performance and reliability.

Ease of Use: The multichannel, functionally complete design in a compact (2″ X 4″ X 0.4″) module, conserves board space and eliminates the need for a number of discrete components that would otherwise be required.

Low Cost: The 2B34 offers the lowest cost per channel for solid state, low level sensor signal conditioning.

Wide Operating Temperature Range: The 2B34 has been designed to operate over -25°C to +85°C ambient temperature range.

FUNCTIONAL DESCRIPTION

The internal structure of the 2B34 is shown in Figure 1. Four individual input channels are multiplexed into a single, low

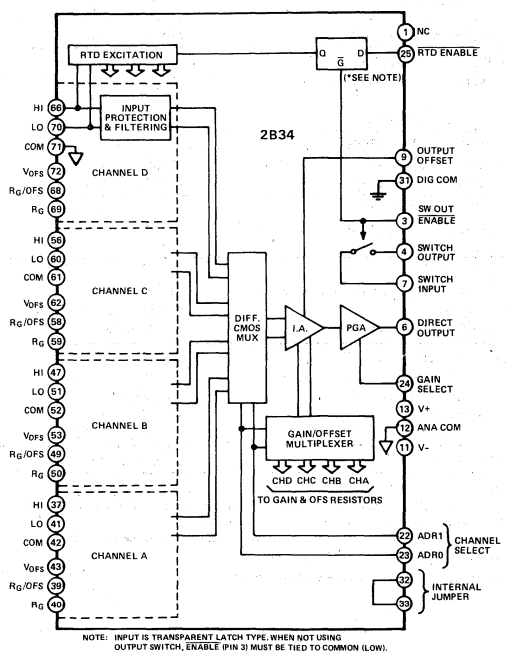


Figure 1. 2B34 Functional Diagram

SPECIFICATIONS (typical @ +25°C, V_S = ±15V, unless otherwise noted)

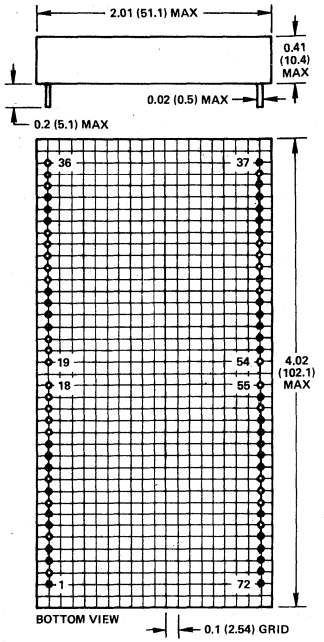
Model	2B34J Strain Gage Mode	2B34J RTD Mode
ANALOG INPUT		
Number of Channels	4	*
Input Range	±30mV & ±100mV	25–175Ω & 0–350Ω
Gain Range (R_G =945Ω)	166.6V/V & 50V/V	*
Expanded[1]	50V/V to 1000V/V	*
Transfer Function	N/A	V_{OUT} = [0.4 X 10^{-3} X (R_{RTD}) –0.04] G
Gain Error	±0.6% max (G = 50)	*
	±0.8% max (G = 166.6)	*
Gain Temperature Coefficient[2]	±25ppm/°C	*
Gain Nonlinearity	±0.01% of Span, max	*
Offset Voltage		
Input Offset, Initial[3] (Adj. to Zero)	±150μV	*
vs. Temperature	±1μV/°C	±0.015 deg/deg
Channel to Channel Offset	±25μV	*
Total Offset Drift (RTI)	±1μV/°C	*
Input Noise Voltage		
0.01Hz–100Hz, R_S = 1kΩ	1.5μV p-p	*
Common Mode Voltage	±6V	N/A
Common Mode Rejection		
R_S = 100Ω, f = 60Hz	94dB (@ G = 166.6)	N/A
R_S = 1kΩ, f = 60Hz	86dB (@ G = 166.6)	
Maximum Safe Differential Input (10 min)	130V rms	*
Normal Mode Rejection @ 60Hz	24dB	*
Input Resistance	20MΩ	*
Input Bias Current	10nA max	*
Lead Resistance Effect	N/A	±0.03 deg/Ω
ANALOG OUTPUT		
Output Voltage Swing	±5V @ 1mA	*
Output Resistance		
Direct Output	0.1Ω	*
Switched Output	35Ω, +0.5%/°C	*
Maximum Switched Voltage	±9V, no load	*
SENSOR EXCITATION		
Excitation Level (per channel)	NA	0.4mA ±1% (±1.7% max)
vs. Temperature	NA	±10ppm/°C
CHANNEL SELECTION		
Channel Selection Time to ±0.01% F.S.	300μs	*
Channel Scanning Speed	>3000 chan/sec	*
DYNAMIC RESPONSE		
Input Settling Time to ±0.01% F.S.	0.4 sec	*
Bandwidth	4Hz	*
POWER SUPPLY		
Voltage, ±V_S, Rated Performance	±15V dc ±5%	*
Current	+35mA, –15mA, max	*
Supply Effect on Offset	±0.003%/%	±0.02%/%
ENVIRONMENTAL		
Temperature		
Rated Performance	0 to +70°C	*
Operating	–25°C to +85°C	*
Storage	–55°C to +85°C	*
CASE SIZE	2" X 4" X 0.4"	

NOTES
[1] Gain range may be expanded by use of external amplifier as shown in Figure 3.
[2] Does not include effects of sensor excitation drift.
[3] With no induced offset, using circuit shown in Figure 2 (pots centered).
*Specifications same as Strain Gage Mode.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTE: TERMINAL PINS INSTALLED ONLY IN SHADED HOLE LOCATIONS

2B34 PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	NC	37	HI
2		38	
3	SW'D OUTPUT ENABLE	39	R_G/OFS
4	SW'D OUTPUT	40	R_G
5		41	LO
6	DIRECT OUTPUT	42	COM
7	SW'D INPUT	43	V_{OFS} (+10V)
8		44	
9	OUTPUT OFFSET	45	
10		46	
11	–15V	47	HI
12	ANA COM	48	
13	+15V	49	R_G/OFS
14		50	R_G
15		51	LO
16		52	COM
17		53	V_{OFS} (+10V)
18		54	
19		55	
20		56	HI
21		57	
22	ADR1 } CHANNEL	58	R_G/OFS
23	ADR0 } SELECT	59	R_G
24	GAIN SELECT	60	LO
25	RTD ENABLE	61	COM
26		62	V_{OFS} (+10V)
27		63	
28		64	
29		65	
30		66	HI
31	DIG COM	67	
32	SYNC IN } *	68	R_G/OFS
33	SYNC OUT } *	69	R_G
34		70	LO
35		71	COM
36		72	V_{OFS} (+10V)

CHANNEL A: pins 37–43
CHANNEL B: pins 49–53
CHANNEL C: pins 56–62
CHANNEL D: pins 66–72

*SHORTED INTERNALLY FOR FEEDTHROUGH FOR USE WITH 2B54/55 MODELS.

drift differential instrumentation amplifier, with the desired channel specified by the two digital channel select inputs. This signal is then fed to a digitally controlled programmable gain amplifier (PGA). The appropriate gain for a particular sensor type is selected by the gain select input.

User selectable direct or switched output permits direct output connection of several modules, should more than four channels be required.

An internally selectable constant current excitation source provides direct connection of 2 or 3 wire RTDs, thus eliminating the need for external excitation sources. Each channel contains an input protection and filtering network to preserve signal integrity in the presence of series mode 50/60Hz noise.

OPERATING INSTRUCTIONS

Connection of the 2B34 with three wire RTD inputs is shown in Figure 2 and will be all that is needed in most cases. The following sections describe the basic application, as well as detail some optional connections that enhance the module's performance in more complex applications. All unused inputs should be shorted to common.

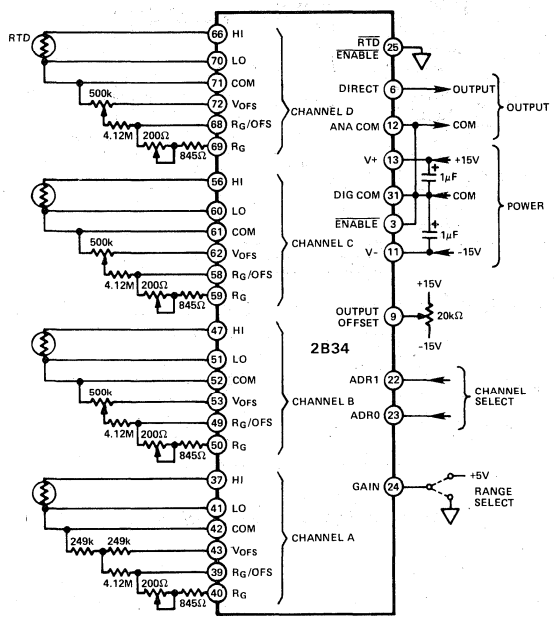


Figure 2. Basic RTD Application

Channel Selection: Each channnel of the 2B34 is turned on and off by applying the proper binary code to channel select inputs (ADR0, ADR1). Channels may be selected in any order and there are no restrictions on rate other than the 300μs settling time for access to a channel (Table 1, channel select truth table).

Gain Selection: The 2B34 is designed to provide signal conditioning of both RTD and strain gage sensor inputs. To accommodate both of these sensor types, the 2B34 is precalibrated to provide gains of 50 and 166.6, with gain components shown in Figure 2. This provides proper amplification of input signals over the span of ±30mV to ±100mV. Selection of the desired gain and sensor input mode is achieved by applying the appropriate binary codes shown in Table 2. A 200Ω pot provides ±3% full scale span adjustment.

AD1	AD0	Channel
0	0	A
0	1	B
1	0	C
1	1	D

Table 1. Channel Selection

(Pin 24) Gain Select Input	Selected Gain
0	166.6
1	50

(Pin 25) RTD ENABLE	Selected Mode
0	RTD
1	Strain Gage

Table 2. Gain and Mode Selection

Zero Suppression & Gain: In most instances, the gain capability of the 2B34 will be sufficient. However, in the case of input signals that may require gains greater than 166, the

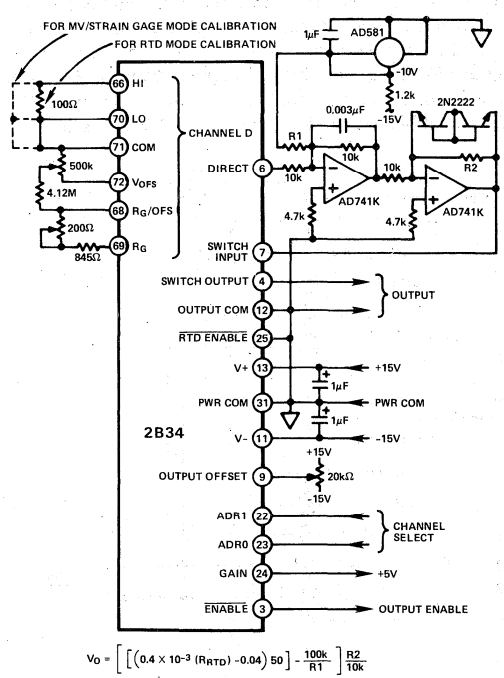


Figure 3. Zero Suppressed Switched Output RTD Application

gain range of the 2B34 may be supplemented by use of an external amplifier (Figure 3). A low drift, operational amplifier (such as the AD741K) should be used to maintain signal integrity.

Optional Offset Adjustment: All channels of the 2B34 are typically within ±150μV (RTI) offset. For use in more demanding applications, the module has provisions for fine adjustment of the input offset (RTI) of each input as well as the output offset (RTO) of the entire module. None of the offset adjustments will affect drift performance.

In some applications, where ±25μV channel-to-channel offset voltage can be tolerated, adjustment of only the output offset will be sufficient. The offset circuit shown in Figure 2 (for channel "A") is required when a potentiometer is not used to adjust input offset. The output offset adjustment may then be used to null the 150μV (RTI) offset, leaving an offset difference between channels of ±25μV. If input offset adjustment is desired, the input offset circuitry shown in Figure 3 should be used. This provides approximately ±140mV (RTO) of adjustment, and should be adequate, in most cases, for elimination of sensor offset errors.

To calibrate in the mV (strain gage) mode, (Figure 3), short the signal inputs (for example, pins 66, 70 for channel "D") to common and center the input offset adjustment potentiometer. Adjust the output offset potentiometer until the output is nulled for that channel at the appropriate gain. The input offset pots on each channel may then be used to eliminate any errors on subsequent channels that are selected.

To calibrate in the RTD mode, follow the same procedure, but replace the short with a 100Ω resistance standard.

Channel Expansion: The 2B34 has provisions for directly interconnecting several modules when more than four channels are required. The series switched outputs of the modules are connected together, the channel select inputs are driven in parallel, and the switched output of the desired module is selected using the $\overline{\text{ENABLE}}$ pin. This technique is shown in Figure 4. Channel address and $\overline{\text{ENABLE}}$ (active low) inputs are CMOS/TTL compatible with an input current of 100μA each.

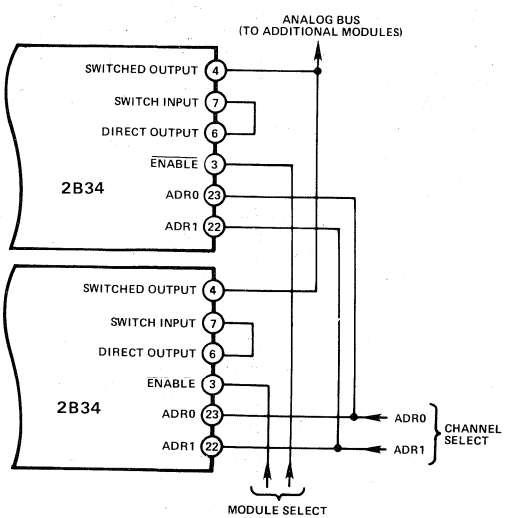


Figure 4. Channel Expansion

2B34 Strain Gage Application: Figure 5 shows a four channel strain gage input system utilizing the multiplexing feature of the 2B34. Input offset and gain adjustments are used to eliminate inherent sensor errors. The model 2B35 triple output supply may be used to provide power for the 2B34 as well as excitation for the strain gage sensors.

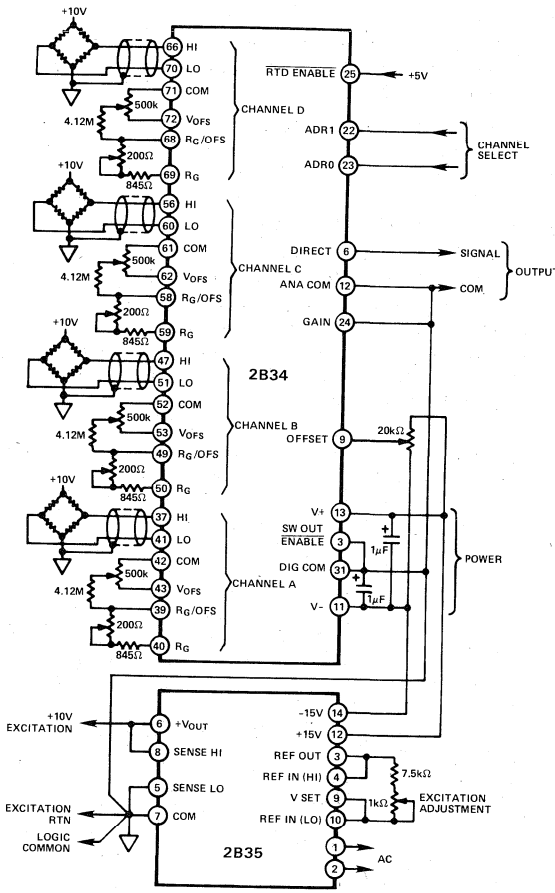


Figure 5. 2B34 Strain Gage Application

Precision, Triple Output Transducer Power Supply

MODEL 2B35

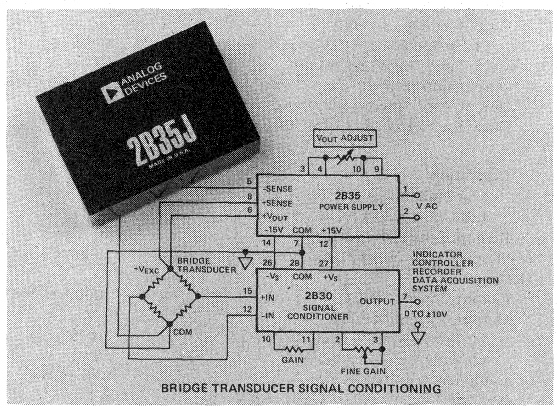
FEATURES

Resistor Programmable Voltage or Current Output
- **Voltage: +1V dc to +15V dc @ 125mA max**
- **Current: 100μA to 10mA (V_{COMPL} = +10V)**

Dual Fixed Output: ±15V dc @ ±65mA max
Excellent Regulation: Line ±0.01% max; Load ±0.02% max
Low Drift: 0.006%/°C max (2B35K)
No Derating Over -25°C to +71°C Operating Range

APPLICATIONS

Measurement and Control Instruments and Systems
Excitation Source For:
- **Strain Gages, Pressure Transducers, Load Cells, Torque Transducers, RTD's**



BRIDGE TRANSDUCER SIGNAL CONDITIONING

9

GENERAL DESCRIPTION

The 2B35 is a triple output modular power supply designed to provide regulated excitation to a wide variety of transducers as well as ±15V power for amplifiers and other analog circuits of an instrumentation system. The single-resistor programmable transducer excitation output may be operated in two modes: constant voltage, providing a +1V to +15V output or a constant current, adjustable from 100μA to 10mA.

The programmable output in the voltage mode features current rating of 0 to 125mA, suitable to excite four 350Ω transducers at 10V. Current limiting protects the output against accidental overload and remote sensing corrects for the transducer cable resistance variations. In the constant current mode, externally set 100μA to 10mA output offers a 0 to +10V compliance voltage range. The ±15V outputs feature 0.5% tracking accuracy and current rating of 0 to ±65mA max.

Two accuracy selections are available offering guaranteed low temperature coefficient; 2B35K: 0.006%/°C max and 2B35J: 0.05%/°C max. Line and load regulation are also guaranteed; 2B35K: 0.01% and 0.02%, and 2B35J: 0.08% and 0.1%, max, respectively.

APPLICATIONS

The 2B35 is designed for ac powered signal conditioning instrumentation applications used for data acquisition, control, indication or recording. This compact module may be applied as a power source for the model 2B30 strain gage transducer/RTD signal conditioner in a high accuracy transducer interface application. Some typical applications involve strain gages for stress/strain measurements, pressure transducers, load cells, torque transducers and RTD's.

OPERATION

Figure 1 illustrates operation of the 2B35K providing an adjustable voltage output and dual 15V dc outputs. The resistor programmable output (+V_{OUT}) is set between +1V to +15V by the R_{TRIM}. R_{TRIM} may be determined by using either the table shown in Figure 1 or the graph shown in Figure 2. For example, to provide an adjustable range from +1V to +6V, R_{TRIM} should be a 5kΩ pot.

The remote sensing inputs (pins 5 and 8) are connected at the transducer (load) to the voltage output (SENSE HIGH to +V_{OUT} and SENSE LOW to COMMON).

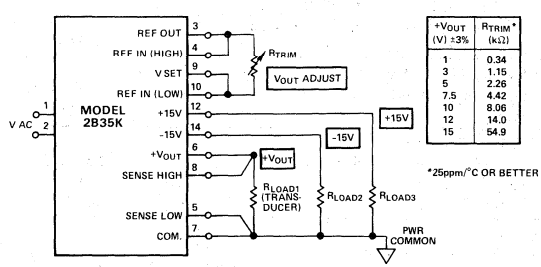


Figure 1. Model 2B35K Connection Diagram for Dual 15V dc and Adjustable +1V to +15V Output

For optional input voltage ranges, see note 1, next page.

SPECIFICATIONS (typical @ +25°C and 115V ac 60Hz unless otherwise noted)

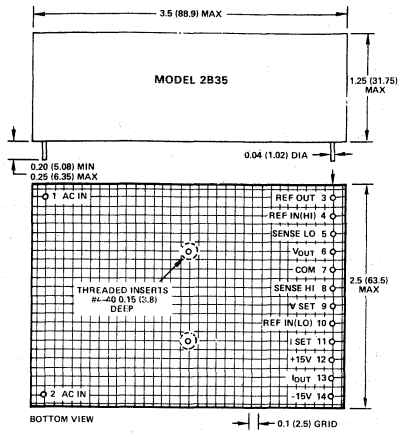
Model	2B35J	2B35K
INPUT		
Input Voltage Range[1]	105V ac to 125V ac	*
Input Frequency Range	50Hz to 400Hz	*
ADJUSTABLE OUTPUT		
Voltage Mode		
Output Voltage Range	+1V to +15V dc	*
Output Voltage Stability		
vs. Temperature – % V_{OUT}/°C max	±0.05	±0.006
vs. Time – % V_{OUT}/month	±0.01	*
Output Current (-25°C to +71°C)[2]	0 to 125mA max	*
Output Impedance – @ dc, max	0.1Ω	*
Noise and Ripple (dc to 1MHz) – mV p-p max	1	*
– mV rms max	0.25	*
Regulation		
Line (full range) – % V_{OUT} max	±0.08	±0.01
Load (no load to full load) – % V_{OUT} max	±0.1	±0.02
Remote Sensing Impedance	30kΩ	*
Short Circuit Current Limit[3] (-25°C to +71°C)	200mA	*
Current Mode		
Output Current Range	100µA to 10mA	*
Output Current Stability		
vs. Temperature – % I_{OUT}/°C max	±0.05	±0.006
vs. Time – % I_{OUT}/month	±0.01	*
Compliance Voltage Range	0 to +10V	*
Noise and Ripple (dc to 1MHz) –µA p-p	0.1	*
Line Regulation (full range) – % I_{OUT} max	±0.08	±0.01
DUAL FIXED OUTPUTS		
Output Voltage	±15V dc	*
Voltage Error – mV max	-0, +300	*
Accuracy Tracking (-15V Ref to +15V) – % max	±0.5	*
Stability vs. Temperature – %/°C max	±0.02	±0.006
Output Current[4]	0 to ±65mA max	*
Output Impedance – @ dc, max	0.1Ω	*
Noise and Ripple (dc to 1MHz) – mV p-p	1	*
– mV rms	0.25	*
Regulation		
Line (full range) – % max	±0.08	±0.01
Load (no load to full load) – % max	±0.1	±0.02
Short Circuit Current Limit[3] (-25°C to +71°C)	±180mA	*
INPUT TO OUTPUT ISOLATION		
Breakdown Voltage – Continuous, ac or dc	±500V pk max	*
Isolation Resistance	50MΩ	*
TEMPERATURE RANGE		
Operating, Rated Performance	-25°C to +71°C	*
Storage	-25°C to +85°C	*
MECHANICAL		
Case Dimensions – Inches	2.5 x 3.5 x 1.25	*
Weight – Grams	550	*
Mating Socket	AC1212	*

NOTES
*Specifications same as model 2B35J.
[1] Optional input voltage ranges: "E" Option; 205-240V ac, 50 to 400Hz
"F" Option; 90-110V ac, 50 to 400Hz
"H" Option; 220-260V ac, 50 to 400Hz
Order option desired as a suffix to model number.
[2] Maximum output current available over the entire output voltage and temperature range without derating.
[3] Output protected for continuous short circuit over the temperature range.
[4] Unbalanced load operation is permissible for any combination of $+I_O$ and $|-I_O|$ which does not exceed a total of 130mA.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



MATING SOCKET: AC1212

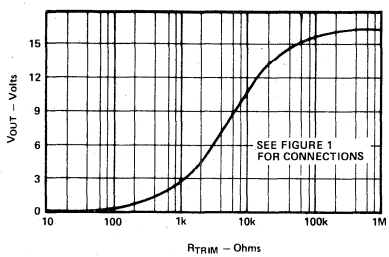


Figure 2. Voltage Output vs. R_{TRIM}

ADJUSTABLE CURRENT OUTPUT WITH DUAL 15V dc OUTPUTS

Pin connections to provide dual 15V dc and a constant current output are shown in Figure 3. The current output is adjusted from 100µA to 10mA via R_{TRIM}. The value of programming resistor R_{TRIM} may be calculated from the relationship: $R_{TRIM} = 2.46/I_{OUT}$ where R_{TRIM} is in kΩ and I_{OUT} in mA.

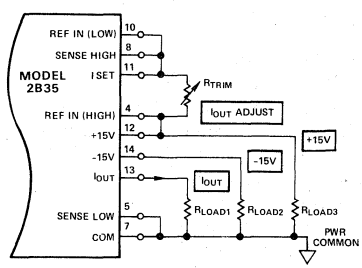


Figure 3. Model 2B35 Connection Diagram to Provide Dual 15V dc and Adjustable 100µA to 10mA Current Output

Isolated, Thermocouple Signal Conditioner

MODEL 2B50

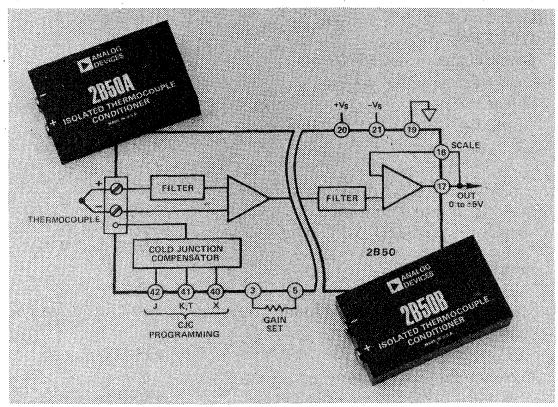
FEATURES

- Accepts J, K, T, E, R, S or B Thermocouple Types
- Internally Provided Cold Junction Compensation
- High CMV Isolation: ±1500V pk
- High CMR: 160dB min @ 60Hz
- Low Drift: ±1μV/°C max (2B50B)
- High Linearity: ±0.01% max (2B50B)
- Input Protection and Filtering
- Screw Terminal Input Connections

APPLICATIONS

Precision Thermocouple Signal Conditioning For:

- Process Control and Monitoring
- Industrial Automation
- Energy Management
- Data Acquisition Systems



9

GENERAL DESCRIPTION

The model 2B50 is a high performance thermocouple signal conditioner providing input protection, isolation and common mode rejection, amplification, filtering and integral cold junction compensation in a single, compact package.

The 2B50 has been designed to condition low level analog signals, such as those produced by thermocouples, in the presence of high common mode voltages. Featuring direct thermocouple connection via screw terminals and internally provided reference junction temperature sensor, the 2B50 may be jumper programmed to provide cold junction compensation for thermocouple types J, K, T, and B, or resistor programmed for types E, R, and S.

The high performance of the 2B50 is accomplished by the use of reliable transformer isolation techniques. This assures complete input to output galvanic isolation (±1500V pk) and excellent common mode rejection (160dB @ 60Hz).

Other key features include: input protection (220V rms), filtering (NMR of 70dB @ 60Hz), low drift amplification (±1μV/°C max - 2B50B), and high linearity (±0.01% max - 2B50B).

APPLICATIONS

The 2B50 has been designed to provide thermocouple signal conditioning in data acquisition systems, computer interface systems, and temperature measurement and control instrumentation.

In thermocouple temperature measurement applications, outstanding features such as low drift, high noise rejection, and 1500V isolation make the 2B50 an ideal choice for systems used in harsh industrial environments.

DESIGN FEATURES AND USER BENEFITS

High Reliability: To assure high reliability and provide isolation protection to electronic instrumentation, the 2B50 has been conservatively designed to meet the IEEE Standard for transient voltage protection (472-1974: SWC) and provide 220V rms differential input protection.

High Noise Rejection: The 2B50 features internal filtering circuitry for elimination of errors caused by RFI/EMI, series mode noise, and 50Hz/60Hz pickup.

Ease of Use: Internal compensation enables the 2B50 to be used with seven different thermocouple types. Unique circuitry offers a choice of internal or remote reference junction temperature sensing. Thermocouple connections may be made either by screw terminals or, in applications requiring PC Board connections, by terminal pins.

Small Package: 1.5″ X 2.5″ X 0.6″ size conserves board space.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V unless otherwise noted)

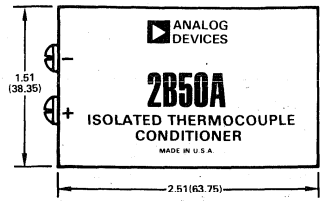
MODEL	2B50A	2B50B
INPUT SPECIFICATIONS		
Thermocouple Types		
Jumper Configurable Compensation	J, K, T, or B	*
Resistor Configurable Compensation	R, S, or E	*
Input Span Range	±5mV to ±100mV	*
Gain Range	50V/V to 1000V/V	*
Gain Equation	$1 + (200k\Omega/R_G)$	*
Gain Error	±0.25%	*
Gain Temperature Coefficient	±35ppm/°C max	±25ppm/°C max
Gain Nonlinearity[1]	±0.025% max	±0.01% max
Offset Voltage		
Input Offset (Adjustable to Zero)	±50µV	*
vs. Temperature	±2.5µV/°C max	±1µV/°C max
vs. Time	±1.5µV/month	*
Output Offset (Adjustable to Zero)	±10mV	*
vs. Temperature	±30µV/°C	*
Total Offset Drift	$\pm\left(2.5 + \frac{30}{G}\right)$ µV/°C	$\pm\left(1 + \frac{30}{G}\right)$ µV/°C
Input Noise Voltage		
0.01Hz to 100Hz, R_S = 1kΩ	1µV p-p	*
Maximum Safe Differential Input Voltage	220V rms, Continuous	*
CMV, Input to Output		
Continuous, ac or dc	±1500V pk max	*
Common Mode Rejection		
@ 60Hz, 1kΩ Source Unbalance	160dB min	*
Normal Mode Rejection @ 60Hz	70dB min	*
Bandwidth	dc to 2.5Hz (-3dB)	*
Input Impedance	100MΩ	*
Input Bias Current[2]	±5nA	*
Open Input Detection	Downscale	*
Response Time[3], G = 250	1.4sec	*
Cold Junction Compensation		
Initial Accuracy[4]	±0.5°C	*
vs. Temperature[5] (+5°C to +45°C)	±0.01°C/°C	*
OUTPUT SPECIFICATIONS		
Output Voltage Range[6]	±5V @ ±2mA	*
Output Resistance	0.1Ω	*
Output Protection	Continuous Short to Ground	*
POWER SUPPLY		
Voltage		
Output ±V_S (Rated Performance)	±15V dc ±10% @ ±0.5mA	*
(Operating)	±12V to ±18V dc max	*
Oscillator +V_{OSC} (Rated Performance)	+13V to +18V dc @ 15mA	*
ENVIRONMENTAL		
Temperature Range, Rated Performance	0 to +70°C	*
Operating	-25°C to +85°C	*
Storage Temperature Range	-55°C to +85°C	*
RFI Effect (5W @ 470MHz @ 3ft)		
Error	±0.5% of Span	*
PHYSICAL		
Case Size	1.5" X 2.5" X 0.6"	*

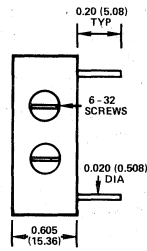
*Specifications same as 2B50A.
[1] Gain nonlinearity is specified as a percentage of output signal span representing peak deviation from the best straight line; e.g., nonlinearity at an output span of 10V pk-pk (±5V) is ±0.01% or ±1mV.
[2] Does not include open circuit detection current of 20nA (optional by jumper connection).
[3] Open input response time is dependent upon gain.
[4] When used with internally provided CJC sensor.
[5] Compensation error contributed by ambient temperature changes at the module.
[6] Output swing of ±10V may be obtained through output scaling (Figure 5).

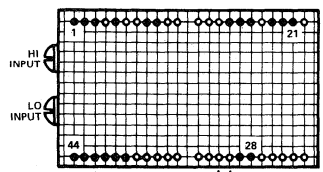
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).







NOTE: TERMINAL PINS INSTALLED ONLY IN SHADED HOLE LOCATIONS

PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	INPUT LO	23	
2	INPUT HI	24	
3	R_G	25	
4		26	
5	R_G/COM	27	
6		28	+V OSC
7		29	OSC COM
8	+V ISO OUT	30	
9	-V ISO OUT	31	
10		32	
11		33	
12		34	
13		35	
14		36	
15	OUTPUT OFFSET ADJUST	37	
		38	
16	OUTPUT SCALE	39	OPEN INPUT DET.
17	OUTPUT	40	X
18		41	K, T } T TYPE PROGRAMMING
19	OUTPUT COM	42	J
20	+V_S	43	CJC SENSOR IN
21	-V_S	44	CJC SENSOR OUT
22			

MATING SOCKET: AC1218

FUNCTIONAL DESCRIPTION

The internal structure of the 2B50 is shown in Figure 1. An input filtering and protection network precedes a low drift, high performance amplifier whose gain is set by a user supplied resistor (R_G) for gains of 50 to 1000V/V. Isolated power is brought out to permit convenient adjustment of the input offset voltage, if desired.

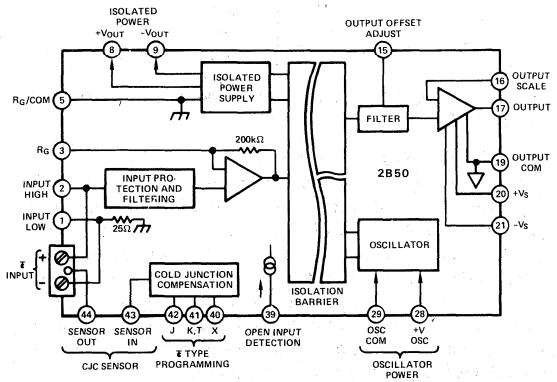


Figure 1. 2B50 Functional Block Diagram

Internal circuitry provides reference junction compensation. An integral reference junction sensor is provided for direct thermocouple connections, or an external reference sensor (2N2222 transistor) may be used in applications having remote thermocouple termination. Compensating networks for thermocouple types J, K, and T are built into the 2B50. A fourth compensation (X) may be programmed with a single resistor for any other thermocouple type. The 2B50 can be programmed for uncompensated output when used with inputs other than thermocouples.

Transformer coupling is used to achieve stable, reliable input to output galvanic isolation, as well as elimination of ground loop error effects.

Normally, the full scale output of the 2B50 is ±5V. However, with the addition of an external resistive divider, the output buffer amplifier may be scaled for a gain of up to 2, providing a full scale output swing of ±10V.

OPERATING INSTRUCTIONS

The connections shown in Figure 2 are common to most applications using the 2B50, and, in many cases, will be all that is required.

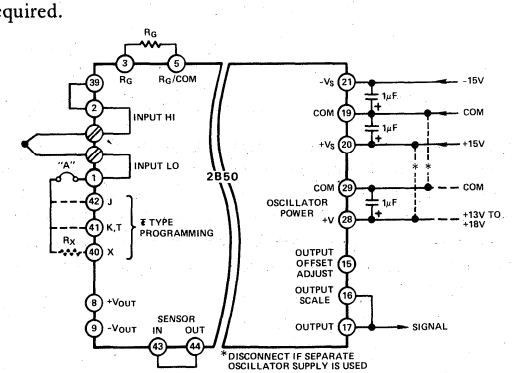


Figure 2. Basic 2B50 Application

Two sets of parallel thermocouple input connections are provided. The thermocouple input may be connected by screw terminals (Input +, Input −) or to terminal pins 1 (−) and 2 (+) in cases where thermocouples are to be remotely terminated. The following sections describe a basic thermocouple application, as well as detail some optional connections to enhance performance in more demanding applications. Jumper A (Figure 2) is used to disconnect cold junction compensation circuitry during offset adjustments.

INTERCONNECTION GUIDELINES

All power supply inputs should be decoupled with 1μF capacitors as close to the unit as possible. Any jumpers installed for programming purposes should also be installed as close as possible to minimize noise pickup effects.

Since the oscillator section of the 2B50 accounts for most of the power consumption but can accept a wide range of voltages (+13V to +18V), it may be desirable to power this section from a convenient source of unregulated power.

If the same supply is to be used for both amplifier and oscillator circuitry, the power supply returns should be brought out separately so that oscillator power supply currents do not flow in the low lead of the signal output. In either case, a 1μF capacitor must be connected from $+V_{OSC}$ (Pin 28) to Oscillator COM (Pin 29).

The oscillator and amplifier sections are completely isolated; therefore, a dc power return path is not required between the two power supply commons.

GAIN SETTING

The gain of the 2B50 is set by a user-supplied resistor (R_G) connected as shown in Figure 2. Gain will normally be selected so that the maximum output of the signal source will result in a plus full scale output swing. The resistor value required is determined by the equation: $R_G = 200k\Omega/(G-1)$.

A series trim on the gain setting resistor can be used to trim out the resistor tolerance and module gain error (Figure 3). Since addition of a series resistance will always decrease gain, the value of the gain-setting resistor should be selected to provide a gain somewhat higher than the desired trimmed gain. A good quality (e.g., 10ppm/°C), metal-film resistor should be used for R_G, since drift of R_G will add to the overall gain drift of the 2B50. A cermet pot is suitable for the trim.

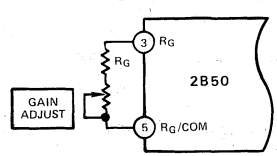


Figure 3. Gain Adjustment

INPUT AND OUTPUT OFFSET ADJUSTMENTS

The 2B50 has provisions for adjusting input and output offset errors of the module. None of the offset adjustments will affect drift performance, and adjustments need not be used unless the particular application calls for lower offsets than those specified.

Connections for offset adjustments are shown in Figure 4. Isolated supply voltages are brought out for input trimming convenience only and are not for use as a power supply for external components.

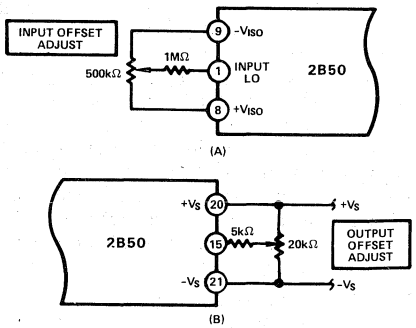


Figure 4. (A) Input and (B) Output Offset Adjustment

OFFSET CALIBRATION

1. Short Input + and Input – together.
2. Disconnect cold junction compensation circuitry by removing Jumper "A" (Figure 2).
3. Adjust input offset trim pot (±250μV range, RTI) to zero output while operating at the desired gain. In most applications, adjustment of the input offset alone will be sufficient. Output offset adjustment (±30mV range) may be performed if it is desired to adjust output offset on the nonisolated side.

OPEN INPUT DETECTION

Connecting the open input detection pin (PIN 39) to input high (PIN 2) creates a 20nA bias current which will provide a negative overscale response if the input is opened, or in case of thermocouple "burn out". The speed at which this occurs is dependent on gain, with a typical response time of 1.4sec @ G = 250.

OUTPUT SCALING

With the output scale (PIN 16) connected to the output (PIN 17), the full scale output range is ±5V and the total gain is equal to the gain set by R_G. For applications requiring a full scale output of ±10V, a resistive divider may be connected to provide a gain of 2 at the output amplifier (see Figure 5). In this configuration, total gain will be twice the gain set by R_G. Output gains greater than 2 cannot be used.

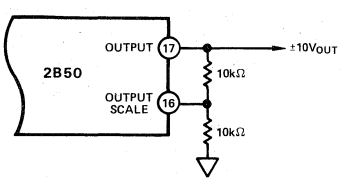


Figure 5. Output Scaling Connections

COLD JUNCTION COMPENSATION

The 2B50 may be programmed to provide cold junction compensation for types J, K and T thermocouples by connecting a jumper from input low (PIN 1) to the appropriate programming points (PIN 42 for J, PIN 41 for K or T). To compensate other thermocouple types, a resistor (R_X) is connected from the "X" programming point (PIN 40) to Input Low (PIN 1). Table 1 shows the appropriate R_X values for types E, R, and S. R_X should be a 50ppm/°C, 1% tolerance resistor.

Type B thermocouples are unique, in that they have almost no output in the +5°C to +45°C range, and, therefore, do not require cold junction compensation at all. To accommodate a type B thermocouple, resistor R_X must be left open. Error due to cold junction temperature will be less than ±1°C for any measurement above 260°C. In the measurement range above 1000°C (where type B thermocouples are normally used) the error will be less than ±0.3°C.

T/C Type	R_X (kΩ)
E	1.87
R,S	19.6
B	Open

Table 1. Compensation Values for Thermocouple Types E, R, S and B

REMOTE REFERENCE SENSING

In applications requiring termination of thermocouple leads at a point located remotely from the 2B50, with connections brought to the 2B50 (PINS 1,2) by copper wires, reference temperature sensing at the remote location will be necessary. The 2B50 has provisions for connection of a 2N2222 transistor (metal can version) for use as a reference junction sensor. The connections are shown in Figure 6. The remote sensing transistor is calibrated by adjusting R_{CAL} to obtain the value of V_{CAL} as specified in Table 2.

(Example: V_{CAL} = 570.0mV @ 25°C)

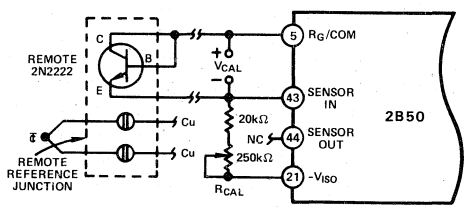


Figure 6. Remote Reference Junction Sensing

Sensor Temp (°C)	V_{CAL} (mV)
5	616.5
10	604.9
15	593.3
20	581.6
25	570.0
30	558.4
35	546.8
40	535.1
45	523.5

(Values may be interpolated)

Table 2. Calibration Voltage vs. Sensor Temperature

Proper sensor placement is important. Close thermal contact of the sensor and thermocouple termination point (reference junction) is essential for accurate operation of the 2B50. The sensor may be placed any distance from the 2B50. When the sensor leads are more than ten feet long, or in the presence of strong noise signal sources, shielded cable should be used.

Two-Wire, Thermocouple Temperature Transmitters

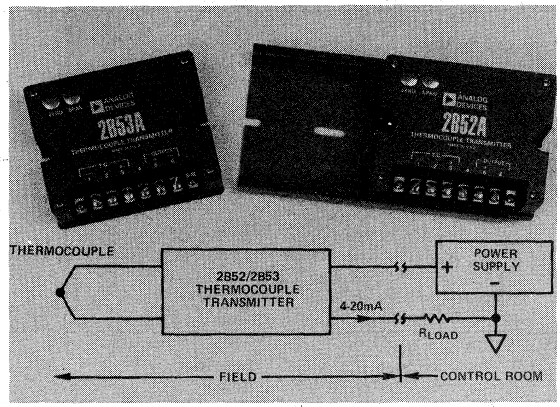
MODELS 2B52 and 2B53

FEATURES

Accept Type J, K or T Thermocouple Inputs
Compatible with Standard 4–20mA Loops
High Accuracy: ±0.1%
High CMV Isolation: 600V rms; CMR = 160dB (2B52)
High Noise Rejection and RFI Immunity
Internal Cold Junction Compensation
Open Thermocouple Detection
Millivolt Signal Transmission
Low Cost

APPLICATIONS

Thermocouple Temperature Monitoring and Control In:
Process Control
Factory Automation
Energy Management



9

GENERAL DESCRIPTION

Models 2B52 and 2B53 are high performance, low cost temperature transmitters designed to accept a thermocouple input from types J, K or T and produce a standard 4–20mA output current proportional to the measured temperature.

Two basic models are available. The 2B52 features high input to output isolation (600V rms) and high CMR (160dB @ 60Hz). The 2B53 offers a functionally equivalent design without input to output isolation. Both models were designed to operate as two-wire transmitters and are compatible with standard 4–20mA loops.

The 2B52 and 2B53 offer high noise rejection, RFI immunity and automatic cold junction compensation to assure accurate operation in noisy industrial environments over a wide ambient temperature range. Other features include open thermocouple detection, fast response time and a low bias current to minimize errors induced by thermocouple extension wires.

A rugged metal enclosure, suitable for field mounting, offers environmental protection and screw terminal input and output connections. This enclosure may be either surface or standard relay track mounted.

APPLICATIONS

The 2B52 and 2B53 have been specifically designed to provide low cost, reliable and accurate thermocouple temperature measurement and transmission in a wide array of industries, including chemical, petrochemical, power generation and food processing.

These models are especially useful in process control and monitoring applications where the process sensor is located remotely from the receiver. The 2B52 and 2B53 may then be used to provide signal conditioning near the point of temperature measurement and to transmit an accurate, noise immune, high level current signal over conventional copper wires, resulting in improved performance and reduced cost.

DESIGN FEATURES AND USER BENEFITS

Low Cost: Low transmitter cost, two-wire operation and the use of inexpensive copper wire for transmission result in lower total installation cost.

High Isolation (2B52): Input to output isolation eliminates ground loop errors in installations requiring grounded sensors and permits direct transmission of signal to a receiver where common mode voltages up to 600V rms may exist.

High Noise Rejection: The 2B52 and 2B53 feature internal filtering circuitry to eliminate errors caused by RFI/EMI and line frequency pickup.

Environmental Protection: High quality electronic components, protective coating and mechanical packaging combine to provide a high degree of reliability and protection against temperature, humidity and noise interference.

Millivolt Transmission: Unique circuitry of the 2B52 and 2B53 allows both models to be used as mV signal transmitters.

Ease of Calibration: Both models can be quickly, easily and accurately calibrated in the field to operate over any input span between 5 and 100 millivolts.

For detailed information, contact factory.

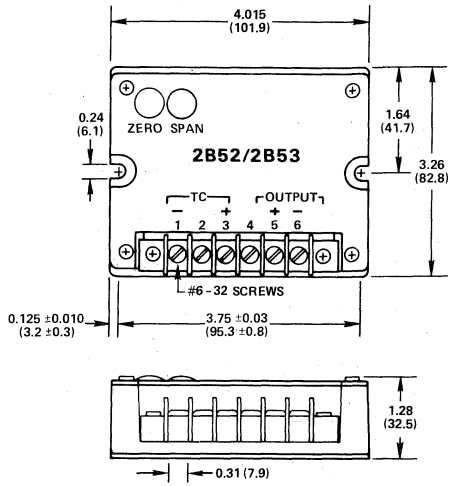
SPECIFICATIONS (typical @ +25°C and V_S = +24V dc unless otherwise noted)

Model	2B52A	2B53A
INPUT SPECIFICATIONS		
Thermocouple Types	J, K, T	*
Input Span Range	5mV min, 100mV max	*
Input Impedance	5MΩ	*
Input Bias Current[1]	85nA	30nA
Zero and Span Adj. Range	±5% of Span	*
Open Input Detection	Upscale	*
OUTPUT SPECIFICATIONS		
Output Span	4–20mA	*
Minimum Output Current	3.3mA, typ	2mA, typ
Maximum Output Current	42mA, typ	28mA, typ
Load Resistance Range Equation	R_L max = (+V_S -12V)/20mA	*
@ +24V Supply	0 to 600Ω max	*
Output Protection[2]	+60V	*
ACCURACY		
Total Output Error[3]	±0.1%	*
Stability vs. Ambient Temperature		
Zero, for Ambient 0 to +50°C[4]	±0.015°C/°C	*
0 to +85°C[4]	±0.025°C/°C	*
-30°C to 0°C[4]	±0.06°C/°C	*
Span, for Ambient -30°C to +85°C	±0.005%/°C	*
Warm-up Time to Rated Performance	5 min	3 min
ISOLATION		
CMV, Input to Output, Continuous	600V rms	NA
Common Mode Rejection, @ 60Hz	160dB	NA
RESPONSE TIME		
to 90% of Span	0.3 sec	0.1 sec
POWER SUPPLY		
Voltage, Operating Range	+12V to +60V dc	*
Supply Change Effect, % of Span		
on Zero	0.005%/V	*
on Span	0.001%/V	*
ENVIRONMENTAL		
Temperature Range, Rated Performance	-30°C to +85°C	*
Storage Temperature Range	-55°C to +125°C	*
Relative Humidity, Noncondensing[5]	0 to 90%	*
RFI Effect (5W @ 470MHz @ 3 ft.) Error, % of Span	±0.5%	*
PHYSICAL		
Case Size	4" X 3.25" X 1.25"	*
Weight	8.5 oz. (240g)	8 oz. (227g)

NOTES
[1] Includes thermocouple burnout detection current.
[2] Protected for reverse polarity and for any combination of input and output pins.
[3] Accuracy is specified as a percent of output span (16mA). Accuracy spec includes combined effects of transmitter repeatability, hysteresis and linearity. Does not include sensor error.
[4] Includes combined effects of cold junction compensation and amplifier offset drift.
[5] Per MIL-STD-202E method 103.
*Specifications same as 2B52A.
Specifications subject to change without notice.

OUTLINE DIMENSIONS (MAX)

Dimensions shown in inches and (mm).



ORDERING INFORMATION

Example: MODEL 2B52A - 1 - J - 03

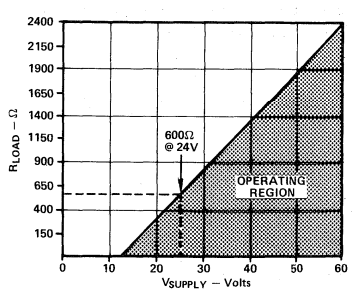
Select Model
2B52A (Isolated)
2B53A (Nonisolated)

Select Housing
1 – Standard Enclosure

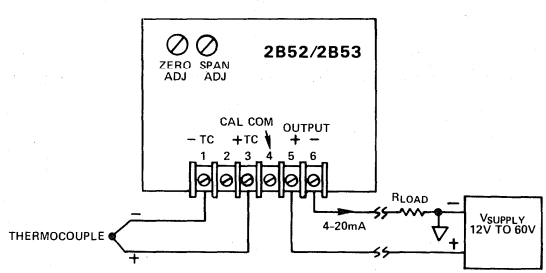
Select Thermocouple Type
J, K or T

Select Temperature Range
01 through 06

Range in °C(°F)	TC Type	No.
-100 to +300 (-148 to +572)	J, K, T	01
0 to +200 (+32 to +392)	T	02
0 to +500 (+32 to +932)	J	03
0 to +600 (+32 to +1112)	K	04
0 to +750 (+32 to +1382)	J	05
0 to +1000 (+32 to +1832)	K	06



R_{LOAD} vs V_{SUPPLY}



Model 2B52/2B53 Basic Application

Four-Channel, Isolated Thermocouple/mV Conditioners

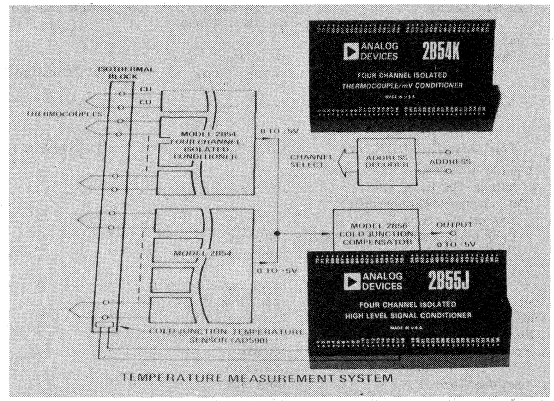
MODELS 2B54 AND 2B55

FEATURES

Low Cost
Wide Input Span Range: ±5mV to ±100mV (2B54)
±50mV to ±5V (2B55)
12-Bit Systems Compatible
High CMV Isolation: ±1000V dc; CMR = 156dB min @ 60Hz
Low Input Offset Voltage Drift: ±1μV/°C max (2B54B)
Low Gain Drift: ±25ppm/°C max (2B54B)
Low Nonlinearity: ±0.02% max (±0.012% typ)
Normal Mode Input Protection (130V rms) and Filtering
Channel Multiplexing: 400 chan/sec Scanning Speed
Solid State Reliability

APPLICATIONS

Multichannel Thermocouple Temperature Measurements
Low and High Level Data Acquisition Systems
Industrial Measurement and Control Systems



TEMPERATURE MEASUREMENT SYSTEM

GENERAL DESCRIPTION

Models 2B54 and 2B55 are low cost, high performance, four-channel signal conditioners. Both models are functionally complete, providing input protection, isolation and common mode rejection, multiplexing, filtering and amplification.

The 2B54 has been designed to condition low level signals (±5mV to ±100mV), like those generated by thermocouples or strain gages, in the presence of high common mode voltages. The 2B55 is optimized to condition ±50mV to ±5V or 4 to 20mA transmitter signals as inputs. The four-channel structure of both models results in significant cost and size reduction.

The high performance of the 2B54 and 2B55 is accomplished by the use of reliable transformer isolation techniques and an amplifier-per-channel architecture. Each of the input channels is galvanically isolated (±1000V dc) from the other input channels and from output ground. The amplifier-per-channel structure is used to obtain low input drift (±1μV/°C max, 2B54B), high common mode rejection (156dB @ 60Hz), and very stable gain (±25ppm/°C max). Other key features include low input noise (1μV p-p), low nonlinearity (±0.02% max) and open-thermocouple detection (2B54).

APPLICATIONS

Models 2B54 and 2B55 were designed to serve as a superior alternative to the relay multiplexing circuits used in multichannel data acquisition systems, computer interface systems, process signal isolators, and temperature measurement and control instrumentation. Advantages over relay circuits include functional versatility, superior performance, and solid state reliability.

In thermocouple temperature measurement applications, outstanding low drift, high noise rejection, high throughput and 1000V isolation make the 2B54 a natural choice over flying capacitor multiplexers in conditioning any thermocouple type. When cold junction compensation is required in measurement of temperature with thermocouples, the 2B54 may be used directly with the model 2B56 Universal Cold Junction Compensator.

DESIGN FEATURES AND USER BENEFITS

High Reliability: To assure high reliability and provide isolation protection to electronic instrumentation, reliable transformer isolation and solid state switching are used. Both models have been conservatively designed to meet the IEEE standard for Transient Voltage Protection (472-1974:SWC) and offer 130V rms normal mode input protection.

High Noise Rejection: To preserve high system accuracy in electrically noisy industrial environments, the 2B54 and 2B55 provide excellent common mode noise rejection, RFI/EMI immunity, and low pass filtering for rejection of series mode noise and 50Hz/60Hz pickup.

Ease of Use: The multichannel, functionally complete design in a compact (2″ X 4″ X 0.4″) module, assures ease of use, conserves board space and eliminates the need for a number of discrete components necessary in relay multiplexing circuits.

Low Cost: The 2B54 and 2B55 offer the lowest cost per channel for isolated, solid state, low level signal conditioners.

SPECIFICATIONS (typical @ +25°C, V_S = ±15V and V_{OSC} = +15V, unless otherwise noted)

Model	2B54A	2B54B	2B55A
ANALOG INPUTS			
Number of Channels	4	*	*
Input Span Range	±5mV to ±100mV	*	±50mV to ±5V
Gain Equation	$G = 1 + 10k\Omega/R_G$	*	*
Gain Error	±0.2% max (G = 50 to 300)	*	±0.2% max (G = 1 to 100)
	±1% max (G = 1000)	*	NA
Gain Temperature Coefficient	±35ppm/°C max	±25ppm/°C max	±25ppm/°C max
Gain Nonlinearity[1]	±0.03% max (G = 50 to 300)	±0.02% max(±0.012% typ)	±0.02% max (G = 1 to 100)
	±0.03% (G = 1000)	*	NA
Offset Voltage			
Input Offset, Initial (Adj. to Zero)	±20µV max	*	±50µV max
vs. Temperature	±2.5µV/°C max	±1µV/°C max(±0.5µV/°C typ)	±5µV/°C max
vs. Time	±1.5µV/month	*	*
Output Offset (Adjustable to Zero)	±12mV max	*	*
vs. Temperature	±50µV/°C max	*	*
Total Offset Drift (RTI), max	$\pm\left(2.5+\frac{50}{G}\right)\mu V/°C$	$\pm\left(1+\frac{50}{G}\right)\mu V/°C$	$\pm\left(5\mu V+\frac{50}{G}\right)\mu V/°C$
Input Noise Voltage			
0.01Hz –100Hz, R_S = 1kΩ	1µV p-p	*	*
CMV, Channel-to-Channel or Channel-to-Ground			
Continuous, ac, 60Hz	750V rms	*	*
Continuous, ac or dc	±1000V pk max	*	*
Common Mode Rejection			
$R_S \leq 100\Omega$, $f \geq 50Hz$	156dB min (G = 1000)	*	145dB min (G = 100)
$R_S \leq 100\Omega$, $f \geq 50Hz$	128dB min (G = 50)	*	110dB min (G = 1)
Normal Mode Input, Without Damage	130V rms, 60Hz	*	*
Normal Mode Rejection, @ 60Hz	55dB min (G = 1000)	*	55dB min (G = 100)
Input Resistance, Power On	100MΩ	*	*
Power Off	35kΩ min	*	74kΩ min
Input Bias Current	+8nA max	*	*
Open Input Detection Time[2]	6 sec (G = 1000)	*	NA
	120 sec (G = 50)	*	NA
Open Input Response	Negative Overscale	*	NA
ANALOG OUTPUT			
Output Voltage Swing[3]	±5V @ ±5mA	*	*
Output Noise, dc – 100kHz	0.8mV p-p	*	*
Output Resistance			
Direct Output	0.1Ω	*	*
Switched Output	35Ω	*	*
CHANNEL SELECTION			
Channel Selection Time to ±0.01% FS	2.5ms max	*	*
Channel Scanning Speed	400 chan/sec min	*	*
Channel Select Input Reverse Voltage Rating	3V max	*	*
POWER SUPPLY			
Voltage			
Output ±V_S (Rated Performance)	±15V dc ±10%	*	*
(Operating)	±12V to ±18V dc max	*	*
Oscillator +V_{OSC} (Rated Performance)	+13.5V to +24V	*	*
Absolute max +V_{OSC}	+26V	*	*
Current			
Output ±V_S = ±15V	±4mA max	*	*
Oscillator +V_{OSC} = +15V	40mA max	*	*
Supply Effect on Offset			
Output ±V_S	100µV/V RTO	*	*
Oscillator +V_{OSC}	1µV/V RTI	*	*
ENVIRONMENTAL			
Temperature			
Rated Performance	0 to +70°C	*	*
Operating	–25°C to +85°C	*	*
Storage	–55°C to +85°C	*	*
Relative Humidity			
Non-Condensing to +40°C	0 to 85%	*	*
CASE SIZE	2" X 4" X 0.4"	*	*

*Specifications same as 2B54A.

[1] Gain nonlinearity is specified as a percentage of output signal span representing peak deviation from the best straight line; e.g. nonlinearity at an output span of 10V pk-pk (±5V) is ±0.02% or ±2mV.

[2] Response time can be reduced by addition of external resistors. More than one open input may cause output to saturate on all channels. To prevent this, use external resistors for a positive overscale response (Figure 8).

[3] Protected for shorts to ground and/or either supply voltage.

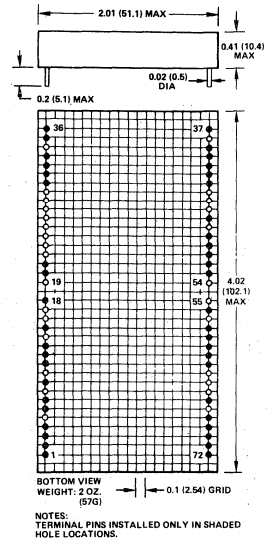
Specifications subject to change without notice.

MOUNTING CARDS AC1215, AC1216

The AC1215 and AC1216 mounting cards are available to assist in evaluation of the 2B54 and 2B55. These 4 1/2" X 6" printed circuit edge connector cards have sockets that allow a 2B54/2B55 and 2B56 to be plugged directly onto them, as well as offset adjustment pots, and address decoding circuitry. The AC1215 and AC1216 differ only in input signal connections: the AC1215 includes a screw terminal block and AC1216 has an edge connector.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



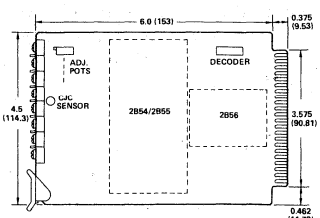
NOTES:
TERMINAL PINS INSTALLED ONLY IN SHADED HOLE LOCATIONS.

2B54/2B55 PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	– SELECT CH. D	37	HI
2	+ SELECT CH. D	38	
3	SW'D OUTPUT ENABLE	39	R_G
4	SWITCHED OUTPUT	40	R_G/COM CHANNEL A
5		41	LO/OFS
6	DIRECT OUTPUT	42	V- OUT
7	SENSE	43	V+ OUT
8		44	
9	OFS. ADJ.	45	
10		46	
11	$-V_S$	47	HI
12	COM	48	
13	$+V_S$	49	R_G
14		50	R_G/COM CHANNEL B
15	– SELECT CH. C	51	LO/OFS
16		52	V- OUT
17		53	V+ OUT
18	+ SELECT CH. C	54	
19		55	
20	– SELECT CH. B	56	HI
21	+ SELECT CH. B	57	
22		58	R_G
23		59	R_G/COM CHANNEL C
24		60	LO/OFS
25		61	V- OUT
26		62	V+ OUT
27		63	
28		64	
29		65	
30	$+V_{OSC}$ OSC. POWER	66	HI
31	COM OSC. POWER	67	
32	IN SYNC	68	R_G
33	OUT SYNC	69	R_G/COM CHANNEL D
34		70	LO/OFS
35	– SELECT CH. A	71	V- OUT
36	+ SELECT CH. A	72	V+ OUT

AC1215 OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



Mating Connector:
Cinch 251-22-30-160 or equivalent.

FUNCTIONAL DESCRIPTION

The internal structure of the 2B54/2B55 is shown in Figure 1. Four individually isolated input channels are multiplexed into a single output buffer, with the desired channel selected by control inputs SELECT A through SELECT D. Isolated power and timing signals for the input channels are provided by an internal oscillator.

Each channel contains an input protection and filtering network and a low-drift amplifier whose gain is set by a user-supplied resistor (R_G). Additional filtering is provided in the amplifier circuit. This structure preserves signal integrity by taking all signal gain ahead of the isolation and multiplexing circuits. The isolated power supply for each channel is brought out to permit convenient fine adjustment of the input offset voltage if desired.

Transformer coupling is used to achieve stable, reliable galvanic isolation of each channel from all other channels and from output ground. Although the bandwidth of the input channels is small (<2Hz at high gains) to provide immunity to normal-mode noise, the multiplexing technique allows the channels to be scanned at a high rate (400 channels/sec). Thus a high revisitation rate is maintained even in systems with a large number of input channels.

The output buffer amplifier operates at unity gain with feedback provided by an external connection from the DIRECT output to the SENSE input. The DIRECT output provides a ±5V swing with low source resistance to permit error-free operation with heavy loads. In addition, a separate series-switched output with an active-low enable control is provided so that multiple modules may be combined without the use of external analog multiplexers. An offset trim point which does not affect drift is also provided on the output channel.

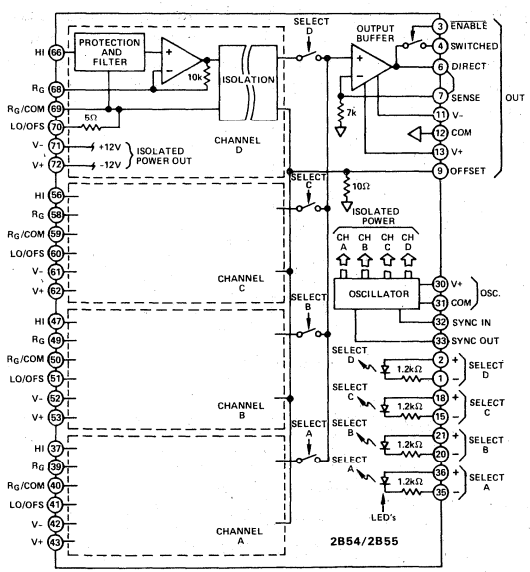


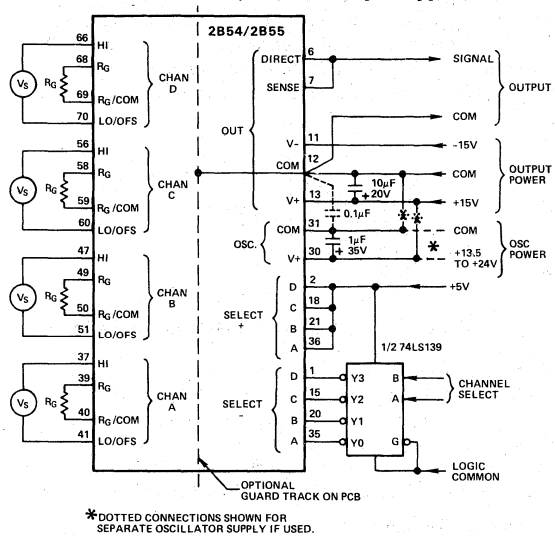
Figure 1. 2B54/2B55 Functional Diagram

The internal oscillator has its own power supply pins for enhanced application flexibility, and a sync mechanism is provided to eliminate beat-frequency errors when multiple 2B54/2B55's are used or when a system clock is present.

The 2B54 and 2B55 share the same design, differing only in input specifications and filter characteristics.

OPERATING INSTRUCTIONS

The connections shown in Figure 2 are common to most applications of the 2B54/2B55, and in many cases will be all that is required. The following sections describe this basic application and also detail some optional connections which enhance the module's utility in more complex applications.



*DOTTED CONNECTIONS SHOWN FOR SEPARATE OSCILLATOR SUPPLY IF USED.

Figure 2. Basic 2B54/2B55 Application

Interconnection Guidelines

In any high accuracy isolator application it is important to minimize coupling between input and output, and the 2B54/2B55 pinout has been designed to make this easy to do. For best results, keep all leads associated with signals on the input edge as far as possible from signals on the output edge. This will minimize the effects of board leakage and capacitance. The use of a guard track on both sides of the board (Figure 2) can also be helpful.

The power supplies should be decoupled with tantalum capacitors as close to the unit as possible. For lowest noise, the output grounding scheme should be as shown in Figure 2. The output signal common is connected directly to pin 12, with power supply returns brought separately to that pin so that power supply currents do not flow in the low lead of the signal output.

Since most of the power taken by the 2B54/2B55 is supplied to the internal oscillator which requires only a positive supply and can accommodate a wide range of supply voltages, it is sometimes desirable to power the oscillator from a convenient source of unregulated power (such as +24V – Figure 2). A 0.1µF capacitor should be then connected directly from pin 12 to pin 31. Since the output and oscillator circuits are not fully isolated, a dc path must exist between the two power supply commons. A small (one or two volts) potential difference between OUT COM and OSC COM will not affect operation.

Gain Setting

The gain of each channel is independently set by a user-supplied resistor (R_G) connected as shown in Figure 2. Channel gain will normally be selected so that the maximum output of the signal source will result in a plus or minus full scale (±5V) output swing. The resistor value required is $R_G = 10k\Omega/(G-1)$. Thus if $R_G = 101\Omega$, the gain will be 100, and an input signal swing of ±50mV will yield an output span of ±5V.

A parallel trim on the gain-setting resistor can be used to trim out the resistor's tolerance and the module's gain error (Figure 3). Since a parallel trim will always increase the gain, the value of the gain-setting resistor should be chosen to give an untrimmed gain somewhat lower than the desired trimmed gain. Good quality metal-film resistors should be used for R_G since gain accuracy and drift are a direct function of R_G's characteristics. Cermet pots are suitable for the trim.

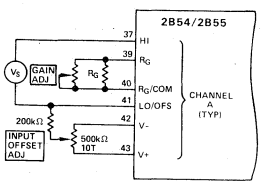


Figure 3. Input Offset and Gain Adjustments

Optional Offset Adjustment

The 2B54/2B55 has provision for fine adjustment of the input offset of each channel and the output offset of the entire module. None of the offset adjustments affect offset drift, and there is no need to make any adjustment unless the application calls for tighter offsets than those specified for the module type.

Connections for input offset adjustment are shown in Figure 3. This is a fine trim with a limited range (±250μV – 2B54 and ±1mV – 2B55, RTI), used to adjust each channel for zero offset while operating at the desired gain. Since the range of the input offset trim is small, it will usually be necessary to adjust output offset first. This can be conveniently done by operating one channel with zero input at unity gain (by disconnecting the gain resistor) and adjusting the output offset control for zero output. Connections for output offset adjustment are shown in Figure 4.

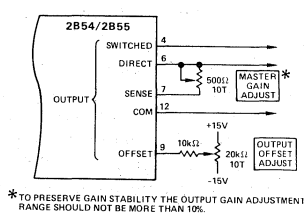


Figure 4. Output Offset and Master Gain Adjustments

An alternative offset adjustment procedure is appropriate in applications where the channel gains are field-selected by switching the gain-setting resistor. Here it is desirable to set the input offset so that there is no zero shift at the output when the gain is changed. To make the adjustment, switch back and forth from low to high gain with zero input and adjust the input offset control until no shift occurs at the output when changing gains. Then adjust the output offset control for zero output at the lower gain.

Stable components (a metal film resistor and a cermet pot) should be used for the input offset adjustment to avoid compromising drift. Output offset adjustment components are not critical and may be omitted altogether when a single 2B54/2B55 is followed by an A to D Converter that has a zero adjustment.

Channel Selection

Each channel in the 2B54/2B55 is turned on and off by a SELECT input. As indicated in Figure 1, each SELECT input consists of an LED in series with a resistor, and is not connected to any other circuits in the module. Turning the LED on (I≥2.5mA) turns the channel on, and turning the LED off (I≤50μA) turns the channel off. This allows considerable flexibility of connection, but the easiest way to use the SELECT inputs is to tie all four SELECT + pins to +5V and drive the SELECT–inputs from TTL logic (either open-collector or totem-pole outputs can be used), as shown in Figure 2.

It is also possible to use CMOS logic to drive the SELECT inputs (Figure 5). With a +15V logic supply a standard CMOS decoder or gate can supply enough current to drive the SELECT inputs directly, but at lower supply voltages it is advisable to use a buffer such as that shown in Figure 5b. The power taken by the SELECT inputs is small, since only one is on at a time, but at the higher CMOS supply voltages more current than the required 2.5mA will flow. This does not affect operation, but if desired the current can be brought back to the minimum value with series resistors as shown in Figure 5. Use 2kΩ for 10V operation, and 3.9kΩ at 15V.

The maximum reverse voltage applied to any SELECT input must be limited to 3V to avoid damage to the LED. Maximum forward current should be kept below 25mA. Each SELECT input is isolated from all other circuits in the module and may be operated up to ±50V away from output and power ground.

Channels may be selected in any order, and there are no restrictions on rate or duty cycle except the 2.5ms settling time for access to a channel. It should be noted, however, that selecting two or more channels simultaneously for more than a few microseconds will result in a very long settling time when the conflict is resolved. Timing overlaps should therefore be avoided.

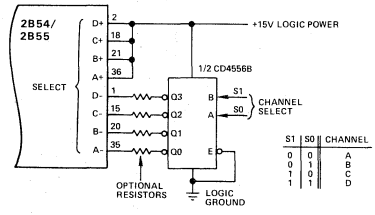


Figure 5a.

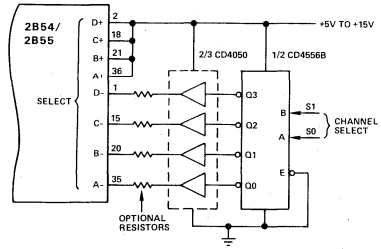


Figure 5b.

Figure 5. CMOS Channel Selection

Channel Expansion

The 2B54/2B55 has provision for directly interconnecting several modules when more than four channels are needed. The series-switched outputs of a group of modules are connected together, the SELECT inputs are driven in parallel, and the output of the desired module is selected using the Output Enable pin. This is shown in Figure 6. A single 74LS139 decoder is used to drive the SELECT inputs of up to four modules, and also provides address expansion so that the binary coded channel address word selects the appropriate module output via the Output Enable pins. The overall operation of the series-switched outputs is analogous to three-state logic, and the output rail is thus an analog bus.

It is possible to operate up to sixteen modules in parallel, for a total of 64 input channels. Note that it will be necessary to break up the SELECT inputs into several groups to avoid overloading the decoder when many modules are used. The settling time of the output switches is <50μs to ±0.01% and is thus negligible in comparison to the channel selection times.

The Output Enable signal is active low, and is compatible with both TTL and CMOS logic. The switching threshold is +1.8V; input current at 0V is typically -0.4mA.

The output resistance of the Switched Output (typically 35Ω +0.5%/°C) is low enough to provide fast switching times but will cause gain errors when driving a heavy load. A single buffer isolating the Switched Outputs from the load will solve this problem in an "analog bus" application (Figure 6). In single-module applications the DIRECT (low impedance) output should be used. Note that in all cases the SENSE pin *must* be connected to the DIRECT output to provide feedback for the output amplifier.

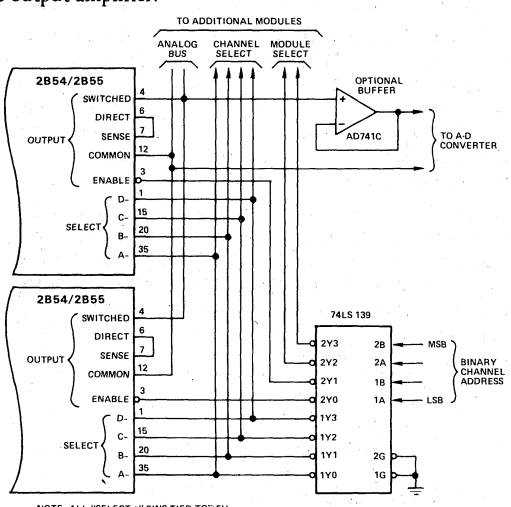


Figure 6. Expansion to More than Four Channels

Synchronization

In applications where multiple 2B54/2B55's are used in close proximity or when system clock signals are present near the isolator, differences in individual oscillator frequencies may cause "beat frequency" related output errors. To eliminate these errors, multiple units may be synchronized by connecting the SYNC OUT (pin 33) terminal to the SYNC IN (pin 32) terminal of the adjacent 2B54/2B55 (Figure 7). The first of a group of modules may be synchronized to an external source via the SYNC IN pin. To minimize noise pickup, sync wiring should be separated from analog signal runs.

The frequency of the external sync source, when used, will have a small effect on the gain and output offset of the 2B54/2B55. Thus any adjustments should be made with the module synchronized.

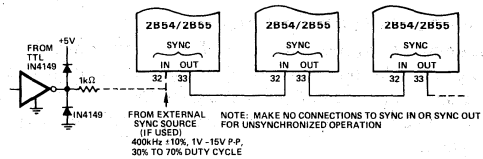


Figure 7. Synchronization

Open Input Detection

The 2B54 always responds to an open-circuit condition on a channel input by presenting a negative overscale (typically -7V) at the output when the affected channel is selected. The response time to detect an open input can be in the tens of seconds, since only a few nA of input bias current is available to charge the input filter. If shorter response times are desired, or if a positive overscale is the desired response, one of the circuits shown in Figure 8 can be used to augment or reverse the input bias current. Either circuit will produce a bias current of approximately 20nA which can be used to aid or oppose the 3nA typically supplied by the module, as shown. The circuit of Figure 8A has the advantage of simplicity, but the high-value resistor may not be readily available. Figure 8B shows how to solve the problem at the expense of complexity. The values shown may be modified to give an optimum trade of bias current for response time in a given application. A 2 to 5 second response is typical for the values shown.

The same circuits may be used to get open input detection with the 2B55, which is not specified for stand-alone open input response.

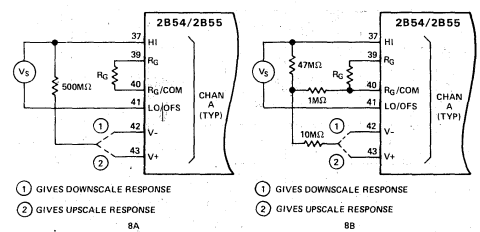


Figure 8. High Speed or Reversed Open Input Detection

Output Filtering

In most applications, no output filtering will be required since the effect of the small carrier-related noise spikes on the output (<1mV p-p, 100kHz B.W.) drops off rapidly as bandwidth decreases and in many cases will be negligible. In some applications (e.g., when driving a successive-approximation A to D) the effective system bandwidth may be large enough to pass the noise. To eliminate the carrier noise (without any effect on switching times), a simple R-C filter may be used at the output (Figure 9A). Only one filter is needed even when multiple modules are used, as shown in Figure 9B. If the load to be driven has an input resistance of less than 10MΩ, a buffer will be needed.

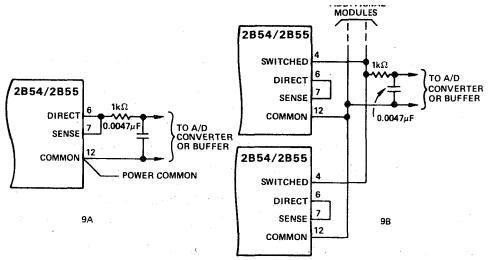


Figure 9. Output Filtering

CMR AND NMR PERFORMANCE

Common mode rejection is a result of both isolation and filtering and indicates ability to reject common mode inputs while amplifying differential signal inputs. CMR is dependent on source impedance imbalance, signal frequency and conditioner gain.

Normal mode rejection is also a function of the 2B54/2B55 gain. Figures 10 and 11 illustrate typical CMR and NMR performance. Note that any additional low pass filtering (e.g., an integrating A to D converter) at the output of the 2B54/2B55 will further improve both CMR and NMR performance.

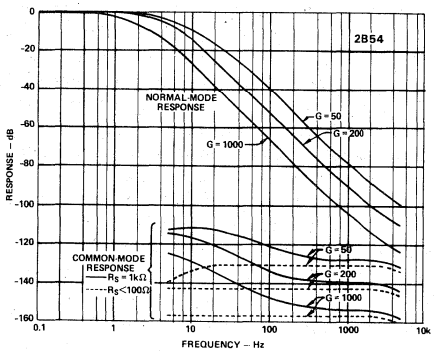


Figure 10. Common Mode and Normal Mode Response – Model 2B54

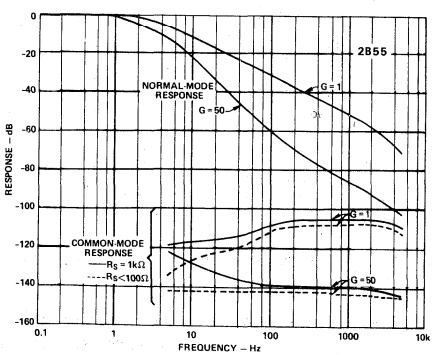


Figure 11. Common Mode and Normal Mode Response – Model 2B55

APPLICATIONS

Thermocouple Temperature Measurement: Figure 12 shows a four-channel thermocouple input system with isolation, amplification, and multiplexing provided by the 2B54. Several different thermocouple types are used, and the gain-setting resistors on each channel have been chosen to take the standard ANSI range for each type to a 5V output span. Since thermocouples must be compensated for the temperature of the reference junction which is formed where the thermocouple leads are terminated, the 2B56 Universal Cold Junction Compensator is used. The 2B56 monitors the temperature of the reference junction (terminal block) via an external sensor and corrects the signal at the output of the 2B54 for reference temperature. Compensation for several thermocouple types is selectable via digital control inputs. Thermocouple linearization, if needed, would be typically performed in system's software.

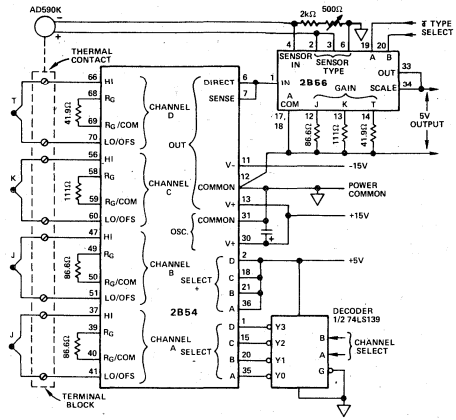


Figure 12. Four-Channel Thermocouple Temperature Measurement with Cold Junction Compensation

Process Signals Interface: In Figure 13, the 2B55 is used to provide floating inputs for four 4-20mA process signal loops. The use of floating inputs in this type of application gives protection from common-mode voltages and greatly simplifies system configuration, since additional loads in series with the loop can be connected on either side of the isolator input.

Each current input is converted into a 1 to 5 volt signal by a 250Ω resistor. The 2B55 is operated at unity gain (no gain-setting resistors) so that a 1 to 5 volt signal appears at the output. Since no gain-setting resistors are used, gain adjustment, if required, is done by connecting trims directly across the input resistors. Other current ranges can be accommodated by changing the value of the input resistors.

When there are several loads on the loop, compliance voltage at the transmitter may be at a premium. In this case it will be advantageous to reduce the voltage swing at the isolator inputs by using smaller resistors (perhaps 25Ω) and scaling the output back to a 5V span by taking an appropriate gain in the isolator.

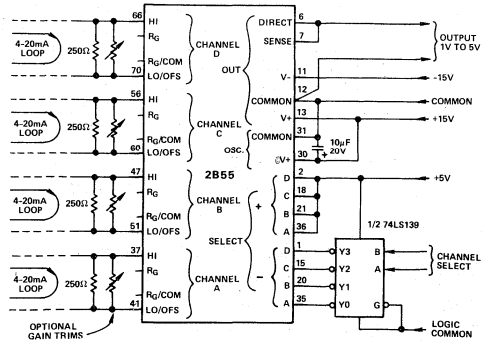


Figure 13. Isolated 4-20mA Loop Signals Interface

High Accuracy, Thermocouple Cold Junction Compensator

MODEL 2B56

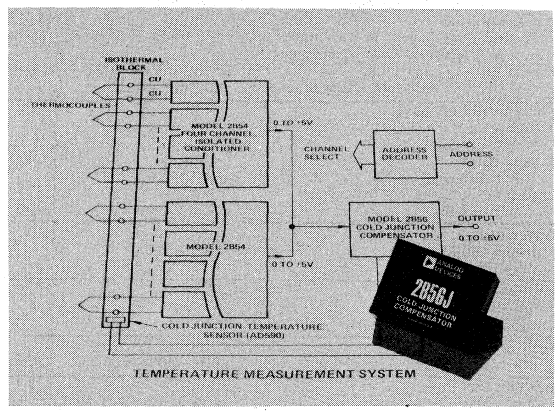
FEATURES

Universal Thermocouple Compensation:
- **Internally Provided: Types J, K, T**
- **User Configurable: Types E, R, S, B**

Digitally Programmable
High Accuracy: ±0.8°C max over +5°C to +45°C
High Ambient Rejection: 50 to 1 min.
Low Cost
Small Size: 1.5" X 2" X 0.4"

APPLICATIONS

Thermocouple Signal Conditioning
Temperature Measurement and Control Systems
Temperature Data Acquisition and Logging
Temperature Controllers



TEMPERATURE MEASUREMENT SYSTEM

9

GENERAL DESCRIPTION

Model 2B56 is a high accuracy, universal thermocouple cold junction compensator. Designed to operate with an external temperature sensor in thermal contact with the cold junction, the 2B56 provides an automatic compensation for amplified thermocouple signals over wide ambient temperature variations. The 2B56 is calibrated to compensate the cold junction to a reference temperature of 0°C. The total compensation error is ±0.8°C max over +5°C to +45°C.

Designed to compensate seven different thermocouple types, the 2B56 may be digitally programmed to select compensation for types J, K and T, and one user programmed type (E, R, S, B or none). This feature makes the 2B56 especially suitable for multichannel applications involving several thermocouple types.

COLD JUNCTION COMPENSATION PRINCIPLES

In thermocouple measurements, temperature is determined by measuring the potential difference between the measurement (hot) junction of two dissimilar metals and the reference (cold) junction which is formed when thermocouple leads are connected to a measuring circuit. Since this potential difference is proportional to the temperature difference between the measurement temperature and the temperature at the reference junction, the reference junction temperature must be known. Changes in reference junction temperature influence the output voltage and, therefore, cold junction compensation is required to eliminate measurement errors.

Two methods may be used to reduce errors introduced at the thermocouple connections: keep the reference junction at a known constant temperature, or measure the reference junction temperature and cancel the changes by the appropriate correction to the thermocouple output signal. The first method, accomplished by immersing the reference junction in an ice bath maintained at 0°C is not very practical. The 2B56 employs the second method and has been specifically designed to eliminate the need for ice baths by electronically simulating the desired reference point. Digital programmability, high accuracy and low cost make the 2B56 ideal for single or multichannel thermocouple temperature measurement, indication or control systems.

FUNCTIONAL DESCRIPTION

The 2B56 compensates for cold junction temperature by adding a correction signal at the output of the user's thermocouple amplifier, as shown in Figure 1. The value of the correction signal is determined by the cold junction temperature, as measured by a sensor, and the thermocouple type in use, as specified by two digital TYPE SELECT inputs. Since compensation is done at the output of the thermocouple amplifier it is also necessary to scale the correction signal for the gain of the amplifier. This is done by a scaling circuit which has provision for a user-supplied gain-setting resistor for each thermocouple type in use.

Compensating networks for thermocouple types J, K, and T are built into the 2B56. A fourth compensation (X) can be programmed with two external resistors for any other thermocouple type. The X compensation can also be used without programming resistors to obtain an uncompensated output when sensors other than thermocouples are in use.

SPECIFICATIONS (typical @ +25°C, V_S = ±15V unless otherwise noted)

MODEL	2B56A
COLD JUNCTION COMPENSATION	
Thermocouple Types:	
Internally Compensated	J, K, T
Externally Programmable	B, E, R, S, None
Reference Temperature	0°C
Compensation Accuracy	
Total Output Error @ +25°C[1]	±0.2°C
vs. Ambient Temperature (+5°C to +45°C)[1]	±0.8°C max
Compensation Error	
vs. Sensor Temperature (+5°C to +45°C)[2]	±0.4°C max (±0.15°C typ)
vs. Compensator Module Temperature (0 to +70°C)[3]	±0.02°C/°C max (0.01°C/°C typ)
Cold Junction Temperature Sensing Element	AD590 or 2N2222
INPUT SPECIFICATIONS	
Voltage Signal Range	±10V
Input Impedance	100kΩ
Signal Gain[4]	+1V/V
vs. Temperature	±10ppm/°C
Input Offset Voltage	±1mV max
vs. Temperature	±15μV/°C max
OUTPUT SPECIFICATIONS[5]	
Output Voltage	±10V @ ±5mA
Output Impedance	0.1Ω
DYNAMIC RESPONSE	
Selection Settling Time	0.5ms
Signal Settling Time, to ±0.01%	50μs
DIGITAL INPUTS	
Select Inputs A & B	TTL, CMOS Compatible
POWER SUPPLY	
Analog, Rated Performance	±15V dc ±10% @ ±5mA
Operating	±12V to ±18V dc
Digital, V_{DD}	+5V to +15V dc @ 2mA max
TEMPERATURE RANGE	
Rated Performance	0 to +70°C
Operating	−25°C to +85°C
Storage	−55°C to +125°C
CASE SIZE	1.5" X 2" X 0.4"

[1] Total compensation error composed of errors of temperature sensor and module at the same ambient temperature.
[2] Compensation error contributed by ambient temperature changes at temperature sensor.
[3] Compensation error contributed by ambient temperature changes at the module.
[4] Signal gain of 2 is also available by jumper selection.
[5] Protected for shorts to ground or either supply voltage.

Specifications subject to change without notice.

Type	Max Gain for Sensor Temp to +45°C	to +70°C
J	1000	650
K, T	1300	820
E	870	550
R, S	9000	5500
B	Any	Any

Table I. Maximum Gain vs. Sensor Temperature and Thermocouple Type

Type	RX1	RX2
E	412kΩ	1.43kΩ
R, S	412kΩ	121Ω

Table II. Resistor for Compensating Types E, R and S

Type Sel. Logic B	A	Compensation
0	0	J
0	1	K
1	0	T
1	1	X

Table III. Digital Selection of Compensation Type

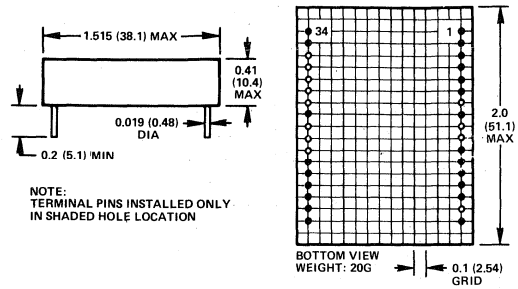
Sensor Temp (°C)	V_{CAL} (mV) 2N2222	AD590
5	616.5	634.5
10	604.9	645.9
15	593.3	657.3
20	581.6	668.7
25	570.0	680.1
30	558.4	691.5
35	546.8	702.9
40	535.1	714.3
45	523.5	725.7

Values may be interpolated

Table IV. Calibration Voltage vs. Sensor Temperature

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	SIGNAL INPUT	18	ANALOG COMMON
2	SENSOR SELECT	19	E TYPE SELECT
3	SENSOR SELECT	20	E TYPE SELECT
4	SENSOR INPUT	21	$+V_{DD}$
5	SENSOR SELECT	22	DIGITAL COMMON
6	SENSOR SELECT	23	$+V_S$
7		24	
8	V_{REF}	25	
9		26	
10		27	$-V_S$
11	"X" COMPENSATION	28	
12	TYPE J	29	
13	TYPE K (GAIN SELECT)	30	
14	TYPE T (GAIN SELECT)	31	
15	TYPE "X" (GAIN SELECT)	32	
16		33	OUTPUT
17	ANALOG COMMON	34	SCALE

MATING SOCKET: AC1217

A buffer amplifier is provided at the output of the 2B56 to preserve accuracy when driving heavy loads. The gain from V_{IN} to V_{OUT} will be +1 when SCALE is connected to V_{OUT} (see Figure 1). Input and output signal swings of up to ±10V can be accommodated with this connection. When the SCALE pin is left open, the gain from V_{IN} to V_{OUT} is +2. This is useful when interfacing a thermocouple amplifier with a ±5V output swing (such as the 2B54) to an A to D converter with a ±10V input range.

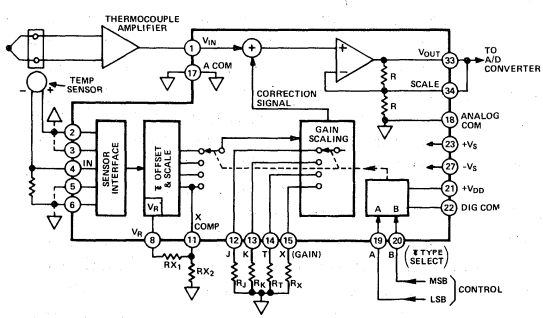


Figure 1. 2B56 Functional Block Diagram

It should be noted that the 2B56 is designed for use with noninverting thermocouple amplifiers. Thus a positive voltage change at the input of the 2B56 must indicate increasing temperature.

OPERATING INSTRUCTIONS

Temperature Sensors: The temperature sensor used with the 2B56 can be either the Analog Devices AD590 temperature transducer or the popular 2N2222 transistor. Either sensor type can be used without loss of accuracy, but each has advantages in different applications. The 2N2222 (the metal can version must be used) is widely available at very low cost. However, an adjustment must be made whenever the sensor is replaced. The AD590 is available in several precalibrated accuracy grades, but at somewhat higher cost.

Connections are shown for both sensor types in Figure 2. Resistor R_{CAL} is the calibration adjustment point. It is used only to adjust for unit-to-unit variations in the sensors. All other adjustments have been made internal to the 2B56.

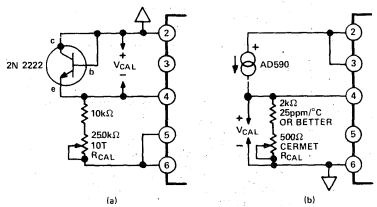


Figure 2. Sensor Connections and Calibration

With either sensor type, proper placement of the sensor is important. Close thermal contact of the sensor and the thermocouple termination point (reference junction) is necessary, particularly when nearby heat sources are present, since these could cause the sensor temperature to differ from the reference junction temperature. In multichannel applications, care should be taken to keep all input terminals at the same temperature to avoid channel-to-channel errors. The sensor may be placed at any distance from the 2B56. When the sensor leads are more than ten feet long, or where strong noise sources are present, shielded cable should be used with the 2N2222 sensor. The AD590 will operate properly with twisted-pair leads at distances up to a few hundred feet.

Gain Selection: Since the 2B56 performs cold junction compensation at the output of the user's thermocouple amplifier, it must take the gain of that amplifier into account. For this purpose, four gain-programming pins are provided: one each for the J, K, and T compensations and one for the X (user-selected) compensation. Thus the user's thermocouple amplifiers can have different gains for each thermocouple type in use, and the 2B56 gain will be selected automatically when the thermocouple type is selected at the digital TYPE SELECT inputs. Gain-programming resistors are connected as shown in Figure 1. The value of each resistor is $R = 10k\Omega/(G-1)$ where G is the gain of the user's thermocouple amplifier from the thermocouple terminals to the input of the 2B56. As an example, if the thermocouple amplifiers in use have a gain of 110 for type J, 90 for type K, and 220 for type T, then R_J = 91.7Ω, R_K = 112Ω, and R_T = 45.7Ω. Gain resistor pins for unused thermocouple types must be grounded. The resistors used to set gain should have a tolerance of 1% or better. A 1% error in setting gain will result in a 0.01°C/°C slope error.

The gain of the thermocouple amplifier will normally be determined by the thermocouple type, temperature measurement range, and A to D converter input range, but there are some practical limits imposed by the 2B56. The minimum allowable gain for proper operation is 40. The maximum gain which can be used is limited by the dynamic range of the compensation circuits in the 2B56, and is a function of thermocouple type and the temperature range (at the sensor) over which compensation is to be effective. Table I lists the maximum gain for each thermocouple type both for the specified +5°C to +45°C sensor temperature range and for a wider (reduced accuracy) 0 to +70°C range.

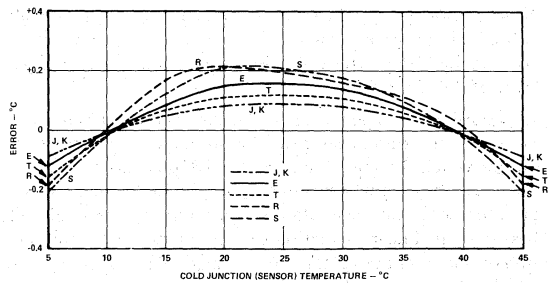


Figure 3. Error Due to Thermocouple Nonlinearity

Compensation of Other Thermocouple Types: Compensation for type J, K, and T thermocouples is built into the 2B56. A fourth compensation can be added by installing two resistors (R_{X1} and R_{X2}) as shown in Figure 1. Table II gives the values needed for proper compensation of type E, R, and S thermocouples. Type B thermocouples are a special case, in that they have almost no output in the +5°C to +45°C range, and therefore, do not need cold junction compensation at all. To accommodate a type B thermocouple, select No Compensation (described in the next section). Errors due to cold junction temperature will be less than ±1°C for any measurement temperature above 260°C. In the measurement range beyond 1000°C (where type B thermocouples are normally used) the error will be less than ±0.3°C.

No Compensation Operation: In some instances it may be desirable to disable the compensation function of the 2B56, so that it functions as a straight-through amplifier with a gain of one (or two, if the output scaling feature is used). This might be done, for example, in a multichannel system with a mixture of thermocouples and strain gage signals or other sources requiring no compensation. It is also necessary when using the type B thermocouple, as described above. The X compensation can be programmed to provide no compensation by grounding pin 11 (X COMP), Figure 1. A 200Ω resistor should be used for R_X (at any gain). Selecting X compensation with this connection will give an uncompensated output.

Digital Inputs: The TYPE SELECT inputs are compatible with TTL or CMOS logic, or may be used with jumpers or switches. Table III shows the truth table for these inputs. Each input has an internal 22kΩ pullup resistor to V_{DD} and drives a single CMOS gate. For use with TTL signals, V_{DD} should be connected to the +5V logic supply. When CMOS logic is used, connect V_{DD} to the CMOS logic power supply (which must be in the +5V to +15V range). If jumpers or switches are used, connect V_{DD} to the +15V analog power supply. Grounding a SELECT input will give a logic "0"; an open input will be at logic "1" due to the action of the internal pullups.

A separate pin is provided for logic ground to minimize ground loop problems. However, for proper operation logic ground at the module must be within ±0.3V of analog common. Failure to observe this restriction may result in damage to the module.

Calibration: Only one adjustment is necessary to get proper operation of the 2B56. This is shown in Figure 2 for both sensor types. R_{CAL} is adjusted to obtain the correct voltage at V_{CAL} for the appropriate sensor type and temperature, as listed in Table IV. Use a high-impedance voltmeter to measure V_{CAL} to prevent loading errors.

The tolerance to which the calibration adjustment must be made depends on the requirements of the application. For either sensor type, and for all thermocouple types, each millivolt of calibration error will result in a temperature offset error at the 2B56 output of 0.44°C, accompanied by a slope error of 0.0015°C/°C.

Curvature Error: The voltage output of thermocouples is a nonlinear function of temperature, so the reference junction output which is compensated by the 2B56 is also nonlinear. The correction signal generated by the 2B56, however, is approximately linear. The 2B56 is adjusted internally to give the best fit of its linear correction to the nonlinear reference junction output over the +5°C to +45°C range. The remaining error, which is included in the specifications given on page 2, is shown for each thermocouple type in Figure 3. Note that as a result of thermocouple nonlinearity the error at +25°C will not be zero after calibration is done. The error for a particular thermocouple type could be adjusted to zero at +25°C by appropriate adjustment of the thermocouple amplifier offset, but the improvement will be at the expense of increased errors over the +5°C to +45°C range.

APPLICATIONS

The application of the 2B56 to a single-channel system is shown in Figure 1. Because the 2B56 compensates at the output of the thermocouple amplifier, it is also very attractive for use in multiplexed multichannel systems. Three typical applications are shown in Figure 4. The amplifier-per-channel structure shown in Figure 4a is one example of a system which could have a different gain for each thermocouple type in use, with channels preassigned or switchable for thermocouple type.

The model 2B30 may be used as an amplifier for applications not requiring isolation.

In systems of this type, it is important that the ON resistance of the multiplex switches be less than 100 ohms, since larger values can create slope errors in the 2B56. If switches with higher resistance are used, a unity-gain buffer should be placed between the multiplexer and the 2B56. An AD741 or AD301-type amplifier will suffice unless the system is very fast.

Figure 4b shows an input-multiplexed system. Different gains for different channels in this type of system are sometimes provided by software control of the amplifier gain. The 2B56 can also accommodate this situation, since it can accept a different gain for each thermocouple type.

Figure 4c shows a somewhat different application of the 2B56. Here the signal input is grounded, so that the output is simply the correction signal rather than a corrected version of the input. In this case the actual summation is done elsewhere, usually in the processor following the A to D converter. The advantage of such a structure is that it allows somewhat simpler calibration of the individual channels because the compensator can be bypassed.

There is no electrical limit to the number of channels that can be served by a single 2B56 in these applications or the many others that are possible. There is, however, a thermal limit in that a single temperature sensor must accurately monitor the temperature of a number of sets of input terminals. The actual channel limit will thus be determined by the allowable error and the degree to which all the inputs can be held at the same temperature.

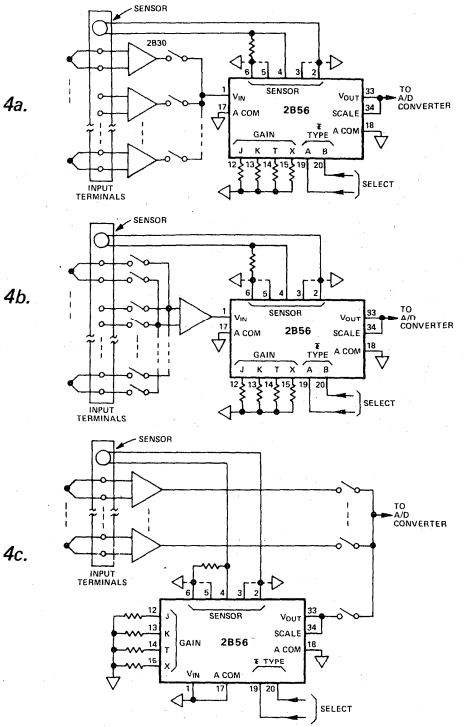


Figure 4. Model 2B56 in Various Multichannel Applications

Figure 5 shows the application of the 2B56 to the output of the 2B54 Four-Channel Isolator. More than one 2B54 can be served by the same 2B56 by using the built-in output switches of the 2B54 to connect several isolators to one output line. Note that the values of the gain-setting resistors for the 2B54 and 2B56 are the same, since both have the same gain formula. This permits very simple reconfiguration when the system must be tailored for new applications.

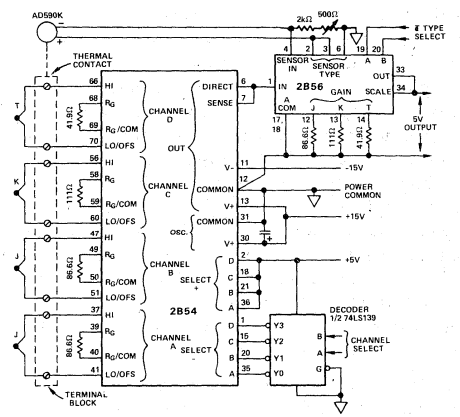


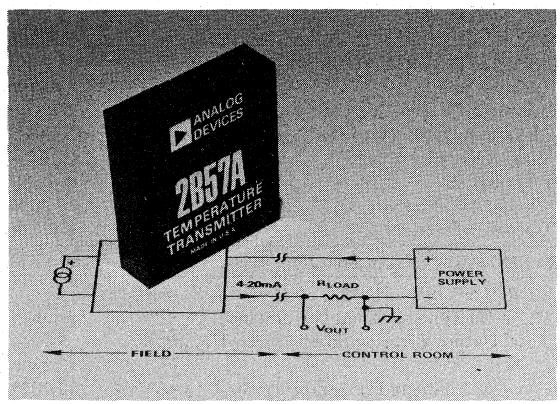
Figure 5. Four-Channel Thermocouple Temperature Measurement with Cold Junction Compensation

Low Cost, Two-Wire Temperature Transmitter

MODEL 2B57

FEATURES
- Low Cost
- Compatible with Standard 4-20mA Loops
- Low Span Drift: ±0.005%/°C max
- Low Nonlinearity: ±0.05% max
- RFI Immunity
- Small Size: 1.5″ × 1.5″ × 0.4″

APPLICATIONS
- Temperature Monitoring and Control
- Remote Temperature Sensing
- Process Control Systems
- Energy Management Systems



9

GENERAL DESCRIPTION

The model 2B57 is a low cost, two-wire temperature transmitter designed to interface with Analog Devices' AD590 temperature transducer and produce a standard 4 to 20mA output current proportional to the measured temperature. The 2B57 features a low span drift of ±0.005%/°C max, a high linearity (±0.05% max) and high noise immunity to assure measurement accuracy in harsh industrial environments.

The transmitter accommodates the AD590 temperature measurement range of −55°C to +150°C. Both zero and span adjustments are provided to trim the range for input measurement spans between 20°C and 205°C. The transmitter output of 4 to 20mA and a wide range of power supply voltages make the 2B57 compatible with standard two-wire control loops.

The basic package is a small (1.5″ × 1.5″ × 0.4″), rugged, epoxy encapsulated module. For applications requiring protective housing, the 2B57 is available in a versatile metal case.

APPLICATIONS

The 2B57 has been specifically designed to provide low cost, accurate and reliable temperature measurement in any applications below +150°C in which conventional electrical temperature sensors and transmitters are currently employed.

Industrial applications in process control and monitoring systems include chemical, petroleum, food processing, power generation and a wide variety of other industries.

In multipoint energy management applications, low cost and small size combine to make the AD590 and 2B57 ideal for mounting in standard utility or thermostat boxes for remote temperature sensing.

DESIGN FEATURES AND USER BENEFITS

RFI Noise Immunity: The transmitter incorporates RFI filtering circuitry to assure protection against radio frequency interference.

Low Cost: The low cost of the 2B57 transmitter and two-wire operation reduce total system installation cost.

Linear Output: The transmitter output is linear with temperature, thus eliminating the need for linearizing circuitry.

Standard Loop Compatibility: The two-wire output structure conforms to the Instrument Society of America Standard ISA-S50.1 "Compatibility of Analog Signals for Electronic Industrial Process Instruments."

SPECIFICATIONS (typical @ +25°C and V_S = +24V dc, unless otherwise noted)

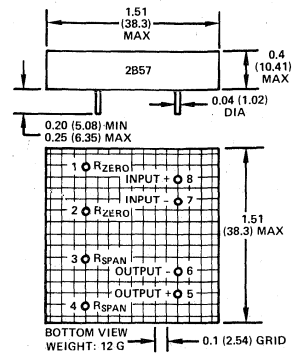
MODEL	2B57A
INPUT SPECIFICATIONS	
Sensor Type[1]	AD590
Maximum Temperature Measurement Range	-55°C to +150°C
Minimum Input Span (for a 4-20mA Output)	20°C
Zero Adjustment Range	-55°C to +60°C
Input Protection[2]	+50V dc
Open Input Detection	Upscale
OUTPUT SPECIFICATIONS	
Output Span	4 to 20mA
Minimum Output Current	2.5mA
Maximum Output Current	26mA
Load Resistance Range	
Equation	$R_{LMAX} = (V_{SUPPLY} - 12V)/20mA$
@ +24V Supply	0 to 600Ω max
Output Protection[2]	+50V dc
NONLINEARITY (% of Span)	±0.02% typ (±0.05% max)
ACCURACY	
Warm-Up Time to Rated Performance	1 min
Total Output Error, without External Trims[3]	
Zero	±0.2% typ.(±0.5% max)
vs. Ambient Temperature (-30°C to +85°C)	±0.005%/°C typ (±0.01%/°C max)
Span	±0.2% typ (±0.5% max)
vs. Ambient Temperature (-30°C to +85°C)	±0.001%/°C typ (±0.005%/°C max)
RESPONSE TIME, to 90% of Span	0.15 sec
POWER SUPPLY	
Voltage, Rated Performance	+24V dc
Voltage, Operating	+12V to +50V dc
Supply Change Effect, % of Span	
on Zero	±0.005%/V
on Span	±0.001%/V
ENVIRONMENTAL	
Temperature Range, Rated Performance	-30°C to +85°C
Storage Temperature Range	-55°C to +100°C
Relative Humidity, to +40°C	0 to 90%
RFI Effect (5W @ 420MHz @ 3 ft)	
Error, % of Span	±0.5% max
CASE SIZE	1.5″ X 1.5″ X 0.4″

NOTES
[1] AD590 produces an output current proportional to absolute temperature (1μA/°K).
[2] Protected for any combination of input and output pins.
[3] Accuracy is specified as a percent of output span (16mA) for an input range of -55°C to +150°C. Accuracy spec includes combined effects of transmitter repeatability, hysteresis, and linearity. Does not include sensor error.

Specifications subject to change without notice.

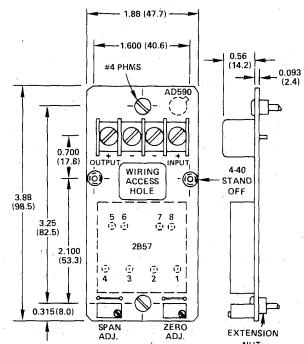
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



MOUNTING CARD AC1583 OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



The AC1583 mounting card is available to assist in applying the 2B57. The AC1583 is suitable for mounting in a standard 2″ X 4″ thermostat or electrical boxes. It includes screw terminals for field wiring, provisions for plugging in the 2B57 and AD590, and 5kΩ span and zero adjustment pots.

FUNCTIONAL DESCRIPTION

The 2B57 transmitter converts the output of an AD590 temperature transducer to a current output within a span of 4 to 20mA. The transmitter includes input protection and filtering circuitry, an amplifier, voltage regulator, precision voltage reference and an output current generator.

A precision voltage reference, resistor network, and span and zero adjusts are used in conjunction with a low current drain amplifier to scale output signal of the AD590. The amplifier drives a current generator which controls output current (Figure 1).

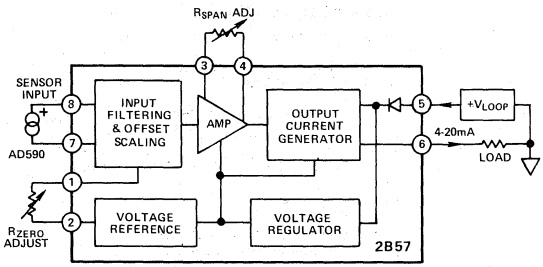


Figure 1. Model 2B57 Functional Block Diagram

Input power and output signal are transmitted over the same two leads. The load resistance is connected in series with a dc power supply, and the current drawn from the supply is the 4 to 20mA output signal. The maximum series load resistance depends on the supply voltage and is given by $R_{LMAX} = (+V_S - 12V)/20mA$. A wide range of power supply voltages may be used (see Figure 2).

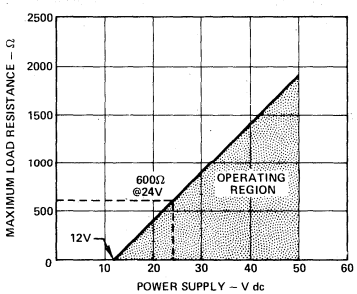


Figure 2. Maximum Load Resistance vs. Power Supply

THE SENSOR

The AD590 is a calibrated two terminal temperature sensor producing a current in microamperes ($1\mu A/^\circ K$) that is linearly proportional to absolute temperature for temperatures from $-55^\circ C$ to $+150^\circ C$. The AD590 sensor is available in a hermetically sealed TO-52 transistor package, a miniature flat-pack, chip form and stainless steel probes (AC2626). The sensor construction assures reliable isolation from ground.

The AD590 is available in several accuracy grades, as shown in Table 1. The grade selection will depend on whether the device is used uncalibrated or with calibration at a single value. For greater accuracy (in any grade), the device may be calibrated at two points.

TABLE 1. AD590 ACCURACY SPECIFICATIONS (MAX ERROR)

Conditions	Max Error (±°C)				
Grade	I	J	K	L	M
Error at 25°C, as delivered	10.0	5.0	2.5	1.0	0.5
Errors over the −55°C to +150°C range:					
Without external calibration	20.0	10.0	5.5	3.0	1.7
With error nulled at 25°C only	5.8	3.0	2.0	1.6	1.0
Nonlinearity	3.0	1.5	0.8	0.4	0.3

OPERATING INSTRUCTIONS

Model 2B57 is factory calibrated to ±0.5% accuracy for a maximum sensor measurement range of $-55^\circ C$ to $+150^\circ C$ ($205^\circ C$ span) with R_{SPAN} and R_{ZERO} resistor values as shown in Figure 3. For this input range 4mA output corresponds to an AD590 temperature of $-55^\circ C$ and 20mA to $+150^\circ C$. The span and zero adjustments can be used to accommodate other input ranges.

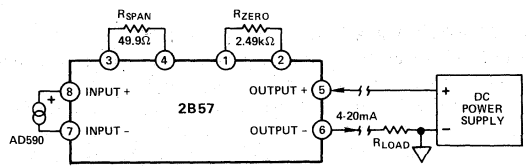


Figure 3. Model 2B57 Basic Application

Span Adjustment: The value of the span setting resistor R_{SPAN} is determined by:

$$R_{SPAN}\ (\Omega) = \left(\frac{1.2V}{10^{-6}\ A \times SPAN}\right) - 5810\Omega$$

where SPAN is a desired measurement span in °C. For example, for a measurement span of $100^\circ C$ R_{SPAN} = $\left(\frac{1.2V}{10^{-6}\ A \times 100}\right) - 5810\Omega = 6.19k\Omega$. If a span accuracy of ±0.5% if desired, the value of the R_{SPAN} resistor should be accurate to ±0.1%.

Zero Adjustment: Zero adjustment must be performed after installation of the R_{SPAN} resistor. To select R_{ZERO} an AD590 or a calibrated current source may be used as an input to the 2B57. If an AD590 is used, it must be maintained at the desired reference temperature. A resistance decade box is inserted between pins 1 and 2 of the 2B57. The decade box is adjusted to produce an output corresponding to the selected reference temperature. For example, for a sensor measurement range of 0 to $100^\circ C$ and an AD590 at $0^\circ C$, the R_{ZERO} is adjusted for an output current of 4mA. If a current source is used, its output must equal the AD590 output at the selected reference temperature. For example, at $0^\circ C$ the current source output must equal $273.2\mu A$.

Sensor Calibration Trim: The sensor calibration error is the major contributor to maximum total error in all AD590 grades. To trim this error the temperature of the AD590 is measured by a reference temperature sensor and R_{ZERO} is trimmed to the calculated value of the 2B57 output current at that temperature. A reference temperature at the midpoint in the span should be selected.

measurement accuracy over temperature, R_{ZERO} and R_{SPAN} should be trimmed with the AD590 at two known temperatures. For example, with the R_{SPAN} selected for a 100°C span and with the AD590 at 0°C R_{ZERO} is adjusted for a 4mA output. R_{SPAN} is then trimmed for a 20mA output with the sensor at 100°C. Figure 4 illustrates a typical two-trim system accuracy.

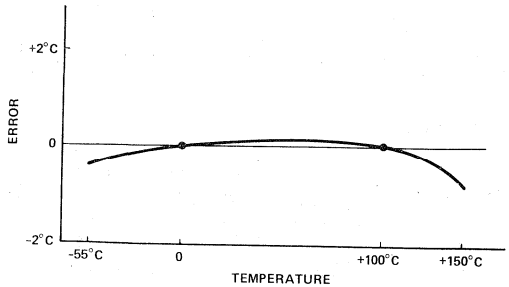


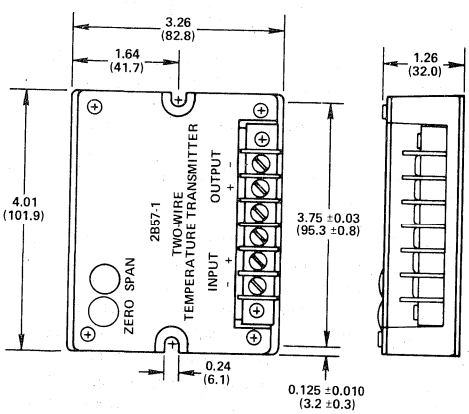
Figure 4. Typical Two-Trim Accuracy (AD590 and 2B57)

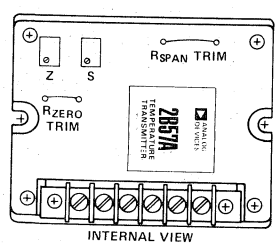
OPTIONAL PACKAGING CONFIGURATION (2B57A-1)

The 2B57 is available mounted in an aluminum case including screw terminals for connecting an external sensor and power. This versatile housing may be surface mounted in racks, cabinets, NEMA enclosures, etc., or snapped onto standard relay tracks. The 2B57 in a metal housing is calibrated for a −55°C to +150°C measurement range and may be ordered by specifying model 2B57A-1.

TRANSMITTER HOUSING OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).





Refer to operating instructions section for suggested method of calibration.

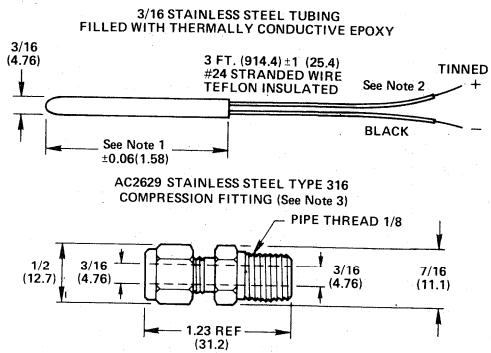
AC2626 PROBE (AD590 PACKAGING OPTION)

The AC2626 is a stainless steel tubular probe measuring 3/16 inch (4.76mm) in outside diameter and is available in 6 inch (152.4mm) or 4 inch (101.6mm) lengths. Based on the AD590F, the probe is available in linearity grades of 0.3°C, 0.4°C, 0.8°C or 1.5°C and is compatible with the 2B57 transmitter. The mechanical outline of the AC2626 is shown below.

The probe is designed for both liquid and gaseous immersion applications as well as temperature measurements in refrigeration or any general temperature monitoring applications.

AC2626 MECHANICAL OUTLINE

Dimensions shown in inches and (mm).



NOTE 1 Probes are available in 4-inch or 6-inch lengths. Other lengths are available; consult factory for price and delivery.

NOTE 2 + lead wire is color coded: J, yellow; K, orange; L, blue; M, .

NOTE 3 When assembling compression fitting (AC2629) to probe, tighten the 1/2" nut 3/4's of a turn from finger tight.

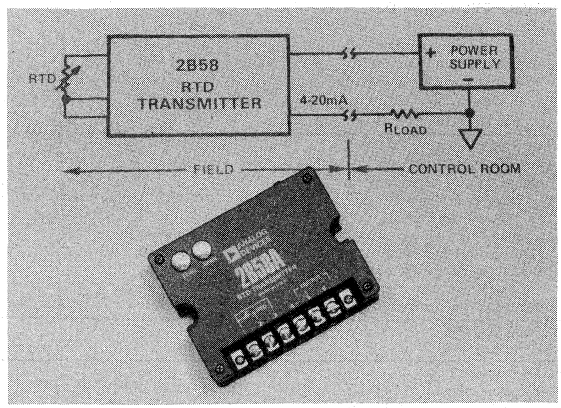
Two-Wire, Linearized RTD Temperature Transmitter

MODEL 2B58

FEATURES
- Platinum RTD Input
- Linearized 4-20mA Output
- High Accuracy: ±0.1%
- Low Drift: ±0.01°C/°C Max
- RFI Immunity
- Low Cost

APPLICATIONS

RTD Temperature Transmission in:
- Process Control
- Factory Automation
- Energy Management



9

GENERAL DESCRIPTION

The model 2B58 is a high accuracy, two-wire temperature transmitter designed to accept a platinum RTD (Resistance Temperature Detector) input and produce a proportional standard 4-20mA output. The RTD signal is internally linearized to provide an output which is linear with temperature. Four precalibrated ranges are available for RTD measurements from -100°C to +400°C.

The 2B58 features high accuracy of 0.1%, low drift of ±0.01°C/°C, high noise rejection and RFI immunity. Both two-wire and three-wire 100Ω sensors may be used. Lead wire compensation is provided for three-wire RTDs.

A rugged metal enclosure, suitable for field mounting, offers environmental protection and screw terminal input and output connections. This enclosure may be either surface or standard relay track mounted.

APPLICATIONS

The 2B58 has been specifically designed to provide high-performance two-wire transmission of measured temperatures using RTD sensors.

Two-wire current transmission permits remote mounting of the transmitter near the sensor to minimize the effects of noise and signal degradation to which low level sensor outputs are susceptible. Transmission of the proportional current output may be accomplished by means of inexpensive copper wires. These factors make the 2B58 ideally suited for applications where accuracy, stability, and low cost installation are desired.

DESIGN FEATURES AND USER BENEFITS

High Accuracy: The 2B58 offers high calibration accuracy, linearized output and conformity with the standard DIN 43760 (α = 0.00385) RTD sensors.

Low Cost: The 2B58 combines low price with a two-wire transmission, lowering total installation cost.

High Noise Rejection: The transmitter features internal filtering circuitry to assure protection against RFI and line frequency pickup.

Standard Loop Compatibility: The two-wire output structure conforms to the ISA Standard S50.1 "Compatibility of Analog Signals for Electronic Industrial Process Instruments".

Wide Operating Temperature Range: The 2B58 has been designed to operate over -30°C to +85°C ambient temperature range.

OPERATING INSTRUCTIONS

The 2B58 is designed to operate with either 2-wire or 3-wire RTDs. The connections shown in Figure 1 are for 3-wire RTD operation. A dc power supply and a series load resistor to monitor the 4-20mA output signal may be located remotely from the transmitter and connected by a simple twisted pair of copper wires.

The transmitter contains individual ZERO and SPAN adjustments which are readily accessible to permit ease of field calibration.

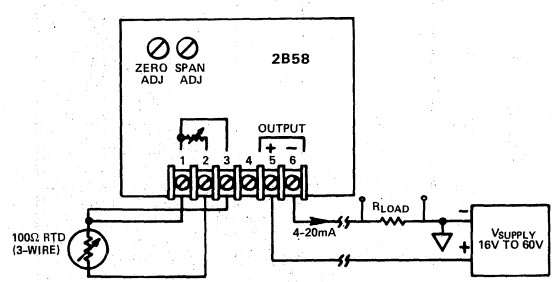


Figure 1. Model 2B58 Basic Application

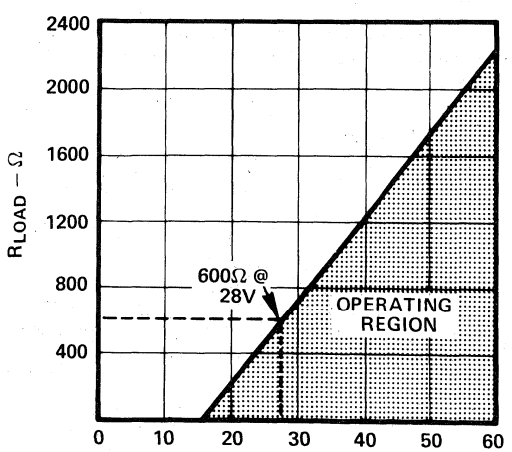
For detailed information, contact factory.

SPECIFICATIONS (typical @ +25°C and V_S = +24V dc unless otherwise noted)

Model	2B58A
INPUT SPECIFICATIONS	
Sensor Type	Platinum, 100Ω @ 0°C, α = 0.00385 2 or 3 Wire
Normal Mode Rejection	56dB @ 60Hz
Sensor Excitation Current	0.5mA
Zero and Span Adjustment Range	±5% of Span
OUTPUT SPECIFICATIONS	
Output Span	4-20mA
Minimum Output Current	3.5mA, typ
Maximum Output Current	40mA, typ
Load Resistance Range Equation	R_L max = (+V_S -16V)/20mA
@ +24V Supply	0 to 400Ω
Output Protection[1]	±60V
ACCURACY	
Total Output Error[2]	±0.1%
Stability vs. Ambient Temperature	
Zero, Measurement Range 01 through 03[3]	±0.01°C/°C max (±0.005°C/°C typ)
Measurement Range 04[3]	±0.01°C/°C
Span	±0.005%/°C
Stability vs. Time[2]	±50ppm/Month
Lead Resistance Effect, to 40Ω per Lead	
Span Error	±0.5%
Warm-Up Time to Rated Performance	3 Minutes
RESPONSE TIME	
To 90% of Span	0.4 sec
POWER SUPPLY	
Voltage, Operating Range	+16V to +60V dc
Supply Change Effect, % of Span	
on Zero	±0.005%/V
on Span	±0.01%/V
ENVIRONMENTAL	
Temperature Range, Rated Performance	-30°C to +85°C
Storage Temperature Range	-55°C to +125°C
Humidity Effect[4]	
Error	±0.6% of Span
RFI Effect (5W @ 470MHz @ 3 ft.)	
Error	±0.5% of Span
PHYSICAL	
Case Size	4" X 3.25" X 1.25"
Weight	8 oz (227 g)

NOTES
[1] Protected for reverse polarity and for any input/output connection combination.
[2] Accuracy is specified as a percent of output span (16mA). Accuracy spec includes combined effects of transmitter repeatability, hysteresis and sensor linearization conformity. Does not include sensor error.
[3] See ordering information for measurement temperature ranges 01 through 04.
[4] Per MIL-STD-202E Method 103B.

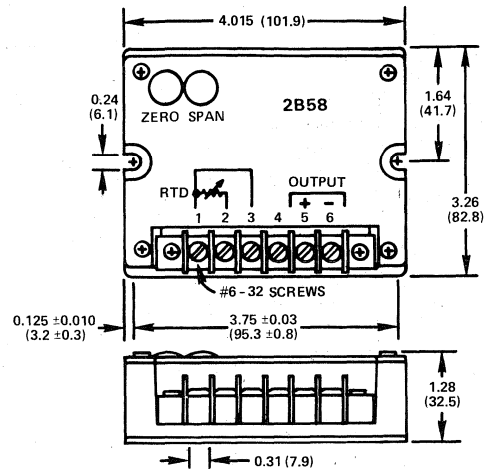
Specifications subject to change without notice.



R_{LOAD} vs. V_{SUPPLY}

OUTLINE DIMENSIONS (MAX)

Dimensions shown in inches and (mm).



ORDERING INFORMATION

Example: Model 2B58A - 1 - 1 - 01

Enter Model
2B58A

Enter Housing
1-Standard Enclosure

Enter Sensor Type
1-100Ω Platinum, α = 0.00385

Enter Temperature Range
01 Through 04

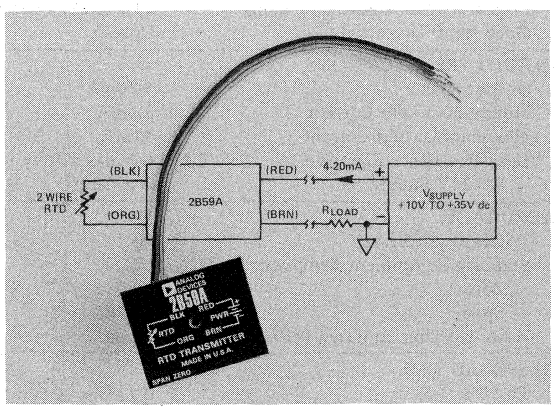
Range in °C (°F)	No.
-100 to +100 (-148 to +212)	01
0 to +100 (+32 to +212)	02
0 to +200 (+32 to +392)	03
0 to +400 (+32 to +752)	04

Low Cost, Two-Wire RTD Temperature Transmitter

MODEL 2B59

FEATURES
Low Cost
Standard RTD Input
Output Compatible with 4-20mA Loops
High Accuracy: ±0.1%
Small Size
Ease of Installation

APPLICATIONS
Temperature Monitoring and Transmission
Energy Management Systems



9

GENERAL DESCRIPTION

The model 2B59 is a low cost temperature transmitter designed to accept an RTD sensor input and produce a 4-20mA output proportional to the measured temperature. The 2B59 is a true two-wire transmitter, with the same wiring used for power and output. The load resistance is connected in series with a dc power supply ($+V_S$) and the current drawn from the supply is the 4-20mA output signal.

The transmitter features high calibration accuracy of ±0.1%. Several factory-calibrated temperature measurement ranges are available for standard platinum and nickel-iron RTD sensors. Both zero and span user-accessible screwdriver adjustments are provided for fine calibration after installation, if needed.

The 2B59 is packaged in a small (1.2″ X 1.5″ X 0.5″), rugged, epoxy encapsulated module and may be easily mounted by using a single screw. Connections to the transmitter are made via four color-coded leads using standard wire nuts.

APPLICATIONS

The 2B59 has been specifically designed to provide low cost, small size, ease of installation, and reliability in multipoint temperature monitoring applications.

In energy management and control systems, the 2B59 may be mounted in standard 2″ X 4″ utility or thermostat boxes in conjunction with a sensor and used for duct or room temperature sensing and transmission.

CALIBRATION

The 2B59 is factory calibrated to provide zero and span accuracy of ±0.1% of span. Should field calibration of the 2B59 to the specified range be desired, the following procedure is recommended:

1. Connect the transmitter as shown in Figure 2. Substitute a resistance standard for the RTD and use a load resistor for the appropriate power supply voltage, as specified by the graph of R_{LOAD} max vs. V_{SUPPLY} (Figure 1).
2. Determine minimum and maximum resistance values of sensor being used from standard resistance/temperature tables. (For example, for a 100 Pt sensor, a measurement range of 0 to +100°C corresponds to the resistance range of 100.0Ω to 138.50Ω.)
3. Connect required minimum input resistance standard. Adjust ZERO potentiometer, if necessary, to obtain an output of 4 ±0.016mA.
4. Connect required maximum input resistance standard. Adjust SPAN potentiometer, if necessary, to obtain an output of 20 ±0.016mA.
5. Repeat steps 3 and 4 until readings converge.

An alternate method of calibration utilizing an RTD sensor would be to adjust the ZERO and SPAN potentiometers while alternatively maintaining the probe at the specified minimum and maximum measured temperatures. A precision thermometer, located at the temperature probe, should be used to provide an accurate point of reference.

SPECIFICATIONS (typical @ +25°C and V_S = +24V unless otherwise noted)

MODEL	2B59A
INPUT SPECIFICATIONS	
Sensor Type	
Platinum	100Ω @0C, α = 0.00385
Nickel-Iron	1000Ω, 2000Ω @ +21.1°C (+70°F)
	α = 0.00527
Zero and Span Adjustment Range	±3% of Span min
Open Input Detection	Upscale
OUTPUT SPECIFICATIONS	
Output Span	4-20mA
Minimum Output Current	3.4mA
Maximum Output Current	35mA
Load Resistance Equation	R_L max = (+V_S - 10V)/20mA
@ +24V Supply	0 to 700Ω
ACCURACY	
Total Output Error[1]	±0.1%
Stability vs. Ambient Temperature	
Zero	±0.015%/°C
Span	±0.005%/°C
Warm-Up Time to Rated Performance	1 min
RESPONSE TIME	
To 90% of Span	0.125ms
POWER SUPPLY	
Voltage, Operating Range[2]	+10V to +35V dc
Supply Change Effect, % of Span	±0.001%/V
ENVIRONMENTAL	
Temperature Range, Rated Performance	-25°C to +85°C
Storage Temperature Range	-55°C to +125°C
Humidity Effect	
Error, 90% RH @ +40°C	±0.2% of Span
PHYSICAL	
Case Size	1.2" X 1.5" X 0.5"

[1] Accuracy is specified as a percent of output span (16mA). Accuracy spec includes combined effects of transmitter linearity, repeatability and hysteresis. Does not include sensor error.
[2] Protected for reverse polarity.

Specifications subject to change without notice.

ORDERING INFORMATION

MODEL 2B59A - 0 - 1 - 01

ENTER MODEL
2B59A

ENTER ENCLOSURE
0 - MODULE

ENTER SENSOR TYPE
1- 100Ω Pt, α = 0.00385
2- 1000Ω NiFe, α = 0.00527
3- 2000Ω NiFe, α = 0.00527

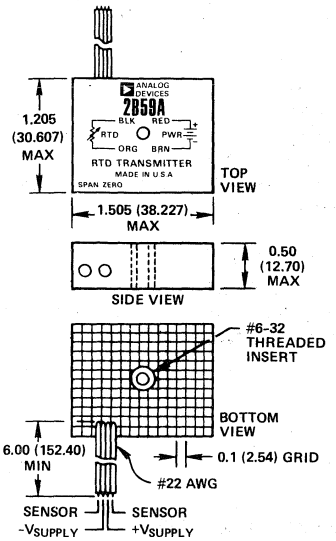
ENTER TEMPERATURE RANGE
01 through 06 → AVAILABLE TEMPERATURE RANGES IN °F (°C)

01	0 to +100 (-18 to +38) – Sensors 1 and 2
02	+20 to +120 (-7 to +49) – Sensors 1, 2 and 3
03	+50 to +150 (+10 to +66) – Sensors 1 and 2
04	+32 to +212 (0 to +100) – Sensors 1, 2 and 3
05	-30 to +130 (-34 to +54) – Sensor 3
06	+200 to +400 (+93 to +204) – Sensor 3

(Consult factory for additional ranges.)

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



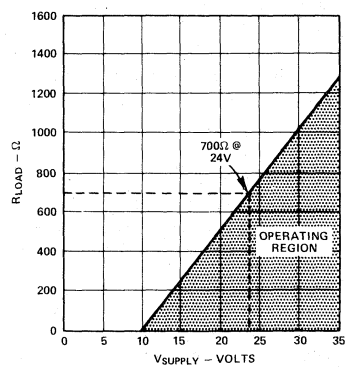


Figure 1. R_{LOAD} vs. V_{SUPPLY}

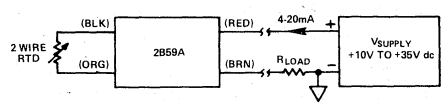


Figure 2. Basic Application

Digital-to-Analog Converters

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ISO-DAC is a trademark of Analog Devices, Inc.

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Selection Guide
Digital-to-Analog Converters

GENERAL PURPOSE DACs FEATURE SELECTION CHARTS

		GENERAL PURPOSE						FAST	
		AD1408	AD DAC80-1	AD DAC80-V	AD DAC85-1	AD DAC85-V	AD DAC-08	AD561	AD DAC100
Resolution	8 Bits	•					•		
	10 Bits							•	•
	12 Bits		•	•	•	•			
Accuracy	8 Bits	•					•		
	10 Bits							•	•
	12 Bits		•	•	•	•			
Output Format	Current	•	•		•		•	•	•
	Voltage			•		•			
Internal Reference			•	•	•	•			
Multiplication Capability	2 Quadrant	•					•	•	•
	4 Quadrant								
Logic Compatible with	TTL	•	•	•	•	•	•	•	•
	CMOS	•					•	•	
Input Coding	Binary	•	•	•	•	•	•	•	•
	BCD		•	•	•	•			
Second Source		•	•	•	•	•	•		•
Single Power Supply									
Input Data Latch Structure	Serial								
	Parallel								
Operating Temperature Ranges[1]	C = 0 to +70°C	•	•	•	•	•	•	•	•
	I = −25°C to +85°C				•	•			
	M = −55°C to +125°C	•			•	•	•	•	•
Low Power									
Dice Availability							•	•	
Volume I Page		10-71	10-215	10-215	10-223	10-223	10-205	10-25	10-235

[1] C = Commercial I = Industrial M = Military

		μP BUS COMPATIBLE			MULTIPLYING							SPECIAL PURPOSE	
		AD558	AD7524	AD7522	AD7523	AD7530	AD7520	AD7533	AD7521	AD7531	AD7541	AD7541A	AD7537 SYSTEMS DAC	AD7538 DUAL DAC
Resolution	8 Bits	•	•		•									•
	10 Bits			•		•	•	•	•	•			•	
	12 Bits										•	•		
Accuracy	8 Bits	•	•	•	•	•	•	•	•	•				•
	10 Bits		•	•	•	•	•	•	•	•			•	
	12 Bits										•	•		
Output Format	Current		•	•	•	•	•	•	•	•	•	•	•	•
	Voltage	•												
Internal Reference		•												
Multiplication Capability	2 Quadrant		•	•	•	•	•	•	•	•	•	•	•	•
	4 Quadrant		•	•	•	•	•	•	•	•	•	•	•	•
Logic Compatible with	TTL	•	•	•		•	•	•	•	•	•			•
	CMOS	•	•	•	•	•	•	•	•	•	•	•	•	•
Input Coding	Binary	•	•	•	•	•	•	•	•	•	•	•	•	•
	BCD													
Second Source			•	•	•	•	•	•	•	•	•	•		
Single Power Supply		•												
Input Data Latch Structure	Serial			•										
	Parallel	•	•	•									•	•
Operating Temperature Ranges[1]	C = 0 to +70°C	•	•	•	•	•	•	•	•	•	•	•	•	•
	I = −25°C to +85°C		•	•	•	•	•	•	•	•	•	•	•	•
	M = −55°C to +125°C	•	•	•	•	•		•	•		•	•	•	•
Low Power		•	•	•	•	•	•	•	•	•	•	•	•	•
Dice Availability		•	•	•	•	•		•	•		•			
Volume I Page		10-17	10-115	10-105	10-111	10-97	10-147	10-151	10-97	10-147	10-157	10-163	10-127	10-139

[1] C = Commercial I = Industrial M = Military

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HIGH PERFORMANCE DACs
FEATURE SELECTION CHARTS

		HIGH PERFORMANCE									μP COMPATIBLE	FAST					MULTIPLYING
		AD563	AD DAC87	AD370	AD371	AD DAC71/ DAC72	AD7546	DAC1136	DAC1138	AD5860	AD567	AD565	AD565A	DAC1108	AD566	AD566A	MDM5
Resolution	0.375dB Steps to 88.5dB																
	1.5dB Steps to 88.5dB																
	8 Bits																●
	10 Bits																●
	12 Bits	●	●	●	●					●	●	●	●	●	●	●	
	16 Bits					●	●	●									
	18 Bits								●								
Output	Current	●	●					●	●		●	●	●	●	●	●	●
Format	Voltage		●	●	●	●	●	●	●	●							
Internal Reference		●	●	●	●	●		●	●	●	●	●	●	●			
Multiplication	2 Quadrant						●								●	●	●
Capability	4 Quadrant																
Logic	TTL	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
Compatible with	CMOS	●	●	●	●	●	●										
Input Code	Binary	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
	BCD	●	●														
Second Source		●	●	●	●	●				●		●	●		●	●	
Single Power Supply																	
Input Data	Serial																
Latch Structure	Parallel						●			●	●						
Operating	C = 0 to +70°C	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
Temperature	I = -25°C to +85°C					●	●										●
Ranges[1]	M = -55°C to +125°C	●	●	●	●					●	●	●	●		●	●	
Low Power				●	●		●										
Input/Output Isolation																	
Dice Availability											●		●			●	
Volume I																	
Page		10-33	10-231	10-11	10-11	10-211	10-197	10-243	10-243	10-75	10-63	10-39	10-43	–	10-51	10-55	10-275
Volume II																	
Page		–	–	–	–	–	–	10-15	10-15	–	–	–	–	10-11	–	–	10-37

[1] C = Commercial I = Industrial M = Military

		HIGH PERFORMANCE										SPECIAL PURPOSE				
		MULTIPLYING				μP BUS COMPATIBLE				ATTENUATION			PROCESS CONTROL 4 TO 20mA OUT μP BUS COMPATIBLE			QUAD DAC
		AD562	AD7541	AD7541A	AD7525	AD7542	AD7543	AD7541	AD7545	AD7110	AD7118	AD7111	DAC1420	DAC1422	DAC1423	AD390
Resolution	0.375dB Steps to 88.5dB															
	1.5dB Steps to 88.5dB									●	●	●				
	8 Bits												●	●		
	10 Bits				●											
	12 Bits	●	●	●		●	●	●	●							●
	16 Bits															
	18 Bits															
Output	Current	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
Format	Voltage															●
Internal Reference													●	●	●	●
Multiplication	2 Quadrant	●	●	●	●	●	●	●	●	●	●	●				●
Capability	4 Quadrant		●	●	●	●	●	●	●							
Logic	TTL	●	●	●					●			●	●	●	●	●
Compatible with	CMOS	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
Input Code	Binary	●	●	●		●	●	●	●	●	●	●				●
	BCD	●			●											
Second Source		●	●	●												
Single Power Supply													●	●	●	
Input Data	Serial						●									
Latch Structure	Parallel					●		●	●			●				●
Operating	C = 0 to +70°C	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
Temperature	I = -25°C to +85°C		●	●	●	●	●	●	●		●	●				
Ranges[2]	M = -55°C to +125°C	●	●	●	●	●	●	●	●		●	●				●
Low Power			●	●	●	●	●	●	●	●	●	●				
Input/Output Isolation															●	
Dice Availablity			●			●	●									
Volume I																
Page		10-33	10-157	10-163	10-121	10-165	10-173	10-181	10-189	10-79	10-91	10-85	10-245	10-245	10-247	10-15
Volume II																
Page		–	–	–	–	–	–	–	–	–	–	–	10-23	10-23	10-27	–

[1] Six-Stage FIFO Input Register [2] C = Commercial I = Industrial M = Military

ULTRA FAST/VIDEO DACs
FEATURE SELECTION CHARTS

		CURRENT OUT												
		HDG-0405	HDG-0605	HDG-0805	MDS-0815	MDS-1020	MDS-1240	HDS-0820	HDS-0810E	HDD-0810	HDD-0810C	HDS-1025	HDS-1015E	HDD-1015
Settling Time to Resolution in Bits	<550ns <210ns <75ns											•		
	<21ns <8ns	•	•	•	•	•	•	•	•	•	•		•	•
Resolution	4 Bits 6 Bits 8 Bits	•	•	•	•			•	•	•	•			
	10 Bits 11 Bits 12 Bits					•	•					•	•	•
Application	General Purpose Lowest Glitch	•	•	•	•	•	•	•	•	•	•	•	•	•
	Multiplying Composite Video	•	•	•							•			
Output Format	Current Voltage	•	•	•	•	•	•	•	•	•	•	•	•	•
Binary Logic	TTL ECL Latched	• •	• •	• •	•	•	•	•	• •	• •	• •	•	• •	• •
Single Power Supply		•	•	•					•	•	•		•	•
Operating Temperature Ranges	0 to +70°C -25°C to +85°C -55°C to +125°C	•	•	•	•	•	•	• •	• •	• •	• •	• •	• •	• •
Volume I Page		10-259	10-259	10-259	–	–	–	10-265	10-269	10-249	10-249	10-265	10-269	10-249
Volume II Page		–	–	–	10-39	10-39	10-39	–	–	–	–	–	–	–

		CURRENT OUT							VOLTAGE OUT			
		HDD-1015C	HDS-1250	HDS-1240E	DAC1106	MDMS-0801	MDMS-1001	MDMS-1101	HDH-0802	HDH-1003	HDH-1205	MDD-0820	MDD-1020
Settling Time to Resolution in Bits	<550ns <210ns <75ns		•	•	•	•	•	•	•	•	•	•	•
	<21ns <8ns	•											
Resolution	4 Bits 6 Bits 8 Bits				•	•			•			•	
	10 Bits 11 Bits 12 Bits	•	•	•	•		•	•	•	•	•		•
Application	General Purpose Lowest Glitch		•	•	•				•	•	•	•	•
	Multiplying Composite Video	•				•	•	•					
Output Format	Current Voltage	•	•	•	•	•	•	•	•	•	•	• •	• •
Binary Logic	TTL ECL Latched	• •	•	•	•	•	•	•	•	•	•	•	•
Single Power Supply		•											
Operating Temperature Ranges	0 to +70°C -25°C to +85°C -55°C to +125°C	• •	•	• •[1]	•	•	•	•	• •	• •	•	•	•
Volume I Page		10-249	10-265	10-271	–	10-275	10-275	10-275	10-265	10-265	10-265	–	–
Volume II Page		–	–	–	10-11	10-37	10-37	10-37	–	–	–	10-33	10-33

[1] -55°C to +100°C

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Orientation
Digital-to-Analog Converters

FACTORS IN CHOOSING A D/A CONVERTER

In the current issue of this two-volume catalog, there are listed some 56 different families of digital-to-analog converters (DACs). If one were to consider all the variations, there would be more than 224 types to choose among. The reason for so many different types is the number of degrees of freedom in selection—technological, functional, and performance. Complete information on converters may be found in the 250-page book, ANALOG-DIGITAL CONVERSION NOTES, published by Analog Devices and available for $5.95 from P.O. Box 796, Norwood MA 02062.

TECHNOLOGICAL FACTORS

The technologies represented in these two volumes include modules (cards and potted circuits) and integrated circuits—monolithic and hybrid. Modules historically have provided the extremes of performance and arbitrary levels of functional completeness (e.g., the 18-bit DAC1138, the 10-bit 20MHz-word-rate deglitched MDD-1020, and the isolated 10-bit DAC1423 loop DAC), although ICs are catching up rapidly.

The technical data in this volume embrace exceptionally high performance (high-resolution and high-speed) d/a converters, in the form of encapsulated modules. As the Selection Guide indicates, there is also a universe of technical data, to be found in Volume I, on a wide range of monolithic and hybrid d/a converters, including microprocessor-compatible types with resolutions through 16 bits, devices screened to the requirements of MIL-STD-883B, and chips for hybrid assembly.

FUNCTIONAL CHARACTERISTICS

The basic structure of all conventional D/A converters involves a network of precision resistors, a set of switches, and some form of level-shifting to adapt the switch drives to the specified logic levels. In addition, the device may contain output-conditioning circuitry, an output amplifier, a reference amplifier, an on-board reference, on-board buffer-registers (single- or dual-rank), configuration conditioning, and even high-voltage isolation.

Basic DAC

This form, which supplies a current, and consequently a small voltage across its internal impedance or an external low-impedance load, is used principally for high speed. Basic current-output DACs are inherently fast, but additional elements (such as an output op amp), furnished by the user to meet overall system specs, slow down the conversion.

While the basic DAC function is almost always linear, there are exceptions. For example, the AD7110 audio attenuator, which has linear two-quadrant analog response, has a digitally controlled exponential gain function, i.e., 1.5dB per bit, a useful function in digital audio systems.

Output Conditioning

The analog quantity that is the "output" of a DAC, representing the input digital data, may be a "gain" (multiplying DAC), a current, and/or a voltage. In order to obtain a substantial voltage output at low impedance, an op amp is required. It is generally provided on-board in modular and hybrid DACs.

Almost all types of DACs provide one or more feedback resistors; they are matched to, and thermally track, resistances in the network, so that an external op amp, if used, will not require an external feedback resistor that might introduce tracking errors. If more than one feedback resistor is provided, a choice of analog output voltage ranges becomes available, e.g., 0–5V full-scale or 0–10V full-scale. If bipolar output-voltage ranges are specified, a bipolar-offset output is provided to subtract a half-scale value from the current flowing through the op amp summing point; it is usually derived from the DAC's reference (or analog) input to avoid additional tracking error. Multiplying DACs use an internal or external op amp for bipolar offset.

In addition to the usual zero-based current and voltage outputs, DACs are available with 4-to-20mA ISA-standard loop-current outputs, both direct-coupled (DAC1420/22) and high-voltage-isolated (DAC1423), with some additional features that are specifically useful in digital control of analog processes.

In order to avoid difficulties, the user must pay especial attention to the specified output polarity, its relationship to the reference (if external) and to the input digital code. This can be especially tricky if the output is bipolar and the input requires a complementary (negative-true) digital coding. Another such case is where a current-output DAC, specified for a particular output-voltage polarity when used with an inverting op amp, is used in a mode that develops an output voltage passively (without the op amp) across an external resistive load. In addition to polarity, in this case, the user should be aware of the output-compliance constraint and the specified resistive component of output impedance.

Reference Input

The reference may be specified as external or internal, fixed or variable, single-polarity or bipolar. If internal, it may be permanently connected (as in the DAC1106/1108) or optionally connectible (as in the DAC1136/1138). If the DAC is a 4-quadrant multiplying type, the reference (or "analog input") is external, variable, and bipolar. The user should check a converter's specifications to determine whether the full-scale accuracy specifications are overall or subdivided into a converter-gain spec and a reference spec.

Digital Data

There are a number of ways in which converters differ in regard to the input data: First, the *coding* must be appropriate (binary, offset-binary, two's-complement, BCD, arbitrary, etc.), and its sense should be understood (positive-true, negative-true). The *resolution* (number of bits) must be sufficient; in addition, the specifications must be checked to ascertain that the 2^n distinct binary input codes will not only be accepted, but that also they will (if necessary) correspond to 2^n output values in a monotonic progression at any temperature in the operating range, with sufficient accuracy.

The *data levels* accepted by the converter must be checked (TTL, ECL, low-voltage CMOS, high voltage CMOS), as must the input loading imposed by the converter, and the supply conditions under which the converter will respond to the data. Check the data notation (is the MSB Bit 1 or Bit (n–1)?)—misinterpretation can lead to connecting the data bits in backward order. If *buffer registers* are desired, the converter should have an appropriate buffer configuration. The data can be clocked in, while the DAC output remains unchanged.

Controls
If the DAC has external digital controls—for example, register strobes– their drive levels, digital sense (true or false), loading, and timing must be considered. The function and use of configuration controls (where present), such as serial/parallel, short-cycle, or chip-select decoding should be understood, and the appropriate ways of disabling them when not needed should be employed.

Power Supplies
Appropriate power supplies should be made available, considering the logic levels and analog output signals to be employed in the system. The appropriate degree of power-supply stability to meet the accuracy specs should be employed. Any recommended external protection circuitry (e.g., Schottky diodes, to ensure that V_{CC} is never more than 0.4V above V_{DD} in the AD7522) should be planned for. In many cases separate analog and digital grounds are required; ground wiring should follow best practice to minimize digital interference with high-accuracy analog signals, while ensuring that a connection between the grounds can always exist at one point, even if the "mecca" point is inadvertently unplugged from the system.

For video converters, use massive, low impedance ground systems. The analog and digital grounds are connected together inside converters of these types, so bus bars are essential for system grounding and power distribution; use lots of ground plane on PC boards.

SPECIFICATIONS AND TERMS
Definitions of the performance specifications, and related information, are provided on the next few pages, in alphabetical order.

Accuracy, Absolute
Error of a D/A converter is the difference between the actual analog output and the output that is expected when a given digital code is applied to the converter. Sources of error include gain (calibration) error, zero error, linearity errors, and noise. Error is usually commensurate with resolution, i.e., less than $2^{-(n+1)}$, or "½ LSB" of full scale. However, accuracy may be much better than resolution in some applications; for example, a 4-bit reference supply having only 16 discrete digitally chosen levels would have a resolution of 1/16, but it might have an accuracy to within 0.01% of each ideal value.

Absolute-accuracy measurements should be made under a set of standard conditions with sources and meters traceable to an internationally accepted standard.

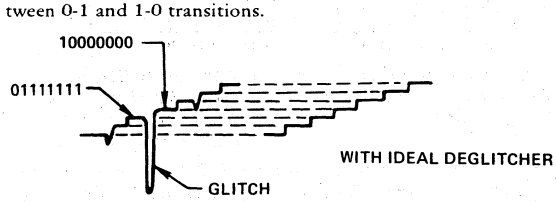
Accuracy, Relative
Relative accuracy error, expressed in %, ppm, or fractions of 1 LSB, is the deviation of the analog value at any code (relative to the full analog range of the device transfer characteristics) from its theoretical value (relative to the same range), after the full-scale range (FSR) has been calibrated. Since the discrete analog output values corresponding to the digital input values ideally lie on a straight line, the relative-accuracy error of a linear DAC can be interpreted as a measure of nonlinearity (see *Linearity*).

Compliance-Voltage Range
For a current-output DAC, the maximum range of (output) terminal voltage for which the device will provide the specified current-output characteristics.

Common-Mode Rejection (CMR)
The ability of an amplifier to reject the effect of voltage applied to both input terminals simultaneously. Usually a logarithmic expression representing a "common-mode rejection ratio" e.g., 1,000,000:1 (CMRR) or 120dB (CMR). A CMRR of 10^6:1 means that a 1V common-mode voltage passes through the device as though it were a differential input signal of 1 microvolt.

Common-Mode Voltage
An undesirable signal picked up in a circuit by both wires making up the circuit, with reference to an arbitrary "ground." Amplifiers differ in their ability to amplify a desired signal accurately in the presence of a common-mode voltage.

Deglitcher
As the input code to a DAC is increased or decreased by small changes, it passes through what is known as major and minor transitions. The most major transition is at half-scale, when the DAC switches around the MSB, and all switches change state, i.e., 01111111 to 10000000. If, at major transitions, the switches are faster (or slower) to switch off than on, this means that, for a short time, the D/A will give a zero (or full-scale) output, and then return to the required 1 LSB above the previous reading. Such large transient spikes which differ widely in amplitude and are extremely difficult to filter out, are commonly known as "glitches", hence, a deglitcher is a device which removes these glitches or reduces them to a set of small, uniform pulses. It normally consists of a fast sample-hold circuit, which holds the output constant until the switches reach equilibrium. Glitch energy is smallest in fast-switching DACs driven by fast logic gates that have little time-skew between 0-1 and 1-0 transitions.



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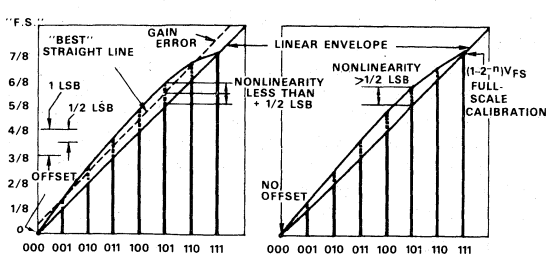
Feedthrough
Undesirable signal coupling around switches or other devices that are supposed to be turned off or provide isolation, e,g,. *feedthrough error* in a multiplying DAC. It is variously specified in %, ppm, fractions of 1 LSB, or fractions of 1 volt, with a given set of inputs, at a specified frequency.

Four-Quadrant
In a multiplying DAC, "four quadrant" refers to the fact that both the reference signal and the number represented by the digital input may be of either positive or negative polarity. A four-quadrant multiplier is expected to obey the rules of multiplication for algebraic sign.

Gain
The "gain" of a converter is that analog scale-factor setting that provides the nominal conversion relationship, e.g., 10V span for a full-scale code change, in a fixed-reference converter. For fixed-reference converters where the use of the internal reference is optional, the converter gain and the reference may be specified separately. Gain- and zero-adjustment are discussed under *Zero*.

Least-Significant Bit (LSB)
In a system in which a numerical magnitude is represented by a series of binary (i.e., two-valued) digits, the LSB is that bit that carries the smallest value, or weight. For example, in the natural-binary number 1101 (decimal 13, or $2^3 + 2^2 + 0 + 2^0$), the rightmost digit is the LSB. Its analog weight, relative to full scale, is 2^{-n}, where n is the number of binary digits. It represents the smallest analog change that can be resolved by an n-bit converter.

Linearity
Linearity error of a converter (also, *integral nonlinearity*, see *Linearity, Differential*), expressed in % or ppm of full-scale range, or (sub)multiples of 1 LSB, is a deviation of the analog values, in a plot of the measured conversion relationship, from a straight line. The straight line can be either a "best straight line", determined empirically by manipulation of the gain and/or offset to equalize maximum positive and negative deviations of the actual transfer characteristics from this straight line; or it can be a straight line passing through the end points of the transfer characteristic after they have been calibrated (sometimes referred to as "end-point" linearity). End-point linearity error is similar to *relative-accuracy* error.



a. ½LSB Nonlinearity Achieved By Arbitrary Location of "Best Straight Line".

b. Nonlinearity Reference is Straight Line Through End Points. Nonlinearity >½LSB for Curve of a.

Comparison of Linearity Criteria for 3-Bit D/A Converter. Straight Line Through End Points is Easier to Measure, Gives More-Conservative Specification.

For multiplying D/A converters, the *analog* linearity error, at a specified digital code, is defined in the same way as for multipliers, i.e., by deviation from a "best straight line" through the plot of the analog output-input response.

Linearity, Differential
Any two adjacent digital codes should result in measured output values that are exactly 1 LSB apart (2^{-n} of full scale for an n-bit converter). Any deviation of the measured "step" from the ideal difference is called *differential nonlinearity*, expressed in (sub)multiples of 1 LSB. It is an important specification, because a differential linearity error greater than 1 LSB can lead to non-monotonic response in a D/A converter and missed codes in an A/D converter (see *Differential Linearity* in the A/D converter section for an illustration).

Monotonic
A DAC is said to be monotonic if the output either increases or remains constant as the digital input increases, with the result that the output will always be a single-valued function of the input. The specification "monotonic" (over a given temperature range) is sometimes substituted for a *differential nonlinearity* specification, since differential nonlinearity less than 1 LSB is a sufficient condition for monotonic behavior.

Most-Significant Bit (MSB)
In a system in which a numerical magnitude is represented by a series of binary (i.e., two-valued) digits, the MSB is that digit (or bit) that carries the largest value of weight. For example, in the natural-binary number 1101 (decimal 13, or $2^3 + 2^2 + 0 + 2^0$), the leftmost "1" is the MSB, with a weight of 2^{n-1}, or 8 LSBs. Its analog weight, relative to a DAC's full-scale span, is ½. In bipolar DACs, the MSB indicates the polarity of the number represented by the rest of the bits.

Multiplying DAC
A multiplying DAC differs from a fixed-reference DAC in being designed to operate with varying (or ac) reference signals. The output signal of such a DAC is proportional to the product of the "reference" (i.e., analog input) voltage and the fractional equivalent of the digital input number (see also *four-quadrant*).

Noise, Peak and rms
Internally generated random noise is not a major factor in D/A converters, except at extreme resolutions (e.g., DAC1138) and dynamic ranges (AD7110). Random noise is characterized by rms specifications for a given bandwidth, or as a spectral density (current or voltage per root hertz); if the distribution is Gaussian, the probability of peak-to-peak values exceeding 7x the rms value is less than 0.1% (see the waveform table in Section 7).

Of much greater importance in DACs is interference in the form of high-amplitude low-energy (hence low-rms) spikes appearing at the DAC's output, caused by coupling of digital signals in a surprising variety of ways; they include coupling via stray capacitance, via power supplies, via inadequate ground systems, via feedthrough, and by glitch-generation. Their presence underscores the necessity for maximum application of the designer's art, including layout, shielding, guarding, grounding, bypassing, and deglitching.

Offset
For almost all bipolar converters (e.g., ±10-volt output), instead of actually generating negative currents to correspond to negative numbers, a unipolar DAC is used, and the output is offset by half full scale (1 MSB). For best results, this offset voltage or current is derived from the same reference supply that determines the gain of the converter.

This makes the zero point of the converter independent of thermal drift of the reference, because the ½ scale offset cancels the weight of the MSB at zero, independently of the amplitude of both.

Power-Supply Sensitivity
The sensitivity of a converter to changes in the power-supply voltages is normally expressed in terms of percent-of-full-scale change in analog output value (or fractions of 1 LSB) for a 1% dc change in the power supply, e.g., $0.05\%/\%\Delta V_S$). Power supply sensitivity may also be expressed in relation to a specified dc shift of supply voltage. A converter may be considered "good" if the change in reading at full scale does not exceed ±½ LSB for a 3% change in power supply. Even better specs are necessary for converters designed for battery operation.

Quantizing Uncertainty (or "Error")
The analog continuum is partitioned into 2^n discrete ranges for n-bit processing. All analog values within a given range of output (of a DAC) are represented by the same digital code, usually assigned to the nominal midrange value. For applications in which an analog continuum is to be restored, there is an inherent quantization uncertainty of ±½ LSB, due to limited resolution, in addition to the actual conversion errors. For applications in which discrete output levels are desired (e.g., digitally controlled power supplies or digitally controlled gains), this consideration is not relevant.

Resolution
An n-bit binary converter should be able to provide 2^n distinct and different analog output values corresponding to the set of n-bit binary words. A converter that satisfies this criterion is said to have a *resolution* of n bits. The smallest output change that can be resolved by a linear DAC is 2^{-n} of the full-scale span. However, a nonlinear device, such as the AD7110 audio attenuator has a logarithmic gain resolution of 1.5/ 88.5dB = 1:59dB, which corresponds to a gain increment of 18.9%/step, or 26,600:1.

Settling Time
The time required, following a prescribed data change, for the output of a DAC to reach and remain within a given fraction (usually ±½ LSB) of the final value. Typical prescribed changes are full-scale, 1 MSB, and 1 LSB at a major carry. Settling time of current-output DACs is quite fast. The major share of settling time of a voltage-output DAC is usually contributed by the settling time of the output op-amp circuit.

Slew Rate (or Slewing Rate)
Slew rate of a device or circuit is a limitation in the rate of change of output voltage, usually imposed by some basic circuit consideration, such as limited current to charge a capacitor. Amplifiers with slew rate of a few V/μs are common, and moderate in cost. Slew rates greater than about 75 volts/μs are usually seen only in more sophisticated (and expensive) devices. The output slewing speed of a voltage-output D/A converter is usually limited by the slew rate of the amplifier used at its output (if one is used).

Stability
Stability of a converter usually applies to the insensitivity of its characteristics to time, temperature, etc. All measurements of stability are difficult and time consuming, but stability vs. temperature is sufficiently critical in most applications to warrant universal inclusion of temperature coefficients in tables of specifications (see "Temperature Coefficient").

Staircase
A voltage or current, increasing in equal increments as a function of time and having the appearance of a staircase (in a time plot), generated by applying a pulse train to a counter, and the output of the counter to the input of a DAC.

A very simple A/D converter can be built by comparing a staircase from a DAC with the unknown analog input. When the DAC output exceeds the analog input by a fraction of 1 LSB, the count is stopped, and the code corresponding to the count is the digital output.

Switching Time
In a DAC, the switching time is the time it takes for the switch to change from one state to the other ("delay time" plus "rise time" from 10%-90%), but does not include settling time, e.g. to <½ LSB.

Temperature Coefficients
In general, temperature instabilities are expressed as %/°C, ppm/°C, as fractions of 1 LSB/°C, or as a change in a parameter over a specified temperature range. Measurements are usually made at room temperature and at the extremes of the specified range, and the temperature coefficient (tempco, T.C.) is defined as the change in the parameter, divided by the corresponding temperature change. Parameters of interest include *gain, linearity, offset* (bipolar), and *zero*.

Gain Tempco: Two factors principally affect converter gain stability with temperature.

a) In fixed-reference converters the reference source will vary with temperature. For example, the tempco of an AD581L is generally less than 5ppm/°C.

b) The reference circuitry and switches may add another 3ppm/°C in good 12-bit converters (e.g. AD566K/T).

High-resolution converters require much better tempcos for accuracy commensurate with the resolution.

Linearity Tempco: Sensitivity of linearity ("integral" and/or differential linearity) to temperature (in % FSR/°C or ppm FSR/°C) over the specified range. Monotonic behavior is achieved if the differential nonlinearity is less than 1 LSB at any temperature in the range of interest. The *differential nonlinearity temperature coefficient* may be expressed as a ratio, as a maximum change over a temperature range, and/or implied by a statement that the device is monotonic over the specified temperature range.

Offset Tempco: The temperature coefficient of the all-DAC-switches-off (minus full scale) point of a bipolar converter (in % FSR/°C or ppm FSR/°C) depends on three major factors:

a) The tempco of the reference source
b) The voltage zero-stability of the output amplifier
c) The tracking capability of the bipolar-offset resistors and the gain resistors

Unipolar Zero Tempco (in % FSR/°C or ppm FSR/°C): The temperature stability of a unipolar fixed-reference DAC is principally affected by current leakage (current-output DAC), and offset voltage and bias current of the output op-amp (voltage-output DAC).

Zero- and Gain-Adjustment Principles

The output of a unipolar DAC is set to zero volts in the all-bits-off condition. The gain is set for F.S. $(1 - 2^{-n})$ with all bits on. The "zero" of an offset-binary bipolar DAC is set to -F.S. with all bits off, and the gain is set for +F.S. $(1 - 2^{-(n-1)})$ with all bits on. The data sheet instructions should be followed.

ANALOG DEVICES

High Speed Digital to Analog Converters

DAC1106/DAC1108

FEATURES
High Speed
8 Bits in 25ns
10 Bits in 50ns
12 Bits in 60ns
Adjustment Free Operation
Gain TC: ±10ppm/°C
Linearity Error: ±½LSB max
Small Size: 2" x 2" x 0.4" Module



GENERAL DESCRIPTION

The DAC1108 is a high speed, current output digital-to-analog converter with 12-bit resolution and accuracy. The very fast settling times to 0.05% accuracy of 60ns and to 0.01% accuracy of 150ns make it ideal for use in high speed applications such as computer driven displays, automatic test equipment, and function generators. In addition to the ±½LSB maximum linearity error, the DAC1108 features temperature coefficients of 30ppm/°C for gain and 8ppm/°C for linearity.

The DAC1106 is also a high speed, current output digital-to-analog converter which is available in both 8- and 10-bit versions. The very fast settling times to ½LSB or 25ns (8-bit models) and 50ns (10-bit models). Accuracy specifications include ±½LSB linearity, 10ppm/°C temperature coefficient, and 0.002%/V power supply rejection.

Everything needed to perform high speed conversions is contained in the compact 2" x 2" x 0.4" package of the DAC1106/1108. Included are a precision temperature compensated reference source, high speed current switches and a carefully trimmed network of weighting resistors. Because of the inherent stability and careful factory adjustment of this device, no external zero or gain adjustment potentiometers are required.

The digital inputs of the DAC1106/1108 are fully DTL/TTL compatible. Binary code is used for unipolar operation and Offset Binary code is used for bipolar operation. The current output of this device can be applied directly to an external resistor to develop a voltage output or it can be applied to the input of a fast settling op amp if amplification or impedance transformation is desired.

INPUT CONSIDERATIONS

The binary weighted current sources which form the basis of the digital to analog conversion process are directly switched by their associated input bits. A change in the converter's current output will begin to occur approximately 10nsec after a new digital word is applied. Because of this extremely fast response, time skew in the digital input can result in momentary erroneous outputs or "glitches". Consider, for example, the case of a transition from 1000 . . . 0 to 0111 . . . 1, a step of only one LSB. If the MSB turns to a "0" before the rest of the bits have turned to "1"s, the input will momentarily be 0000 . . . 0 and the converter will start to respond accordingly as shown below in Figure 1.

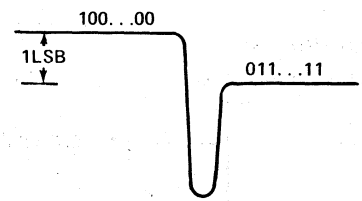


Figure 1. Switching Transient Caused by Time Skew

These switching transients will be minimized if the digital input data time skew is held to less than 5ns.

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SPECIFICATIONS (typical @ +25°C and rated supply voltages, unless otherwise noted)

MODELS	DAC1106	DAC1108
RESOLUTION	8/10 Bits	12 Bits
DIGITAL INPUTS	TTL Compatible	*
0V ≤ Logic "0" ≤ 0.8V	@ -3.2mA (max)	*
+2V ≤ Logic "1" ≤ 15V	@ 80μA (max)	*
INPUT CODES		
Unipolar	Binary	*
Bipolar	Offset Binary	*
OUTPUT RANGES	0 to +5mA	*
	-2.5 to +2.5mA	*
OUTPUT IMPEDANCE	600Ω ±1% (Unipolar)	510Ω ±2%
OUTPUT VOLTAGE COMPLIANCE	±1.2V	*[1]
ABSOLUTE ACCURACY		
Full Scale	±0.1%	*
Offset	±20nA	*
SETTLING TIME		
To 0.2%	25ns (30 max)	
To 0.1%	40ns (50 max)	
To 0.05%	50ns (60 max)	60ns
To 0.01%		150ns
LINEARITY ERROR	±½LSB max	*
TEMPERATURE COEFFICIENT		
Gain	±10ppm/°C	±30ppm/°C
Zero	±75μV/°C	*
Linearity	±8ppm/°C	*
TEMPERATURE RANGE		*
Operating	0 to +70°C	
Storage	-55°C to +85°C	-55°C to +125°C
POWER REQUIREMENTS		
+15V ±5%	47mA max	42mA max
-15V ±5%	37mA max	10mA max
POWER SUPPLY SENSITIVITY		
Gain	0.002%/V	0.01%/%ΔV
OUTLINE DIMENSIONS	2" x 2" x 0.4"	*

[1] ±1V for rated dynamic performance.
*Specifications same as DAC1106.

Specifications subject to change without notice.

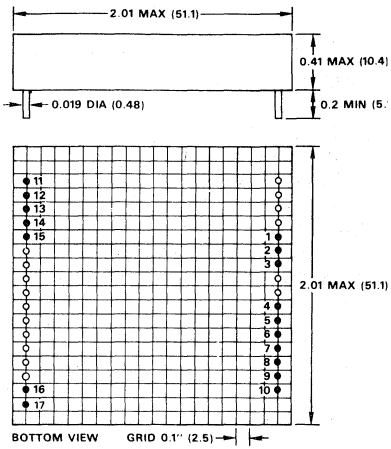
ORDERING GUIDE:

Model DAC1106/XXX

- 001 (EIGHT BIT)
- 002 (TEN BIT)

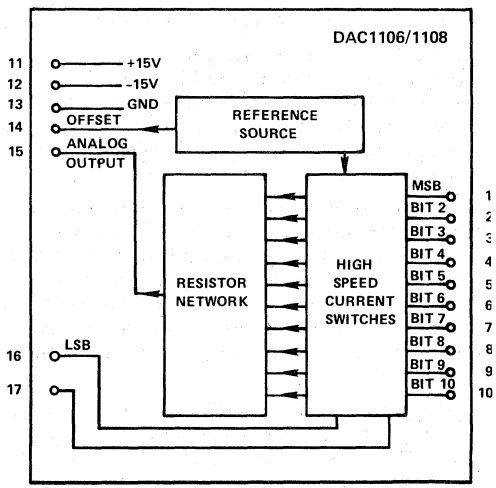
OUTLINE DIMENSIONS AND PIN DESIGNATIONS

Dimensions shown in inches and (mm).



NOTE:
Terminal pins installed only in shaded hole locations.
Module weight: 2 ounces (57 grams).
Pins 9 and 10 included on 10-bit models only.

BLOCK DIAGRAM AND PIN DESIGNATIONS



NOTE:
DAC1106 PIN 16 - N.C.
PIN 17 DELETED

DIGITAL INPUTS

The DAC1106/1108 is fully TTL/DTL compatible with each input bit representing two standard TTL Loads. The logic levels of

$0V \leqslant$ Logic "0" $\leqslant 0.8V$
$+2V \leqslant$ Logic "1" $\leqslant 15V$ (Absolute Max)

are also compatible with CMOS logic systems. When using this device in a CMOS system, standard CMOS/TTL interface rules must be observed to insure that the driving gate is capable of sinking at least 3.2mA.

The simple addition of an external inverter ahead of the MSB input terminal, as shown below in Figure 2, allows the bipolar Two's Complement code to be used.

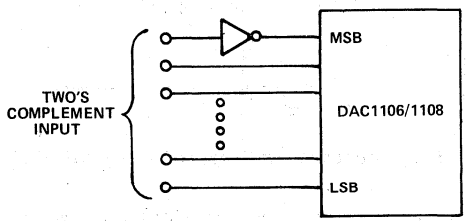


Figure 2. Two's Complement Input Connection

OUTPUT CHARACTERISTICS

The output of the DAC1106/1108 represents the sum of the currents produced by the individual binary-weighted current sources in response to the digital input word. This current varies from 0 to +5mA. In order to produce the half scale offset needed for bipolar outputs, a current of exactly -2.5mA must be added to the output. Such a current is generated internally and is available at pin 14. The analog outputs which are produced by various digital inputs are shown in the following tables.

UNIPOLAR

Digital Input	Analog Output		
	1106-001	1106-002	1108
111 111	+4.981mA	+4.995mA	+4.999mA
100 000	+2.500mA	*	*
000 001	+19.5μA	+4.88μA	+1.22μA
000 000	0mA	*	*

BIPOLAR

Digital Input	Analog Output		
	1106-001	1106-002	1108
111 111	+2.481mA	+2.495mA	+2.499mA
100 000	0mA	*	*
000 000	-2.500mA	*	*

Figures 3 and 4 illustrate the converter's output impedance characteristics for unipolar and bipolar operation.

*Specifications same as 1106-001.

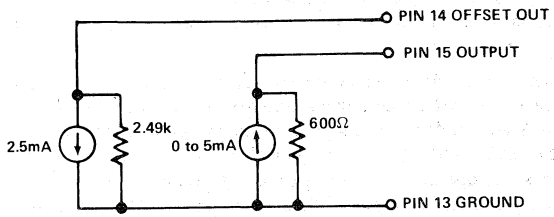


Figure 3. Equivalent Circuit DAC (Unipolar)

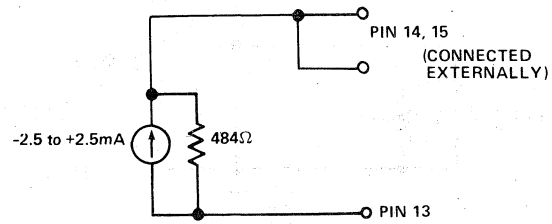


Figure 4. Equivalent Circuit DAC (Bipolar)

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OUTPUT CONNECTIONS

The circuits used to develop an output voltage across a resistor are shown below in Figures 5 and 6 for unipolar and bipolar operation.

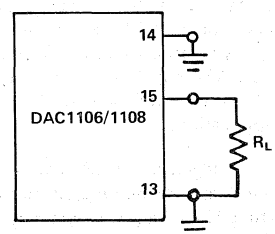


Figure 5. Voltage Output with Load Resistor (Unipolar)

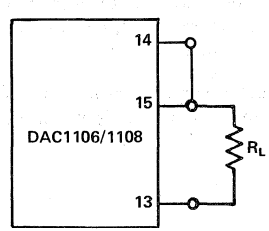


Figure 6. Voltage Output with Load Resistor (Bipolar)

In both cases, the output voltage is limited to ±1.2V max. By referring to Figures 3 and 4, the user can readily compute the value of R_L needed to produce the desired full scale voltage. For example, a 300Ω resistor will develop a 0 to +1V F.S. unipolar output and a 2.325kΩ resistor will develop a +1V F.S. bipolar output.

The DAC1106/1108 may be used in conjunction with a high speed external op amp when outputs greater than ±1.2V and 5mA are needed. Because current output converters such as the DAC1106/1108 are not ideal current sources, the op amp does not operate in a unity gain configuration. Figure 7 below shows, in simplified form, a unipolar DAC driving an op amp.

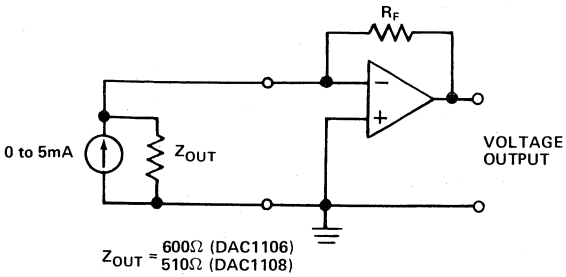


Figure 7. Voltage Output with an Op Amp Simplified Diagram

Because of the output impedance, the closed loop gain becomes $1 + R_F/Z_{OUT}$ instead of 1. For example with an R_F of 2kΩ the closed loop gain is 4.33 for DAC1106 and 4.92 for DAC1108.

This can complicate the job of selecting a suitable op amp since most manufacturers specify settling time at unity gain. One extremely fast op amp that performs well at gains of 2 to 6 is the Analog Devices' model 50 differential input, FET amplifier. The model 50 will settle to 10-bit accuracy (0.05%) in a maximum fo 200ns. The high current output of this device (100mA) also makes it ideal for use with the DAC1108 in CRT deflection applications.

Sometimes space or budgetary considerations dictate that an IC rather than a modular op amp be used. In these cases the AD509K fast settling IC op amp is recommended. The AD509K maintains its guaranteed maximum settling time specification (500ns to 0.1%) even at the closed loop gains encountered with the DAC1106/1108. Furthermore, when the closed loop gain is greater than 3, no external compensating components are required.

Figures 8 and 9 below show the proper means of connecting the converter to an op amp for unipolar and bipolar operation.

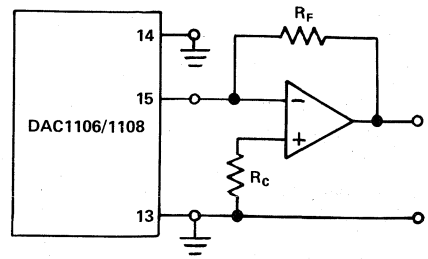


Figure 8. Connections to an External Op Amp (Unipolar)

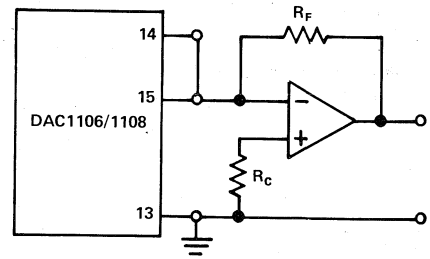


Figure 9. Connections to an External Op Amp (Bipolar)

The resistor R_C is used with the AD509K for bias current compensation. Because of the low bias currents inherent with the model 50, R_C is unnecessary and the noninverting input is connected directly to ground.

Great care must be taken in laying out the circuits of Figures 8 and 9 to assure true high speed performance. Several of the most important considerations are listed below:

1. Keep leads, especially those between the converter output and op amp summing junction, as short as possible to prevent the introduction of noise.
2. Orient components to minimize stray capacitance.
3. Carefully bypass power supplies to the op amp.
4. Select suitable components such as metal film resistors with their low capacitance and low stray inductance.
5. Design the signal and power supply ground circuits so as to prevent the introduction of extraneous voltages in ground signal path.
6. Use separate returns for analog and digital grounds. The DAC1106/1108 and op amp power supply returns go to analog ground; any logic circuits that precede the converter go to digital ground.

High Resolution 16- and 18-Bit Digital to Analog Converters

DAC1136/1138

FEATURES

DAC1138

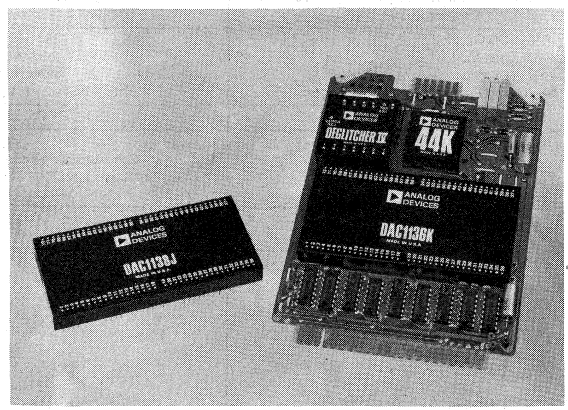
18-Bit Resolution and Accuracy (38μV, 1 Part in 262,144)
Nonlinearity 1/2LSB max (DAC1138K)
Excellent Stability
Settling to 1/2LSB (0.0002%) in 10μs
Hermetically-Sealed Semiconductors

DAC1136

16-Bit Resolution and Accuracy (152μV, 1 Part in 65,536)
Low Cost
Nonlinearity 1/2LSB max (DAC1136K, L)
Settling to 1/2LSB max (0.0008%) in 6μs

DEGLITCHER IV

Eliminates DAC Glitches
Available on DAC1136/1138 Card-Mounted Assembly



GENERAL DESCRIPTION

The DAC1136/1138 are complete self-contained current or voltage output modular digital to analog converters with resolutions and accuracies of 16 and 18 bits.

The DAC1136/1138 combine precision current sources with state-of-the-art steering switches to produce a very linear output. Inputs to these converters are compatible with TTL levels. The converters have a current output of −2mA full scale. A voltage output can be obtained by connecting the internal amplifier to the current output by means of jumpers. By using additional jumpers, the user can select any one of the following output ranges: 0 to +5V, 0 to +10V, ±5V, or ±10V.

The DAC1136/1138 are available on Card-Mounted Assemblies. In this configuration, selectable options include: input codes, output amplifiers, and a high speed transient-suppressing Deglitcher Module, Deglitcher IV.

WHERE TO USE HIGH RESOLUTION DACS

The DAC1136/1138 deliver exceptional accuracy for a broad range of display, test and instrumentation applications. The DAC1136, with a resolution of 16 bits or 1 part in 65,536, and the DAC1138 with a resolution of 18 bits or 1 part in 262,144 are ideally suited for applications requiring wide dynamic range measurement and control. Applications include data acquisition systems, high resolution CRT displays, automatic semiconductor testing, photo-typesetting, frequency synthesis and nuclear reactor control.

CERTIFICATE OF CALIBRATION

Each DAC1138 has been calibrated with equipment and methods that are traceable to the National Bureau of Standards (NBS). A Certificate of Performance is sent with each unit, which includes 1000 hour stability data for the reference zener and linearity test data.

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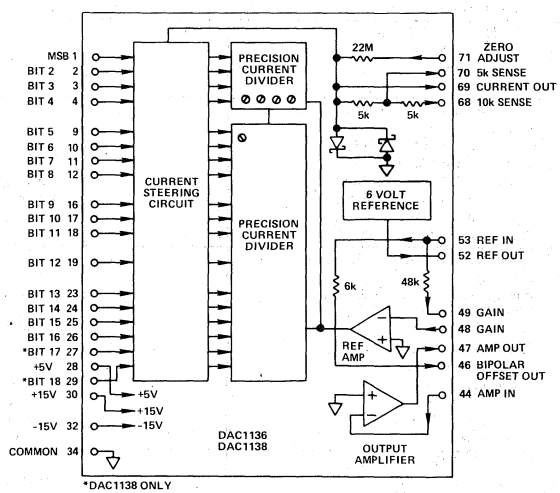


Figure 1. Block Diagram and Pin Designations

SPECIFICATIONS (typical @ +25°C, rated power supplies unless otherwise noted; specifications for mounting card with amplifier/deglitcher options same as module unless otherwise noted)

	DAC1136 Module			DAC1136 on Mounting Card with Amplifier/Deglitcher Options.		
	J	K	L	Deglitcher IV (Internal AD542K)	Low Drift 234L w/wo Deglitcher	High Speed 44K w/wo Deglitcher
RESOLUTION, BITS	16					
ACCURACY						
Integral Nonlinearity	±1LSB max	±1/2LSB max	±1/2LSB max			
Differential Nonlinearity	±1LSB max	±1/2LSB max	±1/2LSB max			
Gain and Offset Error (Externally Adjustable)		±1LSB		Gain, offset and glitch-nulling adjustments provided on the mounting card.		
ANALOG OUTPUT						
Unipolar Mode	−2mA to 0mA					
Bipolar Mode	−1mA to +1mA					
Voltage Output Range (Pin Selectable)	0 to +5V, 0 to +10V, ±5V, ±10V					
DIGITAL INPUTS	TTL/CMOS; See Figure 2					
INPUT CODES						
Unipolar Mode	Complementary Binary (COMP BIN)			BIN, COMP BIN, 2's COMP, COMP 2's COMP		
Bipolar Mode	Complementary Offset Binary (COMP OBIN)			OBIN, COMP OBIN SIGN PLUS MAG BIN, COMP SIGN PLUS MAG BIN		
STROBE INPUT	None			One standard series 74LS load, leading-edge triggered, pulse width 100ns minimum.		
DYNAMIC CHARACTERISTICS						
Settling Time to 1/2LSB						
Current						
Full Scale Step	8µs			Voltage Output, Only		
LSB Step	6µs			Voltage Output, Only		
Voltage						
Unipolar (10V Step)	90µs			80µs	45µs	25µs
Bipolar (20V Step)	250µs			90µs	60µs	30µs
LSB Step	8µs			8µs	8µs	8µs
Slew Rate	1V/µs			2V/µs	6V/µs	20V/µs
TEMPERATURE COEFFICIENTS (ppm of FSR/°C)[1]						
Integral Nonlinearity	±1	±1	±1.5 max			
Differential Nonlinearity	±1	±1	±1.5 max			
Gain (Excluding V_{REF})	±5	±5	±8 max			
Offset						
Unipolar Mode	±0.5			±0.5	±0.1	±2
Bipolar Mode	±5					
STABILITY, LONG TERM (ppm of FSR/1,000 hrs.)[2]						
Gain (Excluding V_{REF})	±5					
Offset	±6			±1	±0.5	±25
NOISE (Include V_{REF}; Double for Bipolar Mode)						
Output Current (BW = 100kHz)	0.5nA rms			Voltage Output, Only		
Output Voltage (BW = 0.1–10Hz)						
@ 0V (A11 1's Code; "ZERO")	4µV pk-pk					
@ 5V (MSB = 0 Code; "Half Scale")	6µV pk-pk					
@ 10V (A11 0's Code; "Full Scale")	9µV pk-pk					
Output Voltage (BW = 100kHz)	30µV rms			20µV rms	40µV rms	35µV rms
VOLTAGE COMPLIANCE (Amplifier Offset, E_{OS})						
Max E_{OS} Allowed for Rated Accuracy	±2mV max					
Initial E_{OS} (Factory Adj.)	±100µV			±50µV	±20µV	±100µV
E_{OS} Drift	±10µV/°C			±5µV/°C	±0.1µV/°C	±15µV/°C
Current Output (pin 69)						
Voltage Protection	via Internal Schottky Diodes					
Source Resistance						
Unipolar Mode	>33kΩ					
Bipolar Mode	>5kΩ					
Source Capacitance	150pF					
REFERENCE VOLTAGE (V_{REF})						
Voltage ($Z_{OUT} \approx 200\Omega$)	+6.000V (Maximum Error, ±0.024V)					
Noise (BW = 0.1–10Hz)	3µV pk-pk					
Tempco	5ppm/°C					
POWER SUPPLY REQUIREMENTS[3]						
+5V dc, ±5%	9mA				95mA	
±15V dc, ±5%	±30mA			±38mA	±37mA	±40mA
POWER SUPPLY REJECTION (±15V dc)						
Gain or Offset vs. FSR	80dB			100dB	100dB	75dB
Differential Nonlinearity	±1/4LSB per Volt ΔV_S					
ENVIRONMENTAL						
Operating Temperature	0 to +70°C			−55°C to +80°C	−55°C to +85°C	−55°C to +85°C
Storage Temperature	−55°C to +85°C					
Humidity	5% to 95%, Noncondensing					

NOTES:
[1]Temperature coefficients guaranteed maximum from 15°C to 35°C, typical from 0 to +70°C.
[2]Recommended DNL calibration check: 6 months.
[3]Recommended Power Supply: Analog Devices Model 923.
Specifications subject to change without notice.

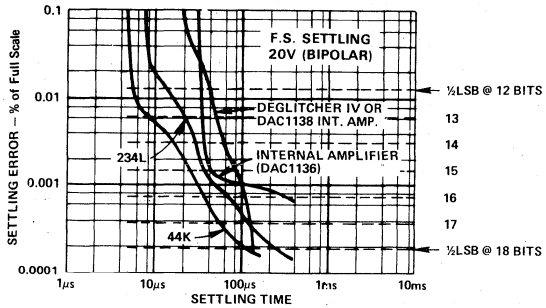
SPECIFICATIONS (typical @ +25°C, rated power supplies unless otherwise noted; specifications for mounting card with amplifier/deglitcher options same as module unless otherwise noted)

	DAC1138 Module		DAC1138 on Mounting Card with Amplifier/Deglitcher Options.	
	J	K	Deglitcher IV (Internal AD542K)	Low Drift 234L w/wo Deglitcher
RESOLUTION, BITS	18			
ACCURACY				
Integral Nonlinearity	±1LSB max	±1/2LSB max		
Differential Nonlinearity	±1LSB max	±1/2LSB max		
Gain and Offset Error (Externally Adjustable)		±1LSB	Gain, offset and glitch–nulling adjustments provided on the mounting card.	
ANALOG OUTPUT				
Unipolar Mode	−2mA to 0mA			
Bipolar Mode	−1mA to +1mA			
Voltage Output Range (Pin Selectable)	0 to +5V, 0 to +10V, ±5V, ±10V			
DIGITAL INPUTS	TTL/CMOS; See Figure 2			
INPUT CODES				
Unipolar Mode	Complementary Binary (COMP BIN)		BIN, COMP BIN, 2's COMP, COMP 2's COMP	
Bipolar Mode	Complementary Offset Binary (COMP OBIN)		OBIN, COMP OBIN SIGN PLUS MAG BIN, COMP SIGN PLUS MAG BIN	
STROBE INPUT	None		One standard series 74LS load, leading-edge triggered, pulse width 100ns minimum.	
DYNAMIC CHARACTERISTICS				
Settling Time to 1/2LSB				
Current				
Full Scale Step	10µs		Voltage Output, Only	
LSB Step	8µs		Voltage Output, Only	
Voltage				
Unipolar (10V Step)	175µs		80µs	45µs
Bipolar (20V Step)	140µs		90µs	60µs
LSB Step	18µs		18µs	18µs
Slew Rate	2V/µs		2V/µs	6V/µs
TEMPERATURE COEFFICIENTS (ppm of FSR/°C)[1]				
Integral Nonlinearity	±0.3			
Differential Nonlinearity	±0.4			
Gain (Excluding V_{REF})	±0.8			
Offset				
Unipolar Mode	±0.5		±0.5	±0.1
Bipolar Mode	±1			
STABILITY, LONG TERM (ppm of FSR/1,000 hrs.)[2]				
Gain (Excluding V_{REF})	±2			
Offset	±2		±1	±0.5
NOISE (Include V_{REF}; Double for Bipolar Mode)				
Output Current (BW = 100kHz)	0.5nA rms		Voltage Output, Only	
Output Voltage (BW = 0.1–10Hz)				
@ 0V (A11 1's Code; "ZERO")	4µV pk-pk			
@ 5V (MSB = 0 Code; "Half Scale")	6µV pk-pk			
@ 10V (A11 0's Code; "Full Scale")	9µV pk-pk			
Output Voltage (BW = 100kHz)	30µV rms		20µV rms	40µV rms
VOLTAGE COMPLIANCE (Amplifier Offset, E_{OS})				
Max E_{OS} Allowed for				
Rated Accuracy	±200µV max			
Initial E_{OS} (Factory Adj.)	±100µV		±50µV	±20µV
E_{OS} Drift	±10µV/°C		±5µV/°C	±0.1µV/°C
Current Output (pin 69)				
Voltage Protection	via Internal Schottky Diodes			
Source Resistance				
Unipolar Mode	>33kΩ			
Bipolar Mode	>5kΩ			
Source Capacitance	150pF			
REFERENCE VOLTAGE (V_{REF})				
Voltage ($Z_{OUT} \approx 200\Omega$)	+6.000V (Maximum Error, ±0.024V)			
Noise (BW = 0.1–10Hz)	3µV pk-pk			
Tempco	5ppm/°C			
POWER SUPPLY REQUIREMENTS[3]				
+5V dc, ±5%	9mA			95mA
±15V dc, ±5%	±30mA		±38mA	±37mA
POWER SUPPLY REJECTION (±15V dc)				
Gain or Offset vs. FSR	80dB		100dB	75dB
Differential Nonlinearity	±1/4LSB per Volt ΔV_S			
ENVIRONMENTAL				
Operating Temperature	0 to +70°C			
Storage Temperature	−55°C to +85°C		−55°C to +80°C	−55°C to +85°C
Humidity	5% to 95%, Noncondensing			

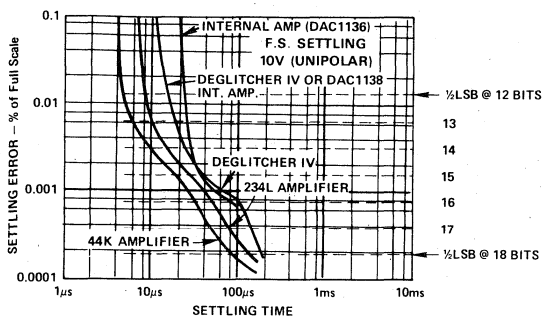
NOTES:
[1]Temperature coefficients guaranteed maximum from 15°C to 35°C, typical from 0 to +70°C.
[2]Recommended DNL calibration check: 6 months.
[3]Recommended Power Supply Analog Devices: Model 923.
Specifications subject to change without notice.

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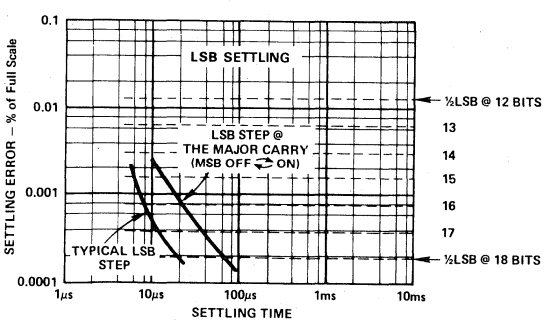
Characteristic Curves*



Settling Time (Voltage Output) vs. %-of-Full-Scale-Error for 20V Output Step (+10V ⇄ -10V)



Settling Time (Voltage Output) vs. %-of-Full-Scale-Error for 10V Output Step (0V ⇄ +10V)

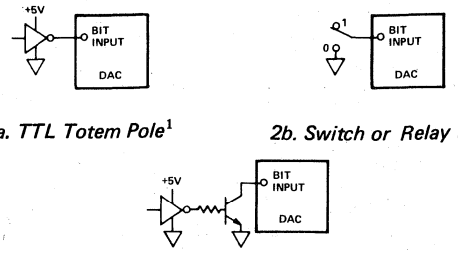


Settling Time (Voltage Output) vs. %-of-Full-Scale-Error for LSB Steps (Essentially Independent of Amplifier Used). With Deglitcher IV, the LSB Step at the Major Carry Settles as Fast as the Typical LSB Step, Following the 11μs Hold Period.

*NOTE: All curves typical at rated supply voltage.
F.S. = Full Scale

INPUT CONSIDERATIONS

The DAC1136/1138 may be driven by TTL or CMOS as shown in Figure 2. Note that the TTL input is shown with inputs for both a direct "totem pole" TTL gate and open collector (or "pull-up") configurations.



2a. TTL Totem Pole[1] *2b. Switch or Relay Inpu*

2c. CMOS Input

1. FOR TTL WITH OPEN COLLECTOR, DO NOT USE EXTERNAL PULL-UP. CONVERTERS HAVE INTERNAL 10kΩ PULL-UP ON EACH INPUT TO 3.8V.
2. USE SPST SWITCH OR RELAY TO GROUND. WHEN SWITCH IS OPEN, THE INTERNAL 10kΩ WILL PULL INPUT UP TO 3.8V.

Figure 2. Input Connections

OUTPUT CONNECTIONS AND GUARDING

The DAC1136/1138 output connections for various voltage ranges are shown in Figure 3.

Since an LSB is only 38μV (at 10 volts full scale for the DAC1138), care must be exercised to properly guard the current output of the converter from leakage current. Any connection made to the DAC's current output (pin 69) should be guarded. Suggested printed circuit board guarding is shown in Figure 3. The optional Card-Mounted Assemblies of the DAC1136/1138 have been carefully designed for optimum guarding and performance.

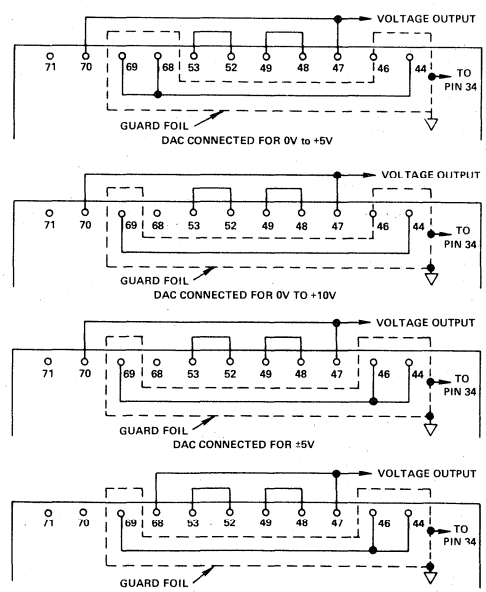
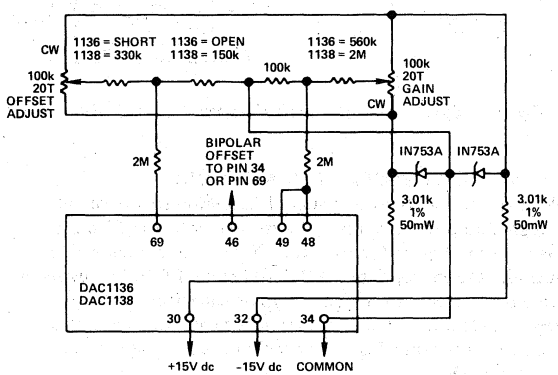


Figure 3. Output Voltage Connections and Suggested PCB Guarding (Unipolar and Bipolar)

GAIN AND OFFSET ADJUSTMENTS

The gain and offset adjustments are made with external potentiometers which the user supplies. With the appropriate digital inputs applied, these potentiometers are adjusted until the desired output voltage is obtained. The proper connections for offset and gain are shown in Figure 4. The voltmeter used to measure the output should be capable of stable resolution of 1/4LSB in the region of zero and full scale. Because of the interaction between offset and gain adjustments, the adjustment procedure described below should be carefully followed. Offset adjustment affects gain, but gain adjustment does not affect offset.



NOTES:
1. ALL FIXED RESISTORS ARE 5% CARBON COMP, UNLESS OTHERWISE NOTED.
2. ALL POTENTIOMETERS ARE 20-TURN INFINITE RESOLUTION TYPE.

Figure 4. Gain and Offset Adjustments

For unipolar mode, apply a digital input of all "1's" (complementary binary code for zero output) and adjust the offset potentiometer until a 0.00000V output is obtained (see Table 1). Once the appropriate offset adjustment has been made, apply a digital input of all "0's". Adjust the gain potentiometer until the plus full scale output is obtained (see Table 1).

For bipolar mode, apply a digital input of all "1's" (complementary offset binary code for minus full scale) and adjust the offset potentiometer for the proper minus full scale output voltage (see Table 1). Once the appropriate minus full scale adjustment has been made, apply a digital input of all "0's". Adjust the gain potentiometer until the plus full scale output shown below is obtained.

RANGE	IDEAL OUTPUT		
		DAC1138	DAC1136
Unipolar:	All 11...1	All 00...0	
0V→+10V	0.00000V	+9.999962V	+9.999848V
0V→+5V	0.00000V	+4.999981V	+4.999924V
Bipolar:			
-10V→+10V	-10.00000V	+9.999934V	+9.999695V
-5V →+5V	-5.00000V	+4.999962V	+9.999848V
To adjust:	Adjust ZERO pot	Adjust GAIN pot	

Table 1. Full Scale Output

DIFFERENTIAL LINEARITY ADJUSTMENT

Each DAC1136/1138 has been factory calibrated and tested to achieve the performance indicated in the electrical specifications. Before attempting recalibration, it is imperative that the circuit be checked to confirm that all previously described precautions have been taken to insure proper application at the 16- or 18-bit level. Basically, the DAC is trimmed by comparing a bit to the sum of all lower bits, and adjusting, if necessary, for a one LSB positive difference. The top 4 major carries, i.e., MSB minus the sum of bits 2-through-the-LSB, down through bit 4 minus the sum of bits 5-through-the-LSB, can be trimmed using the procedure outlined below. A differential voltmeter capable of 100μV Full Scale should be connected to V_{OUT} of the DAC. This will resolve an LSB which at 18 bits is 38μV (10V range). A Fluke 895A or equivalent is recommended.

1. Bit 4 Trim
   a. Set bit inputs to 11110 . . . . 0.
   b. Read the output voltage by nulling the voltmeter.
   c. Set bit inputs to 11101 . . . . 1.
   d. Read voltage by nulling voltmeter. This reading should be equal to that of step 1b plus 1LSB. Adjust bit 4 if required (see B4, Figure 7).

2. Bit 3 Trim
   a. Set bit inputs to 1110 . . . . 0.
   b. Read output voltage by nulling the voltmeter.
   c. Set inputs to 1101 . . . . 1.
   d. Read voltage by nulling the voltmeter. This reading should be equal to that of step 2b plus 1LSB. Adjust bit 3 if required (see B3, Figure 7).

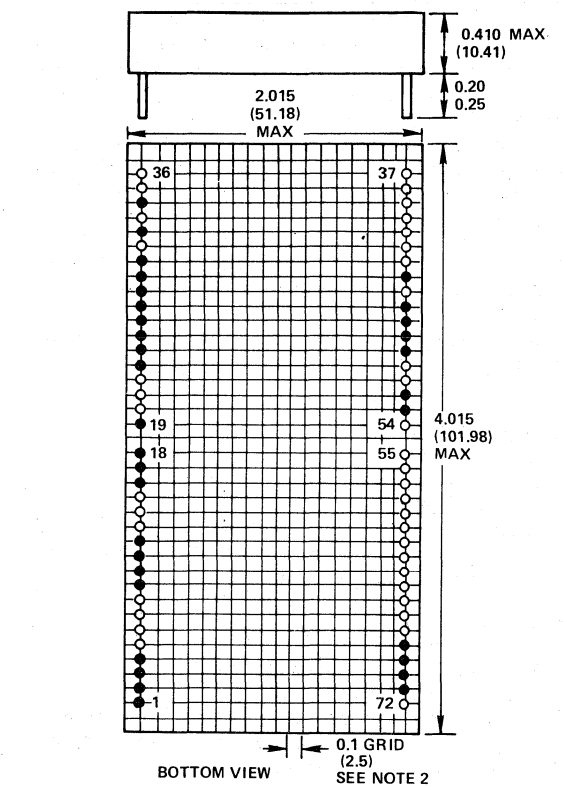
3. Bit 2 Trim
   a. Set bit inputs to 110 . . . . 0.
   b. Read output voltage by nulling the voltmeter.
   c. Set bit inputs to 101 . . . . 1.
   d. Read voltage by nulling voltmeter. This reading should be equal to that of step 3b plus 1LSB. Adjust bit 2 if required (see B2, Figure 7).

4. Bit 1 (MSB) Trim
   a. Set bit switches to 100 . . . . 0.
   b. Read output voltage by nulling the voltmeter.
   c. Set bit switches to 011 . . . . 1.
   d. Read voltage by nulling voltmeter. This reading should be equal to that of step 4b plus 1LSB. Adjust bit 1 (MSB) if required (see MSB, Figure 7).

If insufficient range exists on any adjustment, then a separate adjustment for the weight of bits 5-through-the-LSB (see Sum B5 → LSB, Figure 6) should be performed. This condition will probably not occur on bit 2, 3 and 4 but might occur on the MSB. If adjustment of the sum of bits 5-through-the-LSB is made, the trim procedure for all bits should be repeated. Obviously, since the procedure affects the weight of individual bits, it affects the overall gain of the DAC. The final step should be adjustment of gain (user supplied adjustment external to module, or pot at edge of mounting card).

OUTLINE DIMENSIONS AND PIN DESIGNATIONS

Dimensions shown in inches and (mm).



NOTES:
1. PINS: 0.019 ±0.001 DIA.
2. GRID AND MARKINGS NEXT TO PINS ARE FOR REFERENCE ONLY AND DO NOT APPEAR ON UNIT.
3. PINS 27 AND 29 ARE NOT PRESENT ON DAC1136.

USING AN EXTERNAL 6V REFERENCE

The DAC1136/1138 can be operated with an external reference connected to pin 53 of the module. The current drain on the external reference will be 1.125mA in bipolar mode or 0.125mA in unipolar mode (pin 46 should be left open and not grounded when using an external reference in the unipolar mode). When an external reference is used, pin 52, (the output of the internal reference) is left open.

Codi Semiconductor manufactures a reference module called Certavolt[1] with a 10 volt output accurate to 0.001%. This output is temperature compensated to within 1ppm/°C from +15°C to +55°C. The Certavolt requires a power supply of +28V dc @ 20mA. To convert the +10 volt output of the Certavolt to the +6 volt reguired by the DAC, the circuit shown in Figure 5 is recommended.

[1] Certavolt is a registered trade name by Codi Semiconductor.

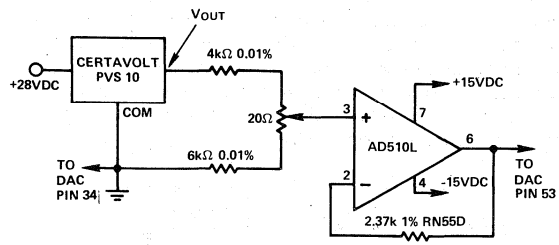
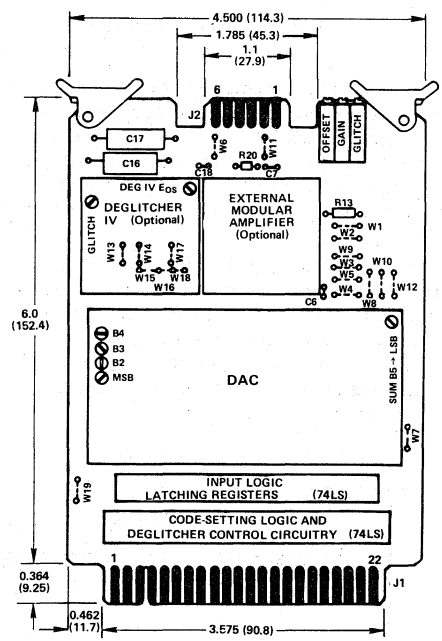


Figure 5. DAC1136/1138 with External Precision Reference

OPTIONAL CARD-MOUNTED ASSEMBLY

Analog Devices offers an optional Card-Mounted Assembly designed to provide optimum performance at the 18-bit level. As shown in Figure 6, this 4 1/2" X 6" printed circuit card includes the appropriate DAC GAIN and OFFSET adjustment potentiometers, power supply bypass capacitors and input registers. The Card-Mounted Assembly can be ordered with custom code-setting logic, external output amplifiers, and a Deglitcher IV.



W'S INDICATE JUMPER POSITIONS.
TO ISOLATE ANALOG AND DIGITAL GROUND W7 IS OMITTED.
W6 AND W11 ARE NOT INSTALLED WHEN USER DESIRES 4-WIRE CONNECTION TO J2 WHEN EITHER A 44K OR 234L AMPLIFIER IS USED.

Figure 6. Card-Mounted Assembly

CARD-MOUNTED ASSEMBLY JUMPER DESIGNATIONS

The output voltage range, reference source, amplifier and deglitcher configurations are programmed at the factory by means of jumpers, resistors, and capacitors (see ordering guide for details). The mounting card can be programmed by the user, if necessary, as shown below.

Output Voltage Range	Install Jumpers
±10V	W10, W5
±5V	W12, W5
+10V	W12, W3

Reference	Install Jumpers
Internal	W2
External	W1

Amplifier	Install Jumpers
Internal	W4, W9
External[1]	W8, W13
Deglitcher IV[2]	W8, W15, W17, W18
Deg. IV with Ext Amp[3]	W8, W14, W16

NOTES:

[1] With a 234L amplifier install C7 (0.01μF, 10%, ceramic capacitor). With a 44K amplifier use a variable resistor (typ value ≈ 499Ω, 0.1W, 1%) to adjust the output voltage for a ±100μV reading as measured between pins 69 and 34 of the DAC (this step sets voltage compliance); install this value resistor (R13 position).

[2] With Deglitcher IV remove R20 (100Ω) and replace the resistor with a jumper.

[3] With Deglitcher IV and a 234L amplifier remove C6 (6.8pF Capacitor) and install: C7 (0.01μF, 10%, ceramic capacitor), C18 (100pF, 10%, ceramic capacitor), C17 (1000pF, 10%, polystyrene capacitor) and replace R20 (100Ω) with a jumper. With Deglitcher IV and a 44K amplifier perform the operation described in Note 1, remove C6 (6.8pF capacitor) and install: C18 (100pF, 10%, ceramic capacitor), C17 (1000pF, 10% polystyrene capacitor) and replace R20 (100Ω) with a jumper.

CONNECTOR J1

PIN	FUNCTION	PIN	FUNCTION
A	BIT 1	U	STROBE
B	BIT 2	V	BIT 18[1]
C	BIT 3	W	+5V
D	BIT 4	X	+15V
E	BIT 5	Y	-15V
F	BIT 6	Z	DIGITAL GND
H	BIT 7	1-4	NC
J	BIT 8	5	INTERLOCK
K	BIT 9	6	INTERLOCK
L	BIT 10	7-16	NC
M	BIT 11	17	BIT 17[1]
N	BIT 12	18	
P	BIT 13	19	
R	BIT 14	20	
S	BIT 15	21	
T	BIT 16	22	

J1 MATES WITH CINCH P.N. 251-22-30-160 (SUPPLIED).

[1] DAC1138 ONLY

CONNECTOR J2

PIN	FUNCTION
1	ANALOG SENSE LOW
2	ANALOG SOURCE LOW
3	NC
4	ANALOG SOURCE HIGH
5	ANALOG SENSE HIGH
6	ANALOG REF. IN/OUT
A	ANALOG REF. IN/OUT
B	ANALOG SENSE HIGH
C	ANALOG SOURCE HIGH
D	NC
E	ANALOG SOURCE LOW
F	ANALOG SENSE LOW

J2 MATES WITH CINCH P.N. 251-06-30-160 (SUPPLIED).

Mounting Card Connector Designations

DEGLITCHER IV

The Deglitcher IV is a precision high-speed, high-isolation sample-and-hold circuit which eliminates the glitches that occur whenever a DAC is dithered through a major carry. Such momentary transients can be of concern in applications such as high-resolution CRT beam positioning, where glitch-free code transitions are often required for optimum display quality and legibility. Oscilloscope photographs in Figures 7a and 7b below show the output of a DAC1136 being dithered up and down through the major carry, between codes 1000000000000000 and 0111111111111111. In Figure 7b, the Deglitcher IV is turned on virtually elminating the glitches and allowing the 152μV LSB step to be clearly seen.

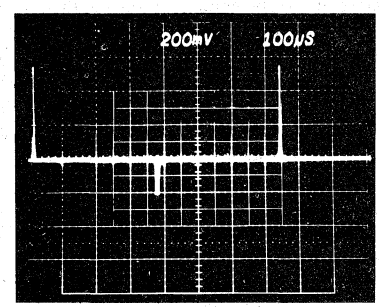


Figure 7a. DAC1136; Major-Carry Dither without Deglitcher IV (BW = 1MHz), Vertical Scale 0.2V/Division

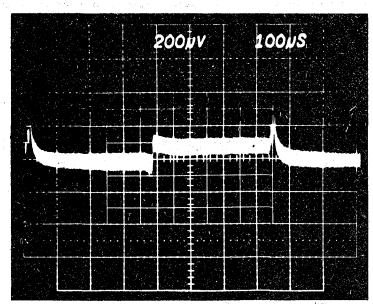


Figure 7b. Same Major-Carry Dither with Deglitcher IV (BW = 1MHz), Vertical Scale, 200μV/Division

The Deglitcher IV utilizes a proprietary sampling technique which isolates the output amplifier during the critical 10μs period immediately following a code change. The only discernible difference in DAC performance when used with Deglitcher IV is a delay of approximately 11μs after the strobe goes HI before the (deglitched) DAC output voltage starts slewing toward the new value.

GLITCH ADJUSTMENT

There are two "Glitch" adjustment potentiometers, accessible on the Card-Mounted Assembly. The adjustment on the card permits nulling of any Track-to-Hold offset, whereas the adjustment internal to the Deglitcher IV allows for precise nulling of the Hold-to-Track transient. Because of the near-infinite attenuation of the actual DAC current glitches, no current-glitch transient is visible on the output. For this reason, it is easiest to null the 2 Deglitcher adjustments while strobing the Card with a static digital input.

INPUT OPTIONS

The Card-Mounted Assembly contains input registers. The input code ordered by the user is set at the factory by means of various jumpers in the logic circuitry. See ordering guide for details.

Since the Card-Mounted Assembly contains input registers, the card requires a strobe pulse circuit. Strobe characteristics of input registers are:

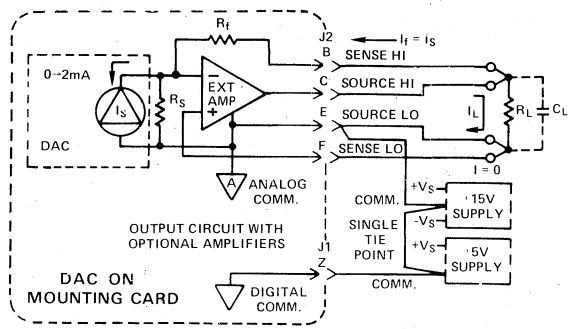
1. ⌐‾└ Strobe Pulse: One Std. series 74LS load, Leading-Edge-Triggered. Positive pulse should remain HI for > 100ns.
2. The digital input code can be changed at any time up to and including that instant when the strobe command goes HI.
3. The actual transfer of the input code to the DAC will occur ≈ 3μs after the strobe command; during this 3μs the digital input code to the card assembly should not be changed, in order to prevent the possible coupling of logic noise into the DAC output. At t_o +3μs, the deglitcher is automatically enabled for the following ≈ 8μs. Thus there will be a delay of ≈ 11μs before the deglitched output starts slewing to the new valve. Actual data transfer to the DAC automatically occurs at t_o +3.1μs.

OUTPUT OPTIONS

The Card-Mounted Assembly for the DAC1136/1138 allows for several user-selectable output configurations:

1. Internal Output Amplifier inside the DAC Module.
2. Analog Devices model 234L; for low noise, low drift applications (2μV, ±0.1μV/°C).
3. Analog Devices model 44K; available only with DAC1136; recommended only for high speed or high current applications.
4. Deglitcher IV with self-contained precision BI-FET output amplifier (AD542K).
5. Deglitcher IV with model 234L output amplifier.
6. Deglitcher IV with model 44K output amplifier (recommend with DAC1136 only).

When using an external amplifier, a four terminal output connection can be utilized on the Card-Mounted Assembly in order to allow for compensation of connector contact resistance.



NOTE:
1. VOLTAGE DROP BETWEEN SOURCE LO AND SENSE LO MUST OBSERVE CURRENT MODE COMPLIANCE LIMITS FOR RATED ACCURACY.
2. THIS CONNECTION SCHEME CANNOT BE USED WITH INTERNAL AMPLIFIER OF THE DAC OR WITH THE AMPLIFIER INTERNAL TO THE DEGLITCHER IV.

Figure 8. Four-Terminal Output Connections

ORDERING GUIDE

WHEN ORDERING THE DAC1136 OR DAC1138, ORDER EITHER:

1. Module only: DAC1136J, DAC1136K, DAC1136L, DAC1138J, DAC1138K

2. DAC1136/1138 as a Card-Mounted Assembly:

DAC113 □ □

CODE	CODE	DAC MODULE RESOLUTION	LINEARITY
6	J	16 BITS	15 BITS
6	K	16 BITS	16 BITS
6	L	16 BITS	16 BITS
8	J	18 BITS	17 BITS
8	K	18 BITS	18 BITS

NOTE:
1. NOT RECOMMENDED FOR DAC1138.

CODE	OUTPUT AMPLIFIER
1	INTERNAL
2	44K[1]
3	234L
4	DEGLITCHER IV
5	DEGLITCHER IV[1] AND 44K
6	DEGLITCHER IV AND 234L

CODE	INPUT LOGIC CODE
1	BIN/OBIN
2	COMP BIN/COMP OBIN
3	2'S COMP
4	COMP 2'S COMP
5	SIGN PLUS MAG BIN
6	COMP SIGN MAG BIN

CODE	OUTPUT VOLTAGE RANGE
1	+10V
2	±5V
3	±10V

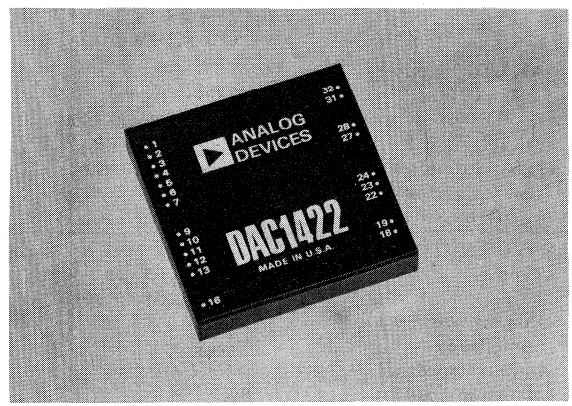
CODE	DAC VOLTAGE REFERENCE
1	INTERNAL
2	EXTERNAL

4-20mA, 8- and 10-Bit Digital-to-Analog Converters

DAC1420, DAC1422

FEATURES
- ISA S50.1 Type 3 Class U Output
- Guaranteed Monotonic 0 to +70°C
- Totally Powered From Loop Supply
- Wide Supply Range +10V to +36V
- Self-Contained Data Latch
- Auxiliary Analog Input
- No Minimum Load Requirement

APPLICATIONS
- Direct Digital Controllers
- Computer Based Process Control Systems
- Digital Pressure Transducers



GENERAL DESCRIPTION

Models DAC1420/1422 are 8/10-bit D/A converters with analog output in the form of a 4-to-20mA current source. Specifically designed for the process-control industry, and requiring but a single +10V to +36V power supply, they meet the requirements of ISA standard S50.1 for Type 3 Class U (3-wire nonisolated) output. Included in the 2″ X 2″ X 0.4″ module are a set of CMOS latches, an 8/10-bit CMOS DAC, two analog-to-current converters—one reflecting the translated output from the DAC, the other an auxiliary backup analog input—a current amplifier, and a regulator & reference. Figure 1 shows the basic connections and operation of the devices with an external loop supply and a remote load, R_L, supplied via a twisted pair.

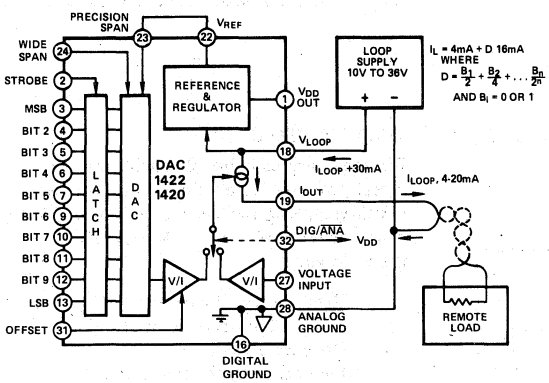


Figure 1. Block Diagram of the DAC1422 in a Simple Application

HOW LOOP DACS WORK

Figure 2 is a more-detailed version of Figure 1, showing some of the options available to the user in applying the DAC1420/1422. The basic digital-to-analog conversion is performed by a circuit employing an Analog Devices CMOS integrated-circuit multiplying DAC. Its output is a voltage, which is converted to a 4-to-20mA output current by a V-to-I converter circuit.

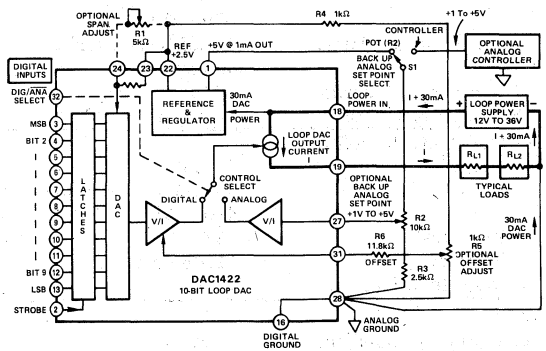


Figure 2. Loop DAC Block Diagram: Connections and Adjustments

SPECIFICATIONS

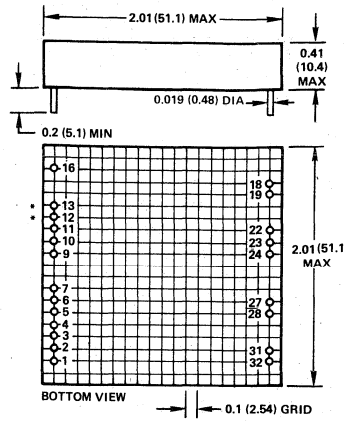
(typical @ +25°C, V_{LOOP} = +24 volts unless otherwise specified)

MODEL	DAC1420	DAC1422
DIGITAL INPUTS		
Resolution	8 Bits	10 Bits
Levels		
(Except "$\overline{ANA}$/DIG")	CMOS V_{DD} =5V	*
	"1" = >3.3V @ 1μA	*
	"0" = <1.7V @ 1μA	*
$\overline{ANA}$/DIG Input		
Impedance	12kΩ	*
"1"	"1" = >2.4V @ 140μA	*
"0"	"0" = <0.7V @ 0μA	*
Latch Strobe	Rising Edge Sensitive	*
T_{DH} (Data Hold)	0ns (min)	*
T_{DS} (Data Set-Up)	50ns (min)	*
ANALOG OUTPUT		
Type	ISA S50.1 Type 3 Meets	
	and Exceeds Class U	*
Nominal Range	4-20mA	*
Compliance	V_{LOOP} -6V	*
Output Impedance	>4MΩ @ dc	*
Minimum Load	0Ω	*
STABILITY AND ACCURACY		
Monotonicity	Guaranteed, 0 to +70°C	*
Integral Nonlinearity	±1/2LSB	*
Differential Nonlinearity	±1/2LSB	*
Temperature Stability		
Offset	25ppm FSR/°C	*
Span	50ppm FSR/°C	*
Adjustability	±10% each, Offset	
	and Span	*
Initial Error, Untrimmed[1]	±2LSB's each, Offset	
	and Span	*
Power Supply Rejection	20ppm FSR/V	*
Noise, 10Hz to 100Hz[2]	4mV p-p	*
ANALOG BACKUP INPUT		
Range[3]	1 - 5V	*
Gain	4mA/Volt (1-5V produces	*
	4-20mA)	*
Accuracy	±3%	*
Stability	±100ppm FSR/°C	*
Input Impedance	10^8 Ω	*
POWER		
Loop Supply, minimum	+10V	*
maximum	+36V	*
Supply Current	I_{OUT} +30mA	*
ENVIRONMENTAL		
Operating Temperature	0 to +70°C	*
Storage Temperature	-25°C to +85°C	*
SIZE	2" X 2" X 0.4"	*

NOTES
*Specifications same as DAC1420.
[1] Both offset and span error are adjustable to zero. See Figures 5 and 6 for details.
[2] Load = 750Ω|| 1,000pF.
[3] This input should not exceed +5.5V and should be grounded if not used.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTE:
Module Weight: 1.6 ounces (45G)

*Pins 12 & 13 appear on DAC1422 only.

DIGITAL INPUT	NOMINAL CURRENT OUTPUT
Binary Code	
1 1 1 1 1 1 1 1 1 1	+19.984mA
0 0 0 0 0 0 0 0 0 1	+ 4.016mA
0 0 0 0 0 0 0 0 0 0	+ 4.000mA

Table 1. Nominal Input-Output Relationships

DAC1423: ISO-DAC™

For applications in hostile environments, where ground loop elimination is required, consider Analog Devices model DAC1423. This isolated 10-bit 4-20mA DAC offers the following:

- High Voltage Protection (1500V dc)
- 8- and 10-bit Bus Compatibility
- Fail Safe Design
- Increment/Decrement Back-Up
- Bumpless Transfer

An important feature of the loop DAC is the self-contained input latch, which permits many DACs to operate from a single parallel bus. The analog output of the DAC changes when a new digital word is latched; i.e., the latch is strobed by a rising-edge signal to latch the digital data appearing on the bus. The DAC output current in this case, is shown driving a pair of external loads in series (RL_1 and RL_2). The maximum allowable value of the total load resistance is determined by the ratio of the compliance voltage, V_{LOOP}–6V, and full-scale output, 20mA. With V_{LOOP} at 36V, the maximum load resistance is 30V/20mA = 1.5kΩ. Since the DAC draws an additional 30mA of operating power from the loop supply, the supply should be rated at 50mA per DAC.

The DAC requires no digital power; it takes all of its power from the loop supply. It can furnish an output of 5V at up to 1mA for low-power CMOS logic. To operate the DAC, the +2.5V reference is jumpered to the PRECISION SPAN input, providing a span accuracy of ±16mA ±0.2%. If greater accuracy, or a different value of span, is required, an external resistor may be connected between the reference and the WIDE SPAN input, for a ±10% range of span adjustment.

The DAC1422's output offset (actually the 4mA output setting) is factory-trimmed to within ±0.2% of full scale (2LSB). If greater precision is required, the resistor network, R4, R5, R6, is connected between the reference and the OFFSET terminal. Because of interaction between SPAN and OFFSET, both adjustments should be repeated so as to converge on an accurate setting.

A key feature of the loop DAC is the ability to revert automatically to a backup analog input (1 to 5V, or 250Ω load on the output of a 4-to-20mA analog controller) if the computer crashes or loses power, since loop power can be supplied independently. A solid-state analog switch, its position controlled by the logic level on DIG/$\overline{\text{ANA}}$ (logic 1 for digital), connects either the DAC output of the backup input to the controlled current source.

This feature is versatile. With the computer's power bus connected to DIG/$\overline{\text{ANA}}$, it will automatically switch to analog if the computer dies, and the separately powered DAC's output will stay alive even though the computer loses power. Or DIG/$\overline{\text{ANA}}$ can be connected to a digital command output which restores analog if the computer is performing anomalously.

The backup analog input can come from the fixed +5V output and a resistor network, or it can be connected to a backup analog controller, as noted in Figure 2 (S1 to right); this backup might be the original equipment in a system being changed over to digital control.

DIGITAL CONTROL

The principal application for these loop DACs is in *direct digital control of analog process loops.* Figure 3 is a functional block diagram of a typical system containing several loop DACs. It consists of a computer, a set of loop DAC's, a data-acquisition system, the controlled process, and an independent loop power supply. System setpoints defining the desired values of process variables—whether determined manually, by a higher-level host computer, or by computation within the computer—are compared with the process inputs; and output values for the actuators are computer. The parallel digital output bus from the computer can be connected to all the loop DACs. The data in each DAC is then updated, either sequentially or at random, by a strobe signal from the computer, addressed to the desired DAC.

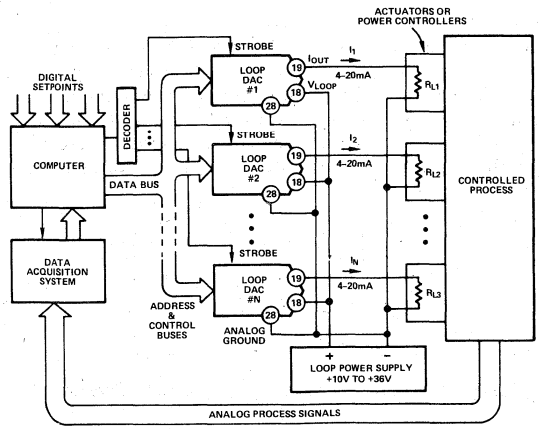


Figure 3. Typical Appications of Loop Dacs

The 4-to-20mA output of each DAC is a direct function of the 8- or 10-bit word which has been latched into its input register. Each current output is transmitted to its remote actuator/controller and develops a voltage across its load resistance. The return current may be over a common line, as shown in Figure 3, or over a set of individual twisted pairs with the common connection at the loop supply.

10

POWER/OUTPUT CONNECTIONS (Figure 4)

The DAC1420/1422 outputs are current sources designed to drive a grounded load. The maximum value of R_L is dependent upon the loop supply and full scale output current according to the formula:

$$R_L\ (\text{max}) = \frac{V_{LOOP} - 6V}{I_{OUT}\ (\text{FSR})}$$

For example, at 20mA, V_{LOOP} = 24 Volts, the maximum R_L is 900Ω. There is no minimum R_L required; the DAC1420/1422 maintain rated performance into a short circuit load.

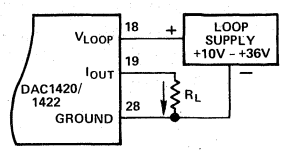


Figure 4. Output/Power Connections

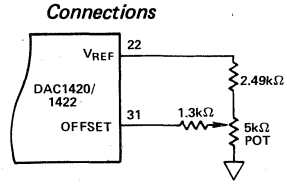


Figure 5. Offset Adjustment Circuit

OFFSET ADJUSTMENT (Figure 5)

The DAC1420/1422 are factory trimmed for offset to within ±0.2% FSR (2LSB's). For this performance, leave the offset pin (pin 31) unconnected. If potentiometer trimming is required, the circuit in Figure 5 will provide approximately ±10% offset adjustment. For greater adjustment resolution, increase the resistor in series with pin 31.

SPAN ADJUSTMENT (Figures 6a & 6b)

If no span adjustment is desired, connect pin 22 (V_{REF}) to pin 23 (Precision Span) for factory trimmed span accuracy of ±0.2% (2LSB's). If span adjust is required, the circuit in Figure 6b will allow ±10% minimum span adjustability. To increase the resolution of the adjustable span, use a resistor in series with the pot and reduce the value of the pot accordingly.

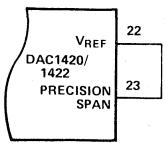


Figure 6a. Factory Trimmed

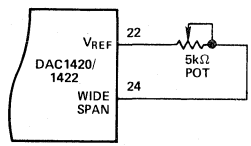


Figure 6b. Span Adjust

STROBE INPUT

The input latches in the DAC1420/1422 are CMOS rising edge sensitive devices. The last loaded digital word remains latched during backup manual operation providing the strobe input does not change. The user is cautioned that the digital inputs remain active even when the control is switched to analog.

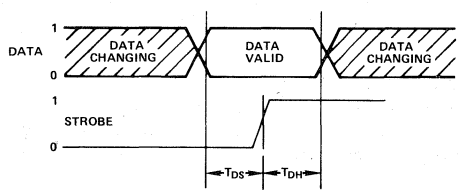


Figure 7. Input Timing

V_{DD} OUTPUT

The V_{DD} output may be utilized as a power supply for external CMOS circuitry such as tri state or buss transceivers, up to a limit of 1mA I_{DD}. If used in this fashion, it is recommended that the user add a 0.1μF bypass capacitor to ground from this pin to keep externally injected "glitches" from disturbing the internal circuitry of the DAC1420/1422.

ANALOG BACKUP INPUT

An Analog Backup Input is provided for use in controlling the output in case the source of digital inputs fail. This is a high impedance voltage input scaled so that 1-5 volts input gives 4-20mA output and is unaffected by the offset and gain adjustments. To prevent induced errors, this input should not exceed +5.5 volts and should be grounded if not used. Switchover to the analog input is provided by pin 32, the Digital/$\overline{\text{Analog}}$ control input. When at Logic "1" the 4-20mA output is controlled by the digital input. When at Logic "0", the 4-20mA output is controlled by the analog input. Figure 8 shows one possible use of the analog input: to provide for potentiometer-variable control in the event of computer failure. The V_{DD} OUT (pin 1) is used as a 5 volt reference for the potentiometer. If this feature is not used, connect pin 32 to pin 1 and pin 27 to ground.

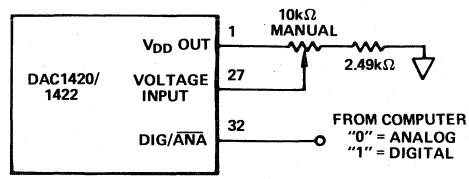


Figure 8. Potentiometer Backup Control

NOISE AND BANDWIDTH CHARACTERISTICS

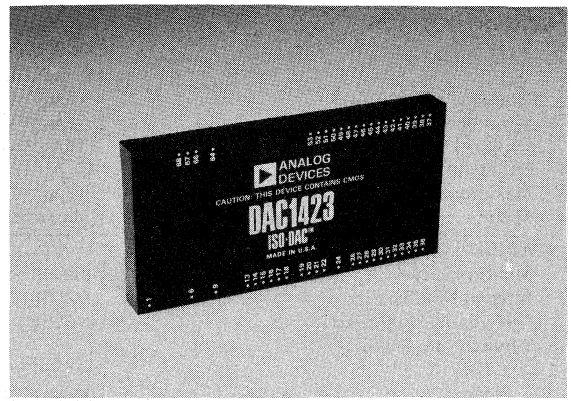
The DAC1420/1422 are used in control systems of modest bandwidth and speed. The noise specification given in the Electrical Characteristics is the typical noise that would be seen under that condition of load and bandwidth. The noise seen at the output of the DAC depends upon the capacitive and resistive load and the bandwidth of the instrument doing the measurement. The majority of the output noise is generated at approximately 65kHz by an internal charge pump inverter which supplies power to the internal DAC. Since the noise fundamental is at a much higher frequency than the systems where the DAC1420/1422 are likely to be used, the output noise should be observed over a limited bandwidth. Therefore, Analog Devices recommends the use of an external capacitance typically in the range of 1000pF to 1μF. This capacitance includes the distributed capacitance of any cable connected to the output of the DACs as well as any value of discrete capacitance that may be used. The capacitive load also has an effect on the time constant of the DAC output. Capacitive load and load resistance form an RC time constant. For example, it takes approximately 7 time constants for the output to step from 4mA and be within 0.2% of full scale, 20mA.

4-20mA, 10-Bit, Isolated Digital-to-Analog Converter

DAC1423

FEATURES
- 3-Port Galvanic Isolation
- Guaranteed Monotonic 0 to +70°C
- Microprocessor Compatible Interface
- Increment/Decrement Backup Control
- May be Powered from Loop Supply
- Low Power: 450mW typ
- Output Will Drive 0Ω Loads
- Bumpless Transfer, Auto to Manual

APPLICATIONS
- Direct Digital Controllers
- Ground Loop Elimination in Industrial and Process Control
- High Voltage Protected Data Acquisition Systems
- Digital Pressure Transducers
- Driving Analog Recorders



GENERAL DESCRIPTION

Analog Devices' ISO-DAC™ (ISOlated Digital-to-Analog Converter) model DAC1423 is a low power 10-bit DAC with 4-20mA current output, designed specifically for the process and industrial control industry. Its advanced features and excellent performance make for easy application within new and existing control systems. The DAC1423 contains a CMOS holding register, allowing direct interface with microprocessors, CMOS digital-to-analog converter, voltage-to-voltage isolator and a voltage-to-loop current converter. The small size and low profile (2" X 4" X 0.4") allows much greater functional density than previously available solutions.

DESIGN FEATURES AND USER BENEFITS

Microcomputer Interface: The parallel digital interface is a 5V CMOS design with independently controllable input latches and Tri-State* buffers, split into upper and lower sections (an 8-bit and a 2-bit byte) so that 8- or 16-bit bus compatibility may be achieved.

True 3-Port Isolation: The output connections and power connections are galvanically isolated, both from each other and from the digital section. Each will accommodate a wide range of power supply voltages and may be operated from the same supply, if desired.

Increment/Decrement: Increment/decrement control is achieved via the input latch/counter. An internal slow speed clock is supplied for this operation. Overflow/underflow lockout circuitry is used to prevent full scale "bumps" from occurring.

*Tri-State is a trademark of National Semiconductor Corporation.
ISO-DAC is a trademark of Analog Devices, Inc.

Adjustable Offset and Span: The ISO-DAC has offset and span accuracies of ±2LSB's (±0.2% FSR) each. However, if the user desires adjustable offset and span, there are provisions for ±10% adjustment range for each.

High CMV Isolation: The isolation barriers will withstand 1.5kV dc continuously, or 1kV rms @ 60Hz for 60 seconds. The ISO-DAC is designed to meet the IEEE Standard for Transient Voltage Protection (472-1974: Surge Withstand Capability). Common Mode Rejection is excellent; typically, 103dB @ 60Hz for a 250Ω load.

Synchronized: The ISO-DAC may be synchronized to an external system clock, multiple DAC1423's may be on synchronized to one another. In the event of loss of external sync, the DAC1423 will "free run" on its own oscillator.

Isolated Power Out: An internally derived +5V supply is brought out so that the user may power a small amount of application circuitry from the DAC1423's power supply.

ISA-S50.1: The three terminal output structure conforms to the Instrument Society of America Standard ISA-S50.1, "Compatibility of Analog Signals for Electronic Industrial Process Instruments."

SPECIFICATIONS (typical @ +25°C, V_{LOOP} = +24 volts unless otherwise specified)

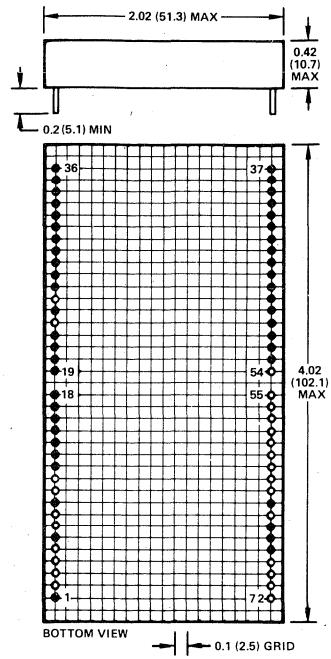
MODEL	DAC1423
DIGITAL INPUTS	
Resolution	10 Bits
Levels, CMOS V_{DD} = 5V	"1" = > 3.3V @ 1μA
	"0" = < 1.7V @ 1μA
Strobe	Level Sensitive (See Table 2)
ANALOG OUTPUTS	
Type	ISA S50.1 Type 3 Meets or Exceeds Class U
Nominal Range	4-20mA
Compliance	V_{LOOP} -6V
Output Impedance	>4MΩ @ dc
Minimum Load	0Ω
Maximum Load	(V_{LOOP} -6V/I_{OUT})
Maximum Capacitive Load	Unlimited
STABILITY AND ACCURACY	
Monotonicity	Guaranteed, 0 to +70°C
Integral Nonlinearity	±1/2LSB
Differential Nonlinearity	±1/2LSB
Temperature Stability	
Offset	50ppm FSR/°C
Span	50ppm FSR/°C
Adjustability	±10% each, Offset and Span
Initial Error, Untrimmed[1]	±2LSB's each, Offset and Span
Power Supply Rejection	20ppm FSR/V
Noise, 10Hz to 100Hz[2]	0.1LSB
Warm Up Time to Rated Accuracy	5 minutes
Warm Up Drift	0.5LSB
ISOLATION	
Max CMV, Inputs to Outputs	
ac, 60Hz, 1 minute	1000V rms
dc, Continuous	1500V dc
CMR, Inputs to Outputs, 60Hz, R_L = 250Ω	103dB
POWER	
Loop Supply Range	12–36V dc
Loop Supply Current	I_{OUT} + 5mA
Power Supply Range[3]	14–36V dc
Power Supply Current[3]	20mA
ENVIRONMENTAL	
Operating Temperature	0 to +70°C
Storage Temperature	-25°C to +85°C

NOTES:
[1] Both offset and span error are adjustable to zero. See Figure 2 for details.
[2] Load = 750Ω‖ 1,000pF and slow clock disabled.
[3] The DAC1423 can be entirely powered from the loop supply. See Figures 4 and 5 for details.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTE:
TERMINAL PINS INSTALLED ONLY IN SHADED HOLE LOCATIONS.
MODULE WEIGHT: 60.8G

MATING CARD
AC1582
(See Figure 13)

PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	I_{OUT}	72	NC
2	NC	71	NC
3	NC	70	NC
4	NC	69	NC
5	NC	68	SYNC IN
6	+V_{LOOP}	67	+V POWER
7	NC	66	SYNC OUT
8	NC	65	NC
9	COMMON	64	PWR COMMON
10	NC	63	NC
11	NC	62	NC
12	NC	61	NC
13	WIDE SPAN	60	NC
14	PRECISION SPAN	59	NC
15	+V_{REF}	58	NC
16	WIDE OFFSET	57	NC
17	PRECISION OFFSET	56	NC
18	SPAN COMMON	55	NC
19	DIGITAL COMMON[1]	54	NC
20	+5V_{OUT}	53	DIGITAL COMMON[1]
21	LOAD HIGH	52	CLOCK IN
22	LOAD LOW	51	LSB OUT
23	NC	50	BIT 9 OUT
24	LSB IN	49	BIT 8 OUT
25	NC	48	BIT 7 OUT
26	BIT 9 IN	47	BIT 6 OUT
27	BIT 8 IN	46	BIT 5 OUT
28	UP/$\overline{DN}$	45	READ HIGH
29	BIT 7 IN	44	READ LOW
30	BIT 6 IN	43	BIT 4 OUT
31	BIT 5 IN	42	BIT 3 OUT
32	BIT 4 IN	41	BIT 2 OUT
33	BIT 3 IN	40	MSB OUT
34	BIT 2 IN	39	CLOCK OUT
35	MSB IN	38	C_T
36	CLEAR	37	DIGITAL COMMON[1]

[1] PINS 19, 37 and 53 ARE INTERNALLY CONNECTED.

THEORY OF OPERATION

The ISO-DAC produces an isolated 4 to 20mA output current which is proportional to the input digital word. Each ISO-DAC contains a µcomputer compatible input section consisting of a 10-bit input latch, a 10-bit tri-state output and the associated control lines for read and write operations. A 10-bit CMOS digital-to-analog converter converts the digital word to a voltage that is modulated, carried across the isolation barrier, demodulated, and converted to a 4 to 20mA current output.

The remarkable performance of the ISO-DAC is derived from the carrier isolation technique which is used to transfer both signal and power between the input circuitry and the output stage. High CMV isolation, with excellent linearity, is achieved by the transformer coupling between the internal DAC, modulator section and the current output circuitry.

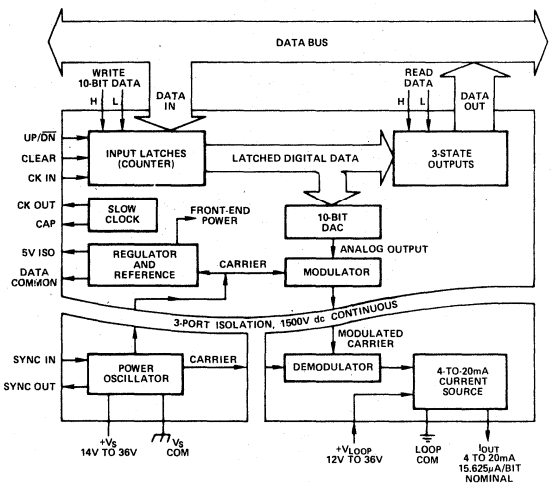


Figure 1. Block Diagram of the DAC1423

OFFSET AND SPAN ADJUSTMENTS

The DAC1423's initial offset and span accuracies are typically ±2LSB's (±0.2% FSR) each. If offset and span adjustments are not necessary, use the connections shown in Figure 2a.

Both offset and span errors are adjustable to zero with two external potentiometers, as shown in Figure 2b. To adjust the offset, apply a digital input of 0000000000 and adjust the offset potentiometer until an output of 4mA is obtained. Once the appropriate offset adjustment has been made, apply a digital input of 1111111111 and adjust the span potentiometer until 19.984mA is obtained. The offset and span adjustments are slightly interactive.

The offset and span potentiometers can provide a wide adjustment range to satisfy the particular needs of the application.

DIGITAL INPUT	NOMINAL CURRENT OUTPUT
Binary Code	
1111111111	+19.984mA
0000000001	+ 4.016mA
0000000000	+ 4.000mA

Table 1. Nominal Input-Output Relationships

The adjustment range of the span control will be typically ±10% full scale range (±2mA), while that of the offset control will be ±10% of offset (±0.4mA). Owing to the impedances involved, it is suggested that the adjustment pots be located near their respective connections or be well-guarded in order to avoid noise pickup.

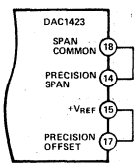


Figure 2a.

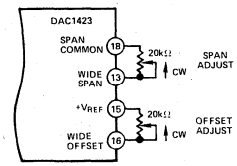


Figure 2b.

Figure 2. Precision and Adjustable Offset and Span

APPLICATION HINTS

The power supply should be carefully checked for noise, which would affect performance, and overshoot which could damage the device.

Unused digital inputs must always be grounded or taken to V_{DD} to ensure correct operation. Particular care should be taken when digital inputs are routed to another PC card. It is recommended that inputs open-circuited when PC cards are disconnected be taken to V_{DD} or GND via high value (1MΩ) resistors to prevent the accumulation of static charges.

10

ISOLATION CHARACTERISTICS

The DAC1423 employs a "three port" isolation architecture which allows for a great deal of flexibility in its application (see Figure 3). The power connections (pins 64, 66–68) are galvanically isolated from any other part of the module and may be subjected to the full common mode range with respect to either digital common or output common. Similarly, the output connections (pins 1, 6, 9) are isolated in the same manner from either power common or digital common.

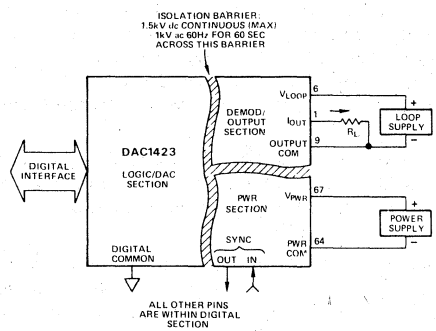


Figure 3. Illustration of Isolation Barrier Within the DAC1423

Figures 4 and 5 show two methods of utilizing the isolation characteristics of the DAC1423. In Figure 4, the DAC1423 is shown with separate loop supply and power supply. This configuration is useful when it is desirable to derive power for the module from the system without losing output isolation. This configuration is also useful when using external synchronization or multiple units, since the sync controls are referenced to power common. Figure 5 shows the use of a single supply for both power and loop current. This technique is useful when

the loop supply is the most secure power source, since the DAC1423 will remain operable even though the system has failed, as long as the loop supply continues to operate.

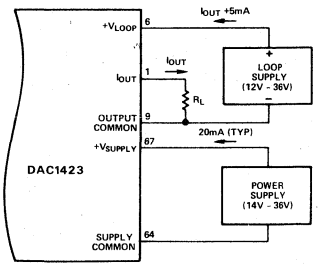


Figure 4. Operation with Isolated Loop and Power Supplies DAC1423

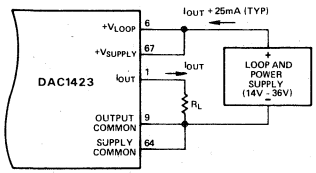


Figure 5. Operation with Common Supply DAC1423

SYNCHRONIZATION

The DAC1423 contains an internal oscillator which generates the carrier frequency for the modulation process. In most cases, there is no appreciable leakage from this oscillator, and it may be ignored by the user. However, when a DAC1423 is used in a system which contains a clock at or near this carrier frequency, or when several DAC1423's are used adjacent to one another, it is possible that a heterodyning phenomenon can occur which results in beat notes that may (or may not) fall within the system's passband. For this reason, the DAC1423 contains provisions for external or multiple synchronization. Pin 68 is the SYNC IN pin which can be driven from an external clock. The external clock should be within 15% of free running frequency of the DAC1423 (200kHz ±15%). It should be a 5V CMOS level (50% duty cycle) via a 2200pF capacitor in series with pin 68.

If external sync is not used, leave the SYNC IN pin unconnected; the DAC1423 will free run at approximately 200kHz. Note that the SYNC IN signal is referred to power common, not loop common or digital common.

When multiple DAC1423's are used, it is recommended that their sync provisions be "daisy chained" as shown in Figure 6. The SYNC OUT pin of one DAC1423 is used as the external sync drive for the next DAC1423. Note that the first DAC1423 in the chain may either "free run" or be synchronized from an external source.

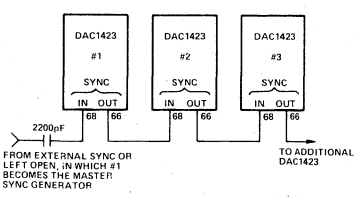


Figure 6. Synchronizing Multiple DAC1423's

The performance of the DAC1423 running in the sync mode is essentially no different from the free running mode, except that there may be slight offset and span shifts (≈1LSB) if the carrier frequency is pulled appreciably from its free running frequency. In no case should the carrier frequency be pulled more than ±15% from its nominal free running frequency.

DIGITAL INTERFACE (PARALLEL)

The parallel interface of the DAC1423 is a 5V CMOS design, arranged to offer a great deal of interfacing flexibility to a variety of user systems.

The interface consists of a 10-bit input latch, a 10-bit tri-state output, and the associated control lines for read and write operations. As shown in Figure 7, the 8 lower bits and 2 upper bits of both the latch and the tri-state are separately controlled, allowing interfaces to both 8-bit and 16-bit bus architectures. For 10-bit or greater bus operation, the LO and HIGH write lines may be connected together, as well as the LO and HIGH read lines.

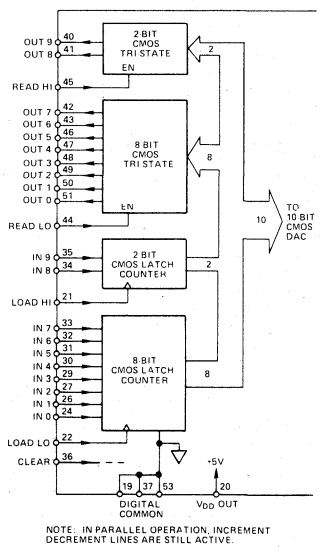


Figure 7. DAC1423 Digital Interface Architecture

An example of an 8-bit microprocessor interface is shown in Figure 8. In this case, the data is arranged as two bytes, right justified. The digital inputs to the DAC1423 are CMOS, therefore, rigid logic levels are required. In some cases, double buffering may be required for bus interface.

The output drive capability of the tri-states is 1 TTL load; in general, the DAC1423 may be used directly on most NMOS or CMOS microcomputer buses if the 3.3V minimum logic "1" level is observed. In some cases, pullups may be required.

In the event of computer failure, the bus inputs must go to either a high or a low state, but read, write and clear lines must go to a low state.

BUMPLESS TRANSFER

In process control applications, there will be times when the computer power fails and critical controls must be operated manually. To avoid causing a "bump" in the process, such as commanding a manually closed valve to fully open when switched to automatic control, it is essential that the computer knows the exact condition of the system when it resumes control. This is known as "bumpless transfer".

Bumpless transfer, when switching between automatic and manual control, is provided by the readback capability of the ISO-DAC's output tri-state logic. It constantly monitors the status of the input register; therefore, when switching from manual to automatic control, the computer can read the status of the ISO-DAC before resuming the algorithm.

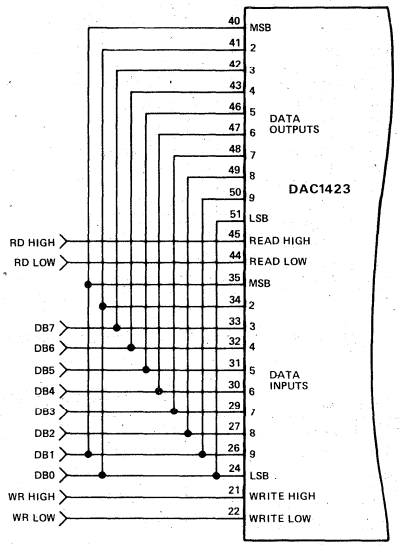


Figure 8. Typical Interface to 8-Bit µComputer

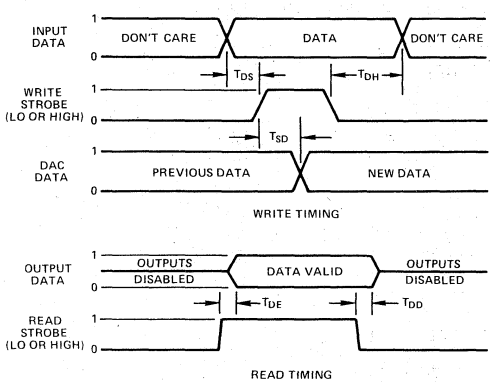


Figure 9. Read/Write Timing

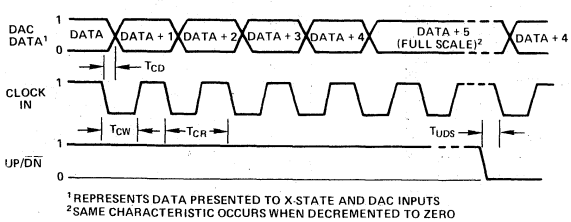


Figure 10. Increment/Decrement Timing

SYMBOL	MEANING	MIN	TYP	MAX	UNITS
t_{SD}	Strobe to Data Time	–	315	–	ns
t_{DS}	Data Set-Up Time	0	–	–	ns
t_{DH}	Data Hold Time	–	100	–	ns
t_{WS}	Write Strobe Width	–	100	–	ns
t_{OE}	Output Enable Time	–	100	–	ns
t_{OD}	Output Disable Time	–	80	–	ns
t_{CD}	Clock to Data Time	–	315	–	ns
t_{CW}	Clock Width	–	200	–	ns
t_{UDS}	Up/Down Set-Up Time	–	250	–	ns
t_{CR}	Clock Repetition Period	–	–	330	ns

Table 2. Timing Requirements

INCREMENT/DECREMENT CONTROL

Increment/decrement operation under computer or manual control is possible with the input latch/counter in the DAC1423. The DAC1423 also contains overflow/underflow lockout circuitry, and a slow speed clock output is provided. The timing diagram shown in Figures 9 and 10 give guidelines for increment/decrement operation. Figure 11 shows the ISO-DAC in the manual back-up mode using increment/decrement control logic. In this circuit, part of Z_1 latches the direction line, UP/$\overline{DN}$. Z_2 and the remainder of Z_1 gate the clock "on"—after one RC time delay. The RC time delay is determined by R_T and C_T which the user supplies. The same circuit could be used for computer control by simply replacing the pushbutton switch with the proper logic.

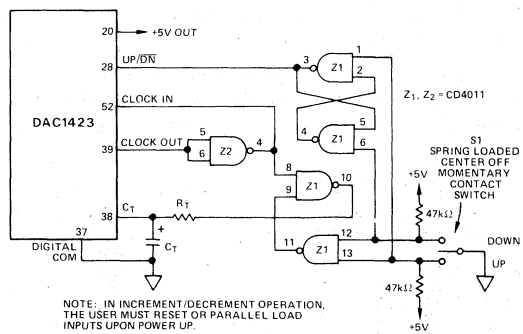


Figure 11. Increment/Decrement Control

SLOW CLOCK OPERATION

The DAC1423 provides a slow speed clock circuit for the user's convenience in operating the increment/decrement feature. This clock requires a resistor and capacitor to set its operating frequency, as shown in Figure 12. When the slow clock is not used, connect pin 38 to digital common (pin 37) and disable the slow clock to prevent any feed-through of the clock signal to the output.

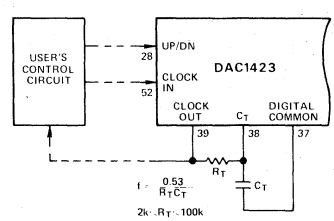


Figure 12. Using the Slow Clock

CLEAR

In many industrial controls, it is desirable to have the ISO-DAC go to a known state when the system is first powered up. The clear pin, pin 36, is provided for just such cases. Strobing the clear pin will reset the input latch/counter to all 0's. Tying pin 36 to the computer reset bus provides an asynchronous means to initiate the system to a known state.

+5V OUTPUT

A +5V output is provided for powering a small amount of user supplied circuitry. This output is referred to digital common and is, therefore, isolated both from the loop and from the power supply. The outboard devices may draw up to a maximum of 0.5mA from this pin (pin 20); however, it is suggested that the user by-pass this pin to digital common with a 0.1μF or greater capacitor in order to avoid externally injected glitches from disturbing the internal circuitry of the DAC1423.

AC1582 MOUNTING CARD

The AC1582 mounting card is available to assist in evaluating the DAC1423. As shown in Figure 13, the AC1582 is an edge connector card with pin receptacles for plugging in the DAC1423. This card includes offset and span adjustment potentiometers, power supply bypass capacitors and the logic needed for increment/decrement control. Increment/decrement control is enabled via connection to J2. In addition, the card allows for several user-selectable configurations:

1. 8- or 16-bit bus interface;
2. Single supply for both power and loop current. Supply delivered via P_1 or TB_1;
3. Separate loop supply and power supply;
4. Offset and Span—fixed or adjustable.

These configurations can be programmed by user-installed jumpers, as shown in the wiring chart of Table 3. Jumper locations are not shown in Figure 13, but are labeled on the mounting card.

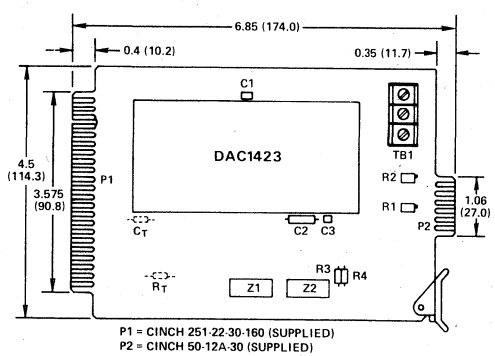


Figure 13. AC1582 Mounting Card. Dimensions shown in inches and (mm).

P1

PIN	FUNCTION	PIN	FUNCTION
1	MSB IN	A	MSB OUT
2	BIT 2 IN	B	BIT 2 OUT
3	BIT 3 IN	C	BIT 3 OUT
4	BIT 4 IN	D	BIT 4 OUT
5	BIT 5 IN	E	BIT 5 OUT
6	BIT 6 IN	F	BIT 6 OUT
7	BIT 7 IN	H	BIT 7 OUT
8	BIT 8 IN	J	BIT 8 OUT
9	BIT 9 IN	K	BIT 9 OUT
10	LSB IN	L	LSB OUT
11	WRITE HIGH	M	READ HIGH
12	WRITE LOW	N	READ LOW
13	CLEAR	P	DIGITAL COMMON
14	NC	R	$+5V_{OUT}$
15	NC	S	NC
16	NC	T	NC
17	+V POWER	U	PWR COMMON
18	SYNC IN	V	SYNC OUT
19	NC	W	NC
20	NC	X	NC
21	$+V_{LOOP}$	Y	LOOP COMMON
22	NC	Z	NC

P2

PIN	FUNCTION
A	DIG COM
B	DECREMENT
C	INCREMENT

TB1

PIN	FUNCTION
1	$+V_{LOOP}$
2	I_{OUT}
3	LOOP COMMON

Table 3. AC1582 Mounting Card Connector Designations

Options	User-Installed Jumpers[1]
8-Bit Bus Interface	J1, J2, J4, J5
16-Bit Bus Interface	J3, J6
Single Supply	J7, J8, J13, J14
Dual Supply (V_{LOOP} via P1)[2]	J13, J14
Offset and Span, Fixed	J10, J12
Offset and Span, Adjustable	J9, J11

Notes:
[1] Jumper locations are not shown in Figure 13, but are labeled on AC1582
[2] Loop supply normally accessible via TB1.

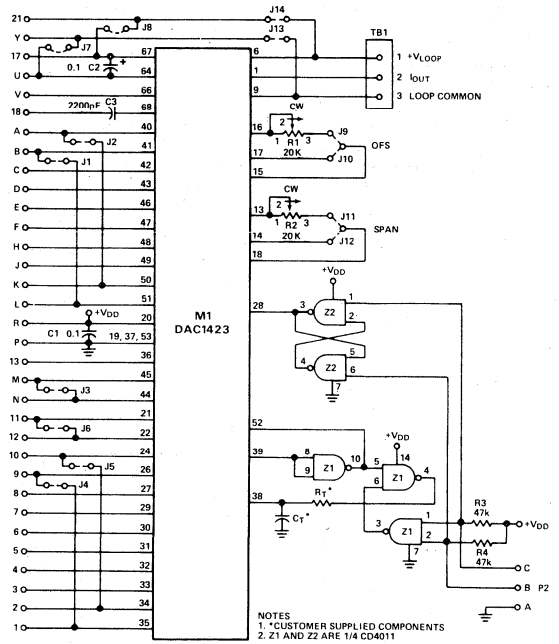


Figure 14. Schematic Diagram for AC1582 Mounting Card

Ultra High Speed Deglitched D/A Converter

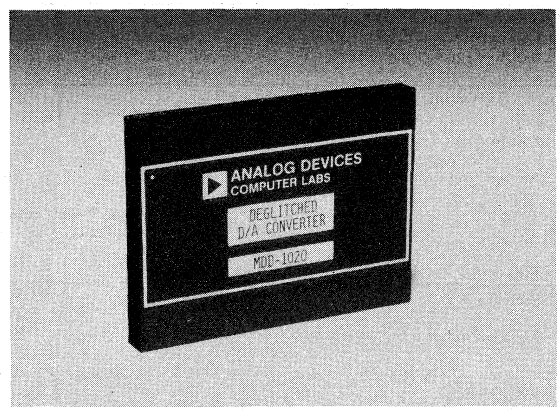
MDD SERIES

FEATURES

- Ultra-High Speed: 20MHz Word Rate
- 8- and 10-Bit Versions Available
- TTL Compatible
- Smallest Size Available: 3″ × 4″ × 0.5″
- Completely Self-Contained with Input Register, D/A, Deglitcher, Timing, Internal References, and Output Buffering

APPLICATIONS

- Color-Television Video Reconstruction, Time-Base Correction and Frame Synchronization
- Graphic Displays
- Deflection Systems
- Character Generators
- High Speed D/A Systems



GENERAL DESCRIPTION

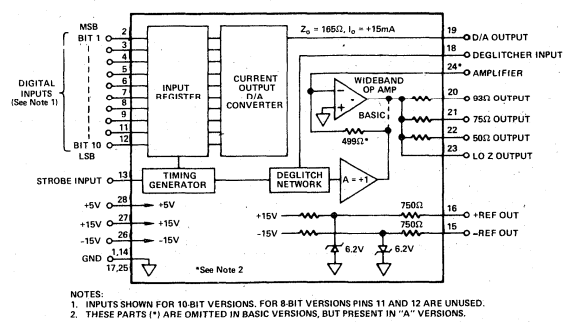
The MDD Series is a subsystem module which contains an input digital register, ultra-high speed current output D/A converter, deglitcher, output buffer amplifier, precision references, and timing circuitry within a 3″×4″×0.5″ case. The output of the device is an ultra-linear analog representation of the digital input. Requiring only external gain and offset potentiometers for final calibration, the MDD D/A solves the glitch problem associated with high-speed D/A converters. The incorporation of an internal register virtually eliminates the need for input bit time deskewing. While not totally eliminating the glitch per se, the remnant glitch is very small, and more importantly, constant (and therefore filterable) over the output range.

The MDD Series is available with 8- or 10-bit resolution and in two versions. The basic versions contain a unity gain output buffer and can deliver 2V p-p open circuit (or 1V p-p into a load) when the MDD output is both source and load terminated. The "A" versions contain a very high speed output gain amplifier to allow the MDD to deliver 4V p-p open circuit (or 2V p-p into a load) when the device is source and load terminated. Higher output voltages may be obtained—up to ±10V by external feedback resistor selection. However, settling time degradation must be expected.

TV APPLICATION

The "A" version of the MDD Series deglitched D/A is ideally suited for color television video reconstruction. Its output can directly drive the low impedances normally associated with video baseband transmission. Since the output impedance of the internal operational amplifier is less than 1Ω, the transmission-line match obtained with the internal source terminating resistor is almost perfect. Other applications include waveform generation, automatic test equipment, and fast process control systems.

Designed primarily for PC board mounting, these D/A's may also be plugged into pin sockets. The pins are 0.04″ diameter, gold plated, and are on 0.2″ centers. For increased reliability, each module is burned-in for 96 hours at +25°C before final test and shipment.



NOTES:
1. INPUTS SHOWN FOR 10-BIT VERSIONS. FOR 8-BIT VERSIONS PINS 11 AND 12 ARE UNUSED.
2. THESE PARTS (*) ARE OMITTED IN BASIC VERSIONS, BUT PRESENT IN "A" VERSIONS.

MDD Series Block Diagram

SPECIFICATIONS (typical at +25°C and nominal supply voltages unless otherwise noted)

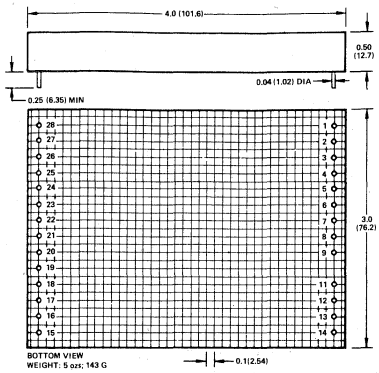
MODEL	MDD-0820 MDD-0820A	MDD-1020 MDD-1020A
RESOLUTION	8 Bits	10 Bits
Accuracy (including linearity) at Maximum Word Rate of 20MHz	±0.2%	±0.05%
Monotonicity	Guaranteed 0 to +70°C	
DIGITAL DATA BIT INPUTS		
Logic Level/Load	1 Standard "S" TTL Load	
Positive Logic—Binary (BIN)	"1" = +2.4V to +5V "0" = 0V to +0.4V	
DIGITAL STROBE INPUT		
Logic Level/Load	2 Standard "S" TTL Loads	
Positive Logic	"1" = +2.4V to +5V "0" = 0V to +0.4V	
Risetime and Falltime	10ns max	
Width	15ns min	
Timing	Negative-Going Trailing Edge to Occur a Minimum of 20ns After Last Data Bit Change	
Frequency	20MHz max	
OUTPUT	**MDD-0820 MDD-1020**	**MDD-0820A MDD-1020A**
Voltage, No Load, Unipolar	0 to +2V	Externally Programmable with Gain and Offset Resistors to ±10V max
Bipolar	+1V to −1V	
Impedance		
Pin 23, Low Z	10Ω max	1Ω max
Pin 22, 50Ω	50Ω ±5%	50Ω ±1%
Pin 21, 75Ω	75Ω ±5%	75Ω ±1%
Pin 20, 93Ω	93Ω ±5%	93Ω ±1%
Amplifier Current	±50mA for dc load = 100Ω min, dc load = $Z_{OUT} + R_{LOAD}$	
DAC Current	+15mA	
SETTLING TIME		
DAC Current Output (to 0.1%)	15ns	
Voltage Output	50ns to 0.1% 2V p-p	120ns to 0.1% 4V p-p
RESIDUAL GLITCH[1]	30mV for 2V p-p F.S. Output or 1.5% of F.S.	
PEDESTAL	10mV for 2V p-p F.S. Output or 0.5% of F.S.	
OUTPUT ZERO OFFSET	Adjustable to Zero	
OUTPUT ZERO OFFSET vs. TEMP	100ppm/°C	
GAIN	Adjustable	
REFERENCES AVAILABLE	±6.2V	
POWER REQUIREMENTS		
+15V ±3%	120mA	
−15V ±3%	150mA	
+5V ±5%	250mA	
Power Supply Rejection Ratio	0.1%/V	
CASE	Diallyl Phthalate (per MIL-M-14 type SDG-F)	
TEMPERATURE RANGE		
Operating	0 to +70°C	
Storage	−55°C to +85°C	

[1] Occurs at the update rate.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	GROUND*	15	-REF OUT
2	BIT 1 INPUT (MSB)	16	+REF OUT
3	BIT 2 INPUT	17	GROUND*
4	BIT 3 INPUT	18	DEGLITCHER INPUT
5	BIT 4 INPUT	19	D/A OUTPUT
6	BIT 5 INPUT	20	93Ω OUTPUT
7	BIT 6 INPUT	21	75Ω OUTPUT
8	BIT 7 INPUT	22	50Ω OUTPUT
9	BIT 8 INPUT	23	LO Z OUTPUT
10	NC	24	AMP FEEDBACK
11	BIT 9 INPUT	25	GROUND*
12	BIT 10 INPUT (LSB)	26	-15V POWER INPUT
13	STROBE INPUT	27	+15V POWER INPUT
14	GROUND*	28	+5V POWER INPUT

*ALL GROUNDS INTERNALLY CORRECTED

NOTES ON "DEGLITCHING"

An MDD Series D/A converter operating with a full-scale p-p analog output of 1V will typically have a glitch, or transient, in its output which is 15mV in amplitude and is 25ns wide, at the 50% points. These typical values are independent of whether the D/A converter is an 8-bit unit or a 10-bit unit.

This glitch remains constant, regardless of the transition points. In other words, it is the same for the transition from 0000000001 to 1000000000 as it is for the transition from 1000000000 to 1000000001 or any other two input words.

A constant glitch is the purpose of the deglitcher circuits. They are intended to hold the area under the curve at a constant value; they are not intended to get rid of all glitches per se.

When the area under the transient curve is held constant, the frequency spectrum of the glitch is a fine line; i.e., a single-line spectrum at the sample rate frequency, and harmonics of the sample frequency.

If the glitch is a function of signal dynamics, as it is in the case of a D/A converter output which is not deglitched, a multitude of intermodulation products are formed. Some of these IM products appear in the video pass-band as spurious signals and increased noise level. The deglitcher circuits effectively eliminate these products. When they do, the S/N ratio approaches that of an ideally-quantized signal, where the rms noise is $Q/\sqrt{12}$, when frequencies above Nyquist are filtered out.

In summary then:

- The residual glitch for an MDD Series D/A converter is typically 15mV for a full-scale 1V p-p output; this is 1.5% of F.S.
- The glitch width is typically 25ns at the 50% points.
- The amplitude and width of the glitch are constant, and independent of:
  - —the magnitude of change in successive transitions
  - —number of bits of digital output
  - —input (update) data rates

D/A converters without deglitching circuits (such as the Analog Devices' MDS/MDP D/A units) have smaller, shorter glitches, on the average; but this type of converter has larger glitches at the major crossings, especially at the mid-scale transition.

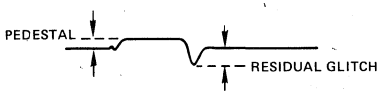


Figure 1. Pedestal/Glitch Relationship

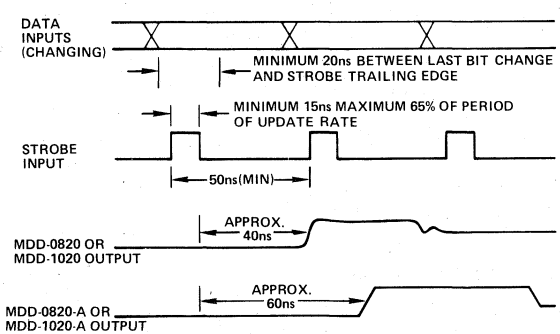


Figure 2. MDD Series Timing Diagram

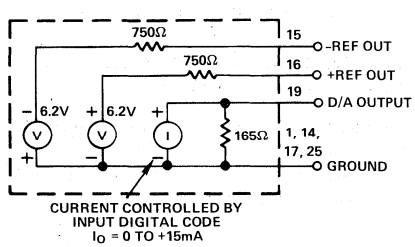


Figure 3. D/A Current Equivalent Circuit

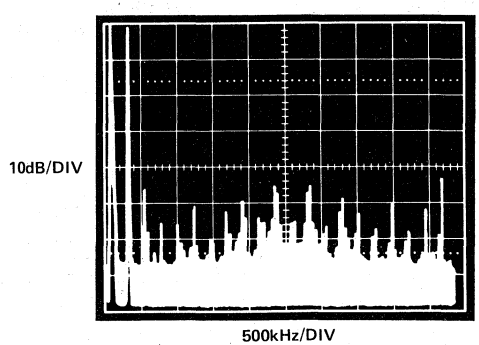


Figure 4. Spectrum of 10-bit D/A Operating at 11MHz Update Rate Without Deglitching — Unfiltered

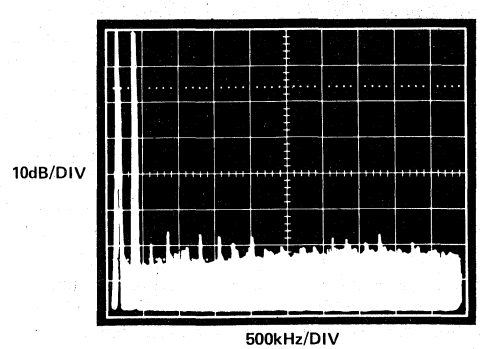


Figure 5. Spectrum of 10-bit D/A Operating at 11MHz Update Rate With Deglitching — Unfiltered

10

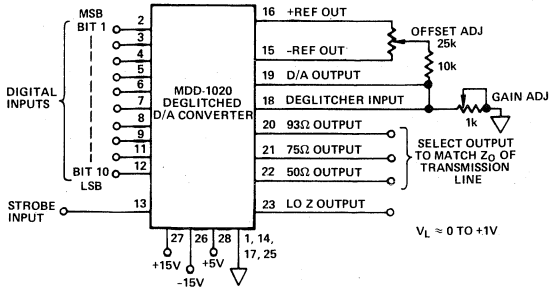


Figure 6. Unipolar Output Configuration Basic Versions

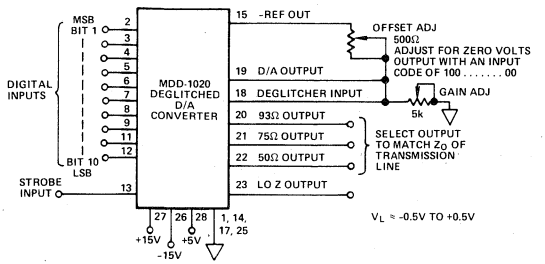
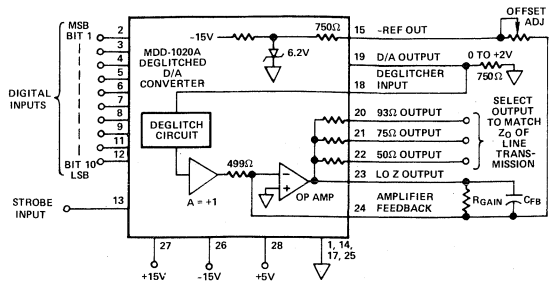


Figure 7. Bipolar Output Configuration Basic Versions



NOTES:
1. SELECT R_{GAIN} TO GIVE DESIRED OPEN CIRCUIT OUTPUT VOLTAGE. THE INPUT VOLTAGE TO THE OP AMP IS APPROXIMATELY 0 TO +2V. THE OUTPUT OF THE OP AMP IS THEREFORE ((2 × R_{GAIN})/500Ω) VOLTS p-p.
2. THE LOGIC IS INVERTED INTERNALLY FOR THE "A" VERSIONS SUCH THAT ALL "1'S" AT THE DIGITAL INPUTS YIELDS A FULL-SCALE POSITIVE VOLTAGE AT THE OP AMP OUTPUT.
3. FOR POSITIVE UNIPOLAR OPERATION, THE NOMINAL OFFSET POTENTIOMETER RESISTANCE SHOULD BE SET FOR A VALUE OF APPROXIMATELY 800Ω, MAKING A 2000Ω POTENTIOMETER IDEAL.
4. FOR BIPOLAR OPERATION, THE NOMINAL OFFSET POTENTIOMETER RESISTANCE SHOULD BE SET FOR A VALUE OF APPROXIMATELY 2300Ω, MAKING A 5000Ω POTENTIOMETER IDEAL. THE OUTPUT VOLTAGE SHOULD BE ADJUSTED FOR ZERO WITH AN INPUT CODE OF 10 . . . . . 00.
5. MAKE C_{FB} NOMINALLY 10pF. SELECT FOR OPTIMUM SETTLING TIME IF DESIRED.
6. IF ADJUSTABLE GAIN IS DESIRED, ADD A LOW-VALUE, LOW-INDUCTANCE CERMET TRIMMING POTENTIOMETER IN SERIES WITH R_{GAIN}. BY PUTTING THE GAIN ADJUSTMENT HERE, THE GAIN AND OFFSET ADJUSTMENTS ARE INDEPENDENT OF EACH OTHER.

Figure 8. Output Configuration — "A" Versions

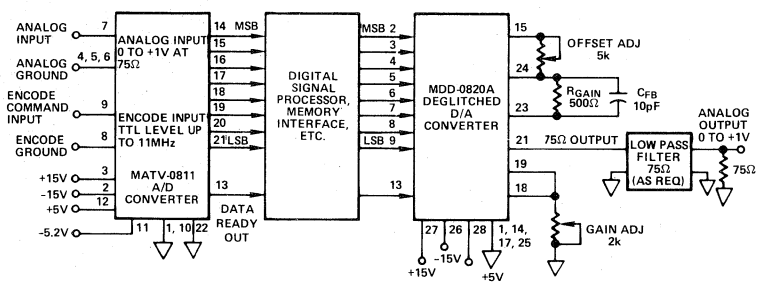


Figure 9. Typical A/D-D/A Back-to-Back Connections for Video Applications or Testing

The typical video differential phase and gain errors (disregarding quantization effects) for the configuration shown are 3° and 3%, respectively, using an encode command frequency of three times the NTSC color subcarrier (10.74MHz). For applications requiring digitization at frequencies of four times NTSC (14.32MHz) or three times PAL (13.29MHz) the MATV-0816 A/D Converter should be substituted. For applications requiring digitization at four times PAL (17.74MHz), the MATV-0820 A/D Converter should be substituted. Results are applicable for either NTSC or PAL test signals using the 20 IRE modulated ramp.

Due to the inherently stable characteristics of the output operational amplifier, the "A" versions are recommended for driving properly terminated video terminated lines.

ORDERING INFORMATION

For 8-Bit Models, Order:	MDD-0820 without output amplifier MDD-0820A with output amplifier
For 10-Bit Models, Order:	MDD-1020 without output amplifier MDD-1020A with output amplifier

Mating pin socket connectors for the MDD Series is model MSB-2. Prototyping socket is MSD-1.

The MDD Series D/A's are normally burned-in at +25°C for a minimum of 96 hours. For extended burn-in, consult the factory. All of Analog Devices' data acquisition products are covered by a one-year warranty.

Ultra High Speed Multiplying D/A Converter

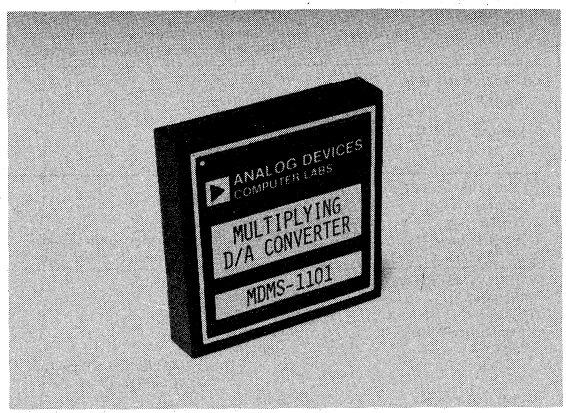
MDMS SERIES

FEATURES

- **Small Size: 2″ X 2″ X 0.4″**
- **Highest Speed Available**
- **High Multiplying Accuracy: Maintains Monotonicity and Linearity for any Analog Input within the Specified Range**
- **High Current Output: 10mA Full Scale**
- **High Reliability, Hybrid Microcircuit Construction**
- **Guaranteed Operation: -30°C to +85°C**

APPLICATIONS

- **CRT Displays**
- **Waveform Generation**
- **Vector Generation**
- **Fast Digital Attenuator**



GENERAL DESCRIPTION

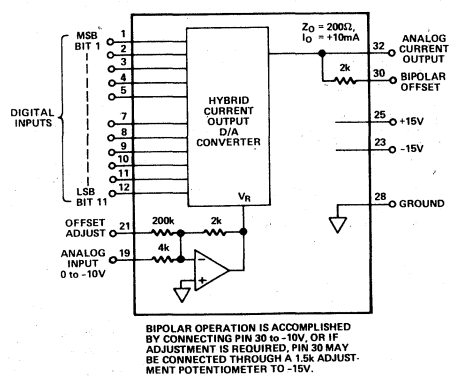
The MDMS series is an ultra-high speed, one or two-quadrant, multiplying D/A converter capable of 10MHz operation and 11-bit precision. The settling time for both analog and digital inputs is 100ns, and the large signal bandwidth of the analog input is in excess of 10MHz. The module is designed for the needs of the graphic display field and other applications requiring high-accuracy, high-speed multiplying operation.

The current output of the MDMS series D/A is precisely proportional to the analog input signal multiplied by the digital input code. The analog input signal may be any voltage between 0V and -10V, and can be a sine wave, triangle wave, sawtooth, or other waveform. The D/A output is an accurate scaled version of the input waveform, the scale factor being the digital input code. Alternatively, the analog input voltage may be used to scale a digitally generated signal. Various offsetting provisions are made so that the analog signal, digital signal, and output may be made bipolar or unipolar in order to accommodate various uses requiring one or two-quadrant operation.

The output impedance of the D/A is 200 ohms so that a two-volt output swing is possible with no load. Loading the output with 200 ohms results in a 1 volt p-p output. If an external operational amplifier such as the Analog Devices' HOS-050 Op Amp is connected to the output of the D/A, output voltages up to 20V p-p are obtainable at a small sacrifice in speed.

ORDERING INFORMATION

Order Model Number MDMS-0801, MDMS-1001, or MDMS-1101. Ruggedized versions with extended burn-in are also available. Consult the factory.



MDMS Series - Block Diagram

SPECIFICATIONS (typical @ +25°C and nominal power supply voltages unless otherwise noted)

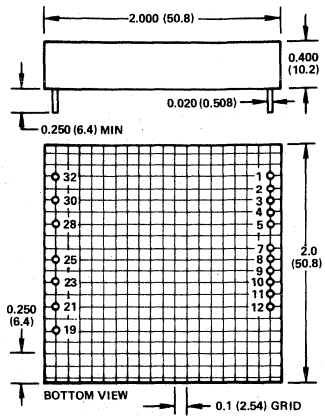
MODEL	MDMS-0801	MDMS-1001	MDMS-1101
RESOLUTION	8 Bits	10 Bits	11 Bits
LSB Weight	40μA	10μA	5μA
ACCURACY (ADJUSTABLE TO)	±0.2%	±0.05%	±0.025%
Monotonicity	Guaranteed	*	*
Linearity	20μA, ±1/2LSB	5μA, ±1/2LSB	2.5μA, ±1/2LSB
ANALOG INPUT			
Voltage Range	0 to -10V	*	*
Impedance	4kΩ ±2%	*	*
Transfer Function (inverting)	0V input scales D/A output to minimum output; -10V input scales D/A output to maximum output.		
DIGITAL INPUT (TTL)			
Positive Logic, "1" =	+2.4V to +5.0V	*	*
"0" =	0V to 0.4V	*	*
Loading, 2 Std. TTL Loads			
"0" =	-5mA	*	*
"1" =	50μA	*	*
CODING (PARALLEL INPUT DATA)			
Unipolar	BIN	*	*
Bipolar	OBN	*	*
All "1's" Input	Maximum Positive Output		
All "0's" Input	Maximum Negative Output		
OUTPUT (CURRENT)			
Unipolar	0 to +10mA	*	*
Bipolar	±5mA	*	*
Compliance Voltage	+1.5V, -2V	*	*
Impedance	200Ω, ±1%	*	*
Loading	200Ω for 0 to 1V p-p Out; 0Ω for 0 to 2V p-p Out		
Zero Offset (max)	50nA	*	*
DYNAMIC CHARACTERISTICS			
Settling Time (digital & analog)	90ns to 0.2% F.S.	100ns to 0.1% F.S.	130ns to 0.05% F.S.
Bandwidth (analog in)	10MHz	*	*
TEMPERATURE COEFFICIENTS			
Linearity	2ppm/°C	*	*
Monotonicity	Guaranteed -30°C to +85°C		
POWER REQUIREMENTS			
+15V ±10%	60mA	*	*
-15V ±10%	20mA	*	*
Power Supply Rejection Ratio	0.005%/V	*	*
TEMPERATURE RANGE			
Operating	-30°C to +85°C		
Storage	-55°C to +125°C		
PHYSICAL CHARACTERISTICS			
Case	Diallyl Phthalate per MIL-M-14 Type SDG-F		

*Specifications same as MDMS-0801

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTE: DOT ON TOP INDICATES POSITION OF PIN 1

WEIGHT: 1.6 OZ, 45.3 G

PINS ARE GOLD PLATED PER MIL-G-5204 TYPE II

MATING SOCKET MSA-1

PIN DESIGNATIONS

PIN	FUNCTION
1	BIT 1 INPUT (MSB)
2	BIT 2 INPUT
3	BIT 3 INPUT
4	BIT 4 INPUT
5	BIT 5 INPUT
7	BIT 6 INPUT
8	BIT 7 INPUT
9	BIT 8 INPUT
10	BIT 9 INPUT
11	BIT 10 INPUT
12	BIT 11 INPUT LSB
19	ANALOG INPUT
21	OFFSET ADJ
23	-15V POWER INPUT
25	+15V POWER INPUT
28	GROUND
30	BIPOLAR OFFSET
32	ANALOG OUTPUT

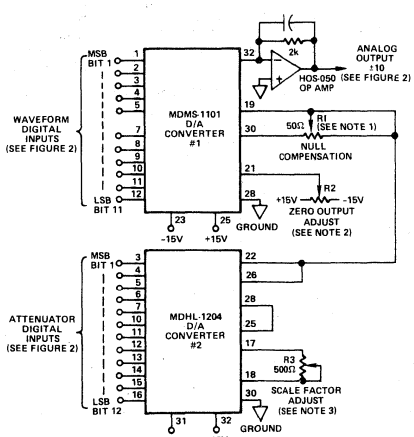
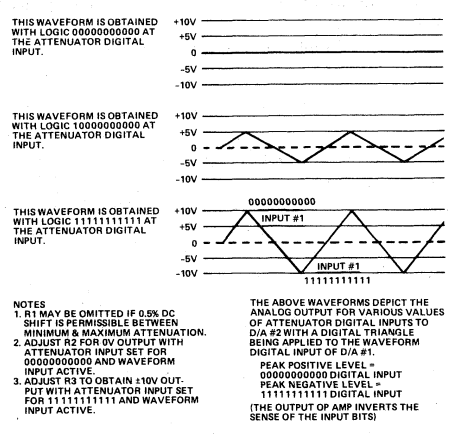


Figure 1. The MDMS-1101 Multiplying D/A Used as a Digital Waveform Generator with Digital Attenuator Control



NOTES

1. R1 MAY BE OMITTED IF 0.5% DC SHIFT IS PERMISSIBLE BETWEEN MINIMUM & MAXIMUM ATTENUATION.
2. ADJUST R2 FOR 0V OUTPUT WITH ATTENUATOR INPUT SET FOR 00000000000 AND WAVEFORM INPUT ACTIVE.
3. ADJUST R3 TO OBTAIN ±10V OUTPUT WITH ATTENUATOR INPUT SET FOR 11111111111 AND WAVEFORM INPUT ACTIVE.

THE ABOVE WAVEFORMS DEPICT THE ANALOG OUTPUT FOR VARIOUS VALUES OF ATTENUATOR DIGITAL INPUTS TO D/A #2 WITH A DIGITAL TRIANGLE BEING APPLIED TO THE WAVEFORM DIGITAL INPUT OF D/A #1.

PEAK POSITIVE LEVEL = 00000000000 DIGITAL INPUT
PEAK NEGATIVE LEVEL = 11111111111 DIGITAL INPUT

(THE OUTPUT OP AMP INVERTS THE SENSE OF THE INPUT BITS)

Figure 2. Operation of Multiplying D/A Circuit

ANALOG DEVICES

8-, 10-, 12-Bit Video Speed Current and Voltage Out, D/A Converters

MDS/MDSE/MDSL/MDH SERIES

FEATURES
- Current Settling Times to 15ns
- ±1.5V Compliance
- Voltage Settling Times to 100ns (MDH)
- Monotonicity Guaranteed Over Temperature
- High Output Currents — 15mA
- -30°C to +85°C Operating Range
- Industry Standard Pin Outs
- 20V, p-p Out (MDH)
- TTL or ECL Logic

APPLICATIONS
- CRT Vector Displays
- Digitial Waveform Generation
- Automatic Test Equipment
- TV Picture Reconstruction



GENERAL DESCRIPTION

This broad family of digital-to-analog converters represents the "state of the art" in modular, high speed, voltage and current output devices. The family consists of a total of 11 devices in 4 series (MDS, MDSE, MDSL and MDH) that allow the user to make engineering trade-offs between resolution, speed, output and logic type. The first 3 are high compliance current output units which make possible linear output swings greater than ±1.5V. The voltage output MDH series contain a fast settling hybrid operational amplifier which provides ±10V output at ±50mA. To simplify selection these major specifications are summarized in Table 1.

MODEL	BITS	FULL SCALE OUTPUT	FULL SCALE SETTLING TIME	INPUT LOGIC
		(Fastest Settling High Current Out)		
MDS-0815	8	15mA	15ns to 0.4% FS	TTL
MDS-1020	10	15mA	20ns to 0.1% FS	TTL
MDS-1240	12	15mA	40ns to 0.025% FS	TTL
		(MDS with ECL Logic)		
MDS-0815E	8	15mA	15ns to 0.4% FS	ECL
MDS-1020E	10	15mA	20ns to 0.1% FS	ECL
		(Low Current MDS)		
MDSL-0825	8	5mA	25ns to 0.1%	TTL
MDSL-1035	10	5mA	25ns to 0.1%	TTL
MDSL-1250	12	5mA	50ns to 0.025%	TTL
		(Voltage Out MDSL)		
MDH-0870	8	10V/50mA	150ns to 0.4%	TTL
MDH-1001	10	10V/50mA	200ns to 0.1%	TTL
MDH-1202	12	10V/50mA	500ns to 0.025%	TTL

Table 1.

SPEED WITH PRECISION

Analog Devices' model MDS-1240 is the first D/A converter available with highly reliable, internal hybrid construction to achieve ultra-high speed operation. In fact, it is the fastest 12-bit D/A available, settling to 0.025% in 40ns. Hybrid construction eliminates the thermal lag problem inherent in 12-bit D/A's constructed with discrete components. This in turn means that the accuracy is maintained over the total frequency range of operation, yielding superior results for frequency domain applications.

The MDS-1240 is particularly well suited for CRT display applications because of its unsurpassed speed and drive capabilities. The high output current (15mA) allows the use of low impedance loads so that settling times remain short — even with higher output voltage levels. The ability to drive load capacitance is at least 3 times that of other 12-bit D/A's thus providing capability to drive a terminated transmission line directly. The MDS-815 and MDS-1020 provide similar performance at 8 and 10 bits, while the MDS-E units provide it with ECL logic. MDSL-0825, MDSL-1035 and MDSL-1250 also utilize this reliable hybrid construction. The use of laser trimmed resistor networks within the D/A's not only eliminates thermal time lag errors but provide the linearity tempco of 2ppm/°C; guaranteeing monotonic operation over the extended temperature range of -30°C to +85°C. The power dissipation of the MDSL series is one-half that of competitive D/A's, but a full 5mA output current is maintained. This allows driving transmission lines or other low impedance loads directly.

Each D/A is housed in industry standard size cases, and each has an internal precision reference. Bipolar operation is achieved by external pin interconnection. In normal circumstances, no external components are required for operation into low impedance loads. Designed primarily for PCB mounting, these D/A's may also be plugged into standard DIL sockets mounted on 1.8″ centers (MDS series 2″ centers).

For ultra-high reliability, this D/A series is optionally available with burn-in extended beyond the Analog Devices standard of 96 hours at +25°C.

SPECIFICATIONS (typical @ +25°C unless otherwise specified)

MODEL	UNITS	CURRENT OUTPUT MDS 0815	MDS 1020	MDS 1240	CURRENT OUTPUT MDS-E (ECL) 0815	MDS-E (ECL) 1020
RESOLUTION	Bits	8	10	12	8	10
LSB (Weight)	μA	58.6	14.6	3.66	58.6	14.6
ACCURACY						
Initial (Adjust to 0)	±%FS	0.2	0.05	0.012	0.2	0.05
Linearity (Integral)	LSB max	±1/2	*	*	*	*
Monotonicity		Guaranteed Over Operating Temp Range			*	*
Zero Offset (Adjust to 0)		15nA max	*	*	*	*
TEMPERATURE COEFFICIENTS						
Linearity	ppm/°C	5	*	2	*	2
Gain	ppm/°C	30	*	20	*	*
Offset (Bipolar)	ppm/°C	15	*	*	*	*
STABILITY WITH TIME	±%/yr max	0.5	*	*	*	*
DATA INPUTS						
Logic Compatability		TTL	*	*	ECL	ECL
Logic Voltage Levels						
Bit On Logic "1"	V	+2 to +5.0	*	*	-0.9	-0.9
Bit Off Logic "0"	V	0 to +0.4	*	*	-1.7	-1.7
Logic Current (Each Bit)						
Bit On Logic "1"	μA	⩽50	*	*	*	*
Bit Off Logic "0"	mA	-8	*	-5 max	*	*
MSB	mA	N/A	*	-10 max	*	*
Coding		All Units Binary (BIN) for Unipolar,			*	*
		Offset Binary (OBN) for Bipolar			*	*
OUTPUT						
Current Range						
Unipolar	mA	0 to +15	*	*	0 to -15	0 to -15
Bipolar	mA	±7.5	*	*	*	*
Impedance (See Figure 3)	Ω	165	*	200 ±1%	*	*
Compliance (MDH V_{OUT})	V	+1.5, -2	*	*	-1.5, +2	-1.5, +2
Load Resistance for V_{OUT} (See Figure 5)						
0 to +1V	Ω	112	*	100	*	*
±1V	Ω	4.32k	*	750	*	*
INTERNAL REFERENCE VOLTAGE OUT	V	N/A	*	-6.2 ±5%	*	*
SETTLING TIME[2]						
Current	ns to %	15 to 0.4[3]	20 to 0.1[3]	20 to 0.1[3] 40 to 0.025	*	20 to 0.1[3]
Unipolar Voltage (R_L = 300Ω ‖ 10pF)	ns to %					
Bipolar Voltage (R_L = 2325Ω ‖ 10pF)	ns to %					
POWER REQUIREMENTS						
Range	V	±11 to ±16	*	±14.5 to ±16.5	*	*
Current at Nominal +V	mA max	105	120	55	*	120
Current at Nominal -V	mA max	15	*	20	*	*
POWER SUPPLY REJECTION RATIO	%/V	0.04	*		*	*
+15V	%/V			-0.0001		
-15V (Bipolar)	%/V			-0.002		
-15V (Unipolar)	%/V			-0.2		
TEMPERATURE RANGE						
Operating	°C	-20 to +75	*	-30 to +85	*	*
Storage	°C	-55 to +85	*	-55 to +125	*	*
CASE		Diallyl Phthalate per MIL-M-14 Type SDG-F			*	*

*Specifications same as MDS-0815.

NOTES:

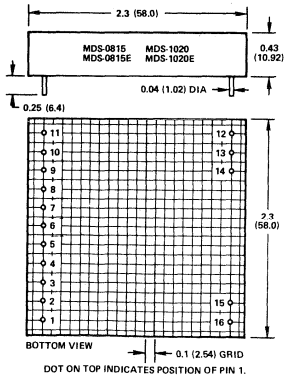
[1] 1ppm/°C for current output. Op amp is 50μV/°C.
[2] For Full Scale Step, worst case.
[3] For the MDS and MDS-E series, the voltage and current output settling times are the same if the DAC's are operated with a load to give 1V p-p output.
[4] 0 to +5V Out
[5] 0 to +10V Out
[6] ±5V Out

Specifications subject to change without notice.

CURRENT OUTPUT MDSL			VOLTAGE OUT MDH		
0825	**1035**	**1250**	**0870**	**1001**	**1202**
8	10	12	8	10	12
19.6	4.88	1.22	Depends on V_{OUT}		
0.2	0.05	0.012	0.2	0.05	0.012
*	*	*	*	*	*
*	*	*	*	*	*
*	*	*	10mV	10mV	10mV
2	2	2	2	2	2
20	20	20	20	20	20
*	*	*	See Note 1		
*	*	*	*	*	*
*	*	*	*	*	*
*	*	*	*	*	*
*	*	*	*	*	*
*	*	*	*	*	*
-1.6	-1.6	-1.6	-1.6	-1.6	-1.6
*	*	*	*	*	*
*	*	*	*	*	*
*	*	*	*	*	*
0 to +5	0 to +5	0 to +5	±50 max	±50 max	±50 max
±2.5	±2.5	±2.5	±50 max	±50 max	±50 max
600 ±1%	600 ±1%	600 ±1%	0.1 max	0.1 max	0.1 max
*	*	*	±10	±10	±10
300	300	300	N/A	N/A	N/A
2.325k	2.325k	2.325k	N/A	N/A	N/A
-6.2 ±5%	-6.2 ±5%	-6.2 ±5%	-6.2 ±5%	-6.2 ±5%	-6.2 ±5%
25 to 0.1	25 to 0.1	50 to 0.025	15 to 0.2	25 to 0.10	50 to 0.025
45 to 0.4	70 to 0.1	70 to 0.1	70 to 0.4[4]	100 to 0.1[4]	200 to 0.025[4]
70 to 0.1	80 to 0.05	90 to 0.025	150 to 0.4[5]	200 to 0.1[5]	400 to 0.025[5]
75 to 0.4	100 to 0.1	100 to 0.1	100 to 0.4[6]	130 to 0.1[6]	250 to 0.025[6]
100 to 0.1	110 to 0.05	125 to 0.025			
±12 to ±15	±12 to ±15	±12 to ±15	±14.5 to ±16.5	±14.5 to ±16.5	±14.5 to ±16.5
26	26	26	50	50	50
16	16	16	35	35	35
0.0001	0.0001	0.0001	0.003	0.003	0.003
0.001	0.001	0.001	0.01	0.01	0.01
0.2	0.15	0.15	0.15	0.15	0.15
-30 to +85	-30 to +85	-30 to +85	-30 to +85	-30 to +85	-30 to +85
-55 to +125	-55 to +125	-55 to +125	-55 to +125	-55 to +125	-55 to +125
*	*	*	*	*	*

MDS-0815, 0815E, 1020, 1020E OUTLINE DIMENSIONS

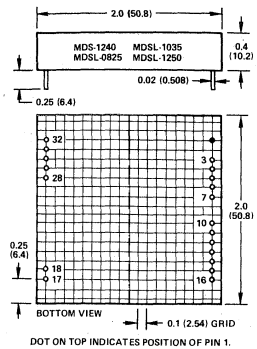
Dimensions shown in inches and (mm).



MATING SOCKET MSB-1

MDS-1240, MDSL-0825, 1035, 1250 OUTLINE DIMENSIONS

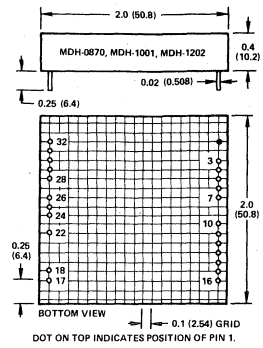
Dimensions shown in inches and (mm).



MATING SOCKET MSA-1

MDH-0870, 1001, 1202 OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



MATING SOCKET MSA-1

PIN DESIGNATIONS MDS-0815E, 1020E

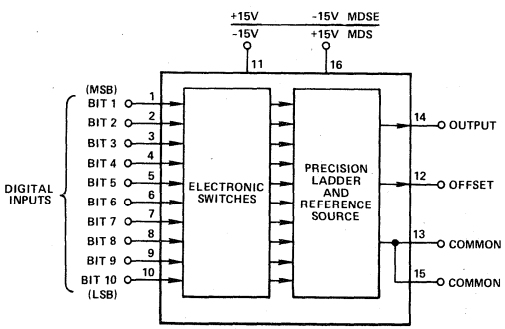
PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	9	BIT 9
2	BIT 2	10	BIT 10
3	BIT 3	11	+15V
4	BIT 4	12	OFFSET
5	BIT 5	13	COMMON
6	BIT 6	14	OUTPUT
7	BIT 7	15	COMMON
8	BIT 8	16	-15V

PIN DESIGNATIONS MDS-0815, MDS-1020

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	9	BIT 9
2	BIT 2	10	BIT 10
3	BIT 3	11	-15V
4	BIT 4	12	OFFSET
5	BIT 5	13	COMMON
6	BIT 6	14	OUTPUT
7	BIT 7	15	COMMON
8	BIT 8	16	+15V

PIN DESIGNATIONS MDS-1240, MDSL-0825, 1035, 1250

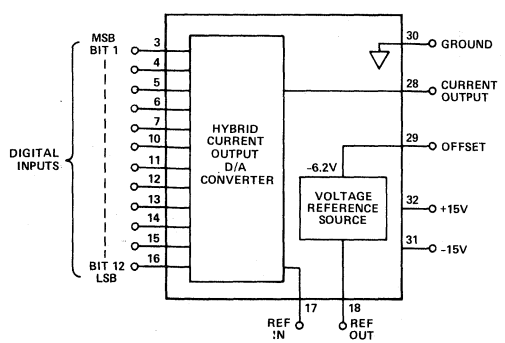
PIN	FUNCTION	PIN	FUNCTION
3	BIT 1 INPUT (MSB)	15	BIT 11 INPUT
4	BIT 2 INPUT	16	BIT 12 INPUT
5	BIT 3 INPUT	17	REFERENCE INPUT
6	BIT 4 INPUT	18	REFERENCE OUTPUT
7	BIT 5 INPUT	28	ANALOG OUTPUT
10	BIT 6 INPUT	29	OFFSET
11	BIT 7 INPUT	30	GROUND
12	BIT 8 INPUT	31	-15V POWER INPUT
13	BIT 9 INPUT	32	+15V POWER INPUT
14	BIT 10 INPUT		



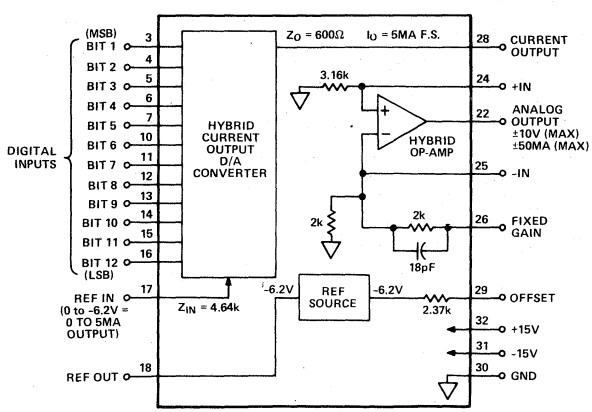
MDS and MDSE Block Diagram

PIN DESIGNATIONS MDH-0870, 1001, 1202

PIN	FUNCTION	PIN	FUNCTION
3	BIT 1 INPUT (MSB)	17	REFERENCE INPUT
4	BIT 2 INPUT	18	REFERENCE OUTPUT
5	BIT 3 INPUT	22	ANALOG OUTPUT
6	BIT 4 INPUT	24	+INPUT
7	BIT 5 INPUT	25	-INPUT
10	BIT 6 INPUT	26	FIXED GAIN
11	BIT 7 INPUT	28	CURRENT OUTPUT
12	BIT 8 INPUT	29	OFFSET
13	BIT 9 INPUT	30	GROUND
14	BIT 10 INPUT	31	-15V POWER INPUT
15	BIT 11 INPUT	32	+15V POWER INPUT
16	BIT 12 INPUT		



MDS-1240 and MDSL Series Block Diagram



MDH Series Block Diagram

Analog-to-Digital Converters

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•New product since *1980 Data-Acquisition Components and Subsystems Catalog*

11

Selection Guide
Analog-to-Digital Converters

HIGH PERFORMANCE/HIGH RESOLUTION FEATURE SELECTION CHART

		GENERAL PURPOSE				μP BUS COMPATIBLE		MULTI-CHAN	HIGH PERFORMANCE				μP BUS COMPATIBLE			HIGH RESOLUTION	
		AD570	AD571	AD ADC80	AD673	AD573	AD7574	AD7581	AD5200	AD5210	AD572	AD574A	AD7550	AD7552	AD7555	ADC1130/ ADC1131	ADC1140
Resolution	8 Bits	•			•		•	•									
	10 Bits		•			•											
	12 Bits			•					•	•	•	•					
	13 Bits												•	•		•	
	14 Bits																•
	16 Bits																
	4 1/2 Digits														•		
	5 1/2 Digits														•		
Conversion Time	1800ms																
	50ms												•	•			
	66.6μs/ch							•							•		
	50μs								•								•
	25μs	•	•	•	•	•				•	•	•				•	
	15μs						•			•						•	
Internal Reference		•	•	•	•	•			•	•	•	•				•	•
Ratiometric Capability							•	•	•	•			•	•	•		
Low Power							•	•					•	•	•		
Second Source				•					•	•							
Logic Compatibility	TTL	•	•	•	•	•		•	•	•	•	•	•	•		•	•
	CMOS		•				•	•					•	•	•		
Operating Temperature Ranges	C = 0 to +70°C	•	•		•	•	•	•				•			•	•	•
	I = -25°C to +85°C			•			•	•	•	•	•		•	•	•		•
	M = -55°C to +125°C	•	•		•	•	•		•	•	•	•					
Dice Availability		•	•			•											
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HIGH SPEED/VIDEO FEATURE SELECTION CHART

		HIGH SPEED											VIDEO				
		AD579	AD578	AD ADC84/85[1]	AD5240[1]	HAS-0802	HAS-1002	HAS-1202	MAH-0801	MAH-1001	MAS-1202	MATV-0811[2]	MATV-0816[2]	MATV-0820	MOD-1005[2]	MOD-1020[2]	MOD-1205[2]
Resolution	8 Bits	•				•			•			•	•	•			
	10 Bits		•	•			•			•					•	•	
	12 Bits		•	•	•			•			•						•
Conversion Time	⩽8μs		•	•	•	•	•		•	•	•						
	⩽3μs	•	•			•	•	•	•	•	•						
	⩽1.1μs								•	•							
Word Rate	⩾5MHz											•			•		•
	⩾16MHz												•	•		•	
Internal Reference		•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
Logic Compatibility	TTL	•	•	•	•	•	•	•	•	•	•	•	•	•	•		•
	ECL															•	
Operating Temperature Ranges	C = 0 to +70°C	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	I = -25°C to +85°C			•		•	•	•									
	M = -55°C to +125°C	•	•	•	•												
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[1] Second Source
[2] Complete with Track and Hold.

Orientation
Analog-to-Digital Converters

FACTORS IN CHOOSING AN A/D CONVERTER

In the two volumes of this catalog, there are listed some 27 different families of analog-to-digital converters (ADCs). If one were to consider all the variations, there would be considerably more than 50 different types to choose among (excluding digital panel meters and data-acquisition systems, which are catalogued elsewhere). The reason for so many different types is the number of degrees of freedom in selection—technological, functional, performance, and package. Complete information on converters may be found in the 246-page book, *Analog-Digital Conversion Notes*, published by Analog Devices and available for $5.95 from P.O. Box 796, Norwood, MA 02062.

TECHNOLOGICAL FACTORS

The technologies represented here include modules (cards and potted circuits) and integrated circuits—monolithic and hybrid. Modules generally can provide the extremes of performance as well as arbitrary levels of functional completeness. For example, the 12-bit 5MHz MOD-1205 is built on a card that includes a track-hold amplifier.

The technical data in this volume embrace exceptionally high performance (high-resolution and high-speed) A/D converters, in the form of encapsulated modules and printed-circuit cards. As the Selection Guide indicates, there is also a universe of technical data, to be found in Volume I, on a wide range of monolithic and hybrid A/D converters, including many microprocessor-compatible types—and including devices screened to the requirements of MIL-STD-883 and chips for hybrid assembly.

Besides the products in this section, analog-to-digital conversion functions in this Volume (at various levels of system integration) are also inherent in the sections devoted to Data-Acquisition Subsystems, Digital Panel Instruments, Microcomputer Interface Boards, Intelligent Measurement-and-Control Subsystems, and MACSYM. A/D conversion functions are also performed by products in the Voltage-to-Frequency and Synchro-Digital Conversion sections.

FUNCTIONAL CHARACTERISTICS

Block diagrams illustrating the various conversion techniques appear on individual data sheets.

The moderate-speed converters described in this volume (<1MHz) employ two fundamental techniques—*successive approximations*, for moderate-to-high resolution at moderate-to-high speed, and *integration*, for high resolution at modest speeds. The ADC1131 and ADC1140 are examples of the former, the converters used in DPMs, the latter.

Like a chemist's balance with binary weights (1/2, 1/4, 1/8, etc.), the *successive-approximation* converter compares the unknown input with sums of accurately-known binary fractions of full scale, starting with the largest (2^{-1}), and rejecting any that change the comparator's state ("tip the scale"). At the end of conversion (EOC), the output of the converter is a digital word, representing the ratio of the input to full scale by a fractional-binary code.

Integrating types count pulses for a period proportional to the input. Most-frequently used are *dual slope* types, which count off the period required for the integral of the reference to become equal to the average value of the input (over a fixed period). Integrating types can be made insensitive to drift by storing errors during an error-correcting cycle and subtracting them during the input-measuring cycle. This correction can be performed in analog fashion, using capacitance for storage, or digitally—using the information stored in a counter for correction (AD7550).

The *video converters* described here (MATV, MOD-1205, etc.) employ two basic encoding techniques: simultaneous, or *flash* conversion, and serial-Gray-code conversion. High resolution and high speed are obtained by *subranging*, i.e., by performing an n-bit conversion in two steps; Analog Devices has perfected a form of subranging, known as DCS—*digitally corrected subranging*—which permits accurate resolutions of 12 bits and more.*

In *flash* conversion, the analog signal is compared against $2^n - 1$ graded voltage levels, using as many comparators, and the comparator output logic levels are processed by a priority encoder, which converts the "thermometer" output to a binary (or Gray) code. Since the whole conversion occurs essentially simultaneously, it is the fastest means of conversion, but it requires many accurate comparators and large numbers of gates.

In *serial*-analog-parallel-digital conversion, there are a number of cascaded stages, each having a gain of +2 for signals less than one-half the reference, and a gain of −2 for signals between one-half the reference and full scale. At each stage, a decision is made as to whether the signal is larger (1) or smaller (0) than one-half the reference; the stage's analog output becomes the input to the next stage. The complete time for one conversion is determined by the propagation delay of the analog signal through all stages; however, since the decision of each stage can be latched as soon as the stage has settled (and a new conversion can, in principle, be started as soon as the first bit has been latched), the rate at which conversions come out of the pipeline is considerably faster than the time for one sample to go through the conversion process. Though fast, this process is difficult to implement accurately for more than a few bits, because of the compounding of gain (hence errors).

A *subranging* converter digitizes to a group of more-significant bits, and stores them in a latch. A fast, very-high-accuracy D/A converter converts them to an analog signal, which is then subtracted from the input. The difference, or residue, is amplified and digitized, and (in DCS) the result is combined digitally in such a way as to correct for mid-scale conversion errors.

Whatever the technique, these A/D converters comprise several essential functions: an analog section, a digital data-generating section, data outputs, and digital controls. Some video converters also include an on-board track-hold function.

*A considerable amount of useful information about video conversion can be found in "Understanding High-Speed (Video) A/D Converter Specifications", available upon request.

Analog Section
This section requires a reference, one or more high-gain comparators, and either a D/A converter (successive approximations and subranging) or a controllable integrator. The reference may be internal or external, fixed or variable, and of a specified polarity/sense in relation to the analog input. In ratiometric conversion, the reference is usually external and variable.

In successive-approximation converters, the comparator is generally used in the *current-summing* mode; that is, the current output of the DAC is summed with the current developed in the DAC's "feedback resistor" by the input voltage (of opposite polarity), and the balancing action of the converter tends to bring the summing junction towards a voltage null (much like that of an op amp) at the end of conversion. The typical DAC feedback options, when applied in an ADC, provide input-scaling choices. When the bipolar-offset connection is jumpered to the summing point, input signals of both polarities can be handled. The current-switching action of the DAC, at the typically fast clock-rates used in successive-approximation converters, can disturb the output of the analog signal source, especially if it is a slow high-precision op amp. In such cases, buffering may be necessary; some of the modules, have on-board analog buffer-followers, and the card-mounted video converters have on-board track-hold-buffer amplifiers.

In integrating types, absolute-value and polarity-sensing circuitry may be required at the front end to handle both polarities of input. Outputs are usually sign-magnitude BCD.

Digital Data-Generating Section
In successive-approximation types, this section consists of a discrete or integrated successive-approximations register (SAR), its controls, and inputs from the comparator and clock (which is on-board, but in many cases permits external clock pulses, frequency adjustment, and/or control). In integrating types, this section consists of the clock-pulse generator, the counter(s), the input from the comparator, and the associated controls.

Data Outputs
Factors to consider here include coding, resolution, overrange information, levels, format, validity, and timing. *Coding* is usually binary, including jumper-connected offset-binary and/or two's complement for bipolar input signals. For some types, BCD is available, with sign-magnitude for bipolar inputs. Output coding specs should always be checked for digital polarity (positive- or negative-true) of both magnitude and sign information. The *resolution* (number of output bits) must be sufficient for the application; in addition, the specifications must be checked to ascertain that not only will all 2^n (binary) output codes be present (no missing codes), but they must all be present at any temperature in the operating range and related to the input with sufficient accuracy. Integrating types generally have no problems with missing codes (except sometimes at zero, with sign-magnitude coding); nevertheless, nonlinear integration can cause the conversion relationship to become nonlinear. Successive-approximation types have no way of determining *overrange;* they simply fill up. However, counter types roll over and put out a carry flag to signal overrange.

The *data levels* available at the converter output must be checked (TTL, low-voltage CMOS, high-voltage CMOS, ECL), as must the load-driving capability and fanout, and the supply conditions under which appropriate output levels will be furnished. The available choice of output *formats* must also be as desired—parallel, serial, byte-serial, and/or pulse-train. If the converter is intended to communicate directly with a data bus, the output should have three-state capability, and parallel outputs must be enabled in bytes of appropriate widths. If the output is serial NRZ (non-return-to-zero), it should be accompanied by a set of synchronized clock-pulses.

A *status* (or *busy* or EOC or "*data ready*") output changes state to indicate when the data becomes *valid*. The exact nature of this transition should be specified—polarity, timing, levels, etc. For serial data, the exact relationship between the data and the synchronizing clock should be specified, to indicate when each bit becomes valid, and for how long. In general, the *timing* of the whole conversion process must be clearly understood, especially if high speeds are necessary, either for conversion, or for communication with a processor (or both). The timing diagrams on specification sheets are usually accompanied by adequate descriptions of the conversion process and specifications of the critical interface parameters.

Controls
The functions, action (levels or edges), polarity, and timing of all control inputs and outputs should be clearly understood, as well as their loading characteristics and dependence on the supply. In addition to the essential *start-conversion-command* input and a *status* output, various control commands may be available, such as *clock inhibit, high (low)-byte enable, status enable*, and—for speeding up conversion at the cost of resolution in successive-approximation converters—*short-cycle.*

Power Supplies
Appropriate power supplies should be made available, considering the logic levels and analog input signals to be employed in the system. The appropriate degree of power-supply stability to meet the accuracy specifications should be provided. Any recommended external protection circuitry should be planned for. In many cases, separate analog and digital grounds are required; ground wiring should follow best practice to minimize digital interference with high-accuracy analog signals, while ensuring that a connection between grounds can always exist at one point, even if the "mecca" point is inadvertently unplugged from the system.

For video converters, use massive, low-impedance ground systems. The analog and digital grounds are connected together inside converters of these types, so bus bars are essential for system grounding and power distribution; use lots of ground plane on PC boards.

Application Checklist
The designer will generally require specific information in the following categories, before proceeding to the selection process:

- Accurate description of input and output
  1. analog signal range and source or load impedance
  2. digital code needed – binary, offset binary, 2's complement, BCD, etc.
  3. logic level system, i.e., TTL/DTL/ECL compatible
- What are the needed analog bandwidth and data throughput rate?
- What are the control interface details?
- What does the system error budget allow for the converter?
- What are environmental conditions – temperature range, time, supply voltage – over which the converter should operate to the desired accuracy?

For A/D converters, the following considerations are typical.

- What is the analog input voltage range, and to what resolution must the signal be measured?
- What is the requirement for linearity error (or relative accuracy error)?
- To what extent must the various sources of error be minimized as environmental temperature changes?
- How much time can be allowed in the system for each complete conversion? What aperture uncertainty and acquisition time are needed for the sample-hold?
- How stable is the system power supply? What errors will result from power supply terminal voltage variations of this order?
- Can the system tolerate missed codes under any conditions?
- What is the character of the input signal? Is it noisy, sampled, filtered, rapidly-varying, slowly-varying? What kind of pre-processing is to be (or can be) done that will affect the choice (and cost) of the converter? Is aliasing a potential problem?

SPECIFICATIONS & TERMS

Definitions of performance specifications, and related information, are to be found on the following pages, in alphabetical order.*

*For video converters, there are a number of additional application-oriented specifications pertaining to the device's use in a system (e.g., *noise power ratio*, *differential phase*, *differential gain*, *signal-to-noise ratio*). Some useful references for understanding such specifications can be found in the following publications, available from Analog Devices, Computer Labs Division, 505 Edwardia Drive, Greensboro NC 27409.

Kester, W.A., "PCM Signal Codecs for Video Applications", *SMPTE Journal*, Volume 88, November 1979, pp 770-778.
Pratt, W.J., "Test A/D Converters Digitally", *Electronic Design*, December 6, 1975
Smith, B.F. and Pratt, W.J., "Understanding High-Speed A/D Converter Specifications", Computer Labs, 1974

Accuracy, Absolute
The error of an A/D converter at a given output code is the difference between the theoretical and the actual analog input voltages required to produce that code. Since the code can be produced by any analog voltage in a finite band (see Quantizing Uncertainty), the "input required to produce that code" is defined as the midpoint of the band of inputs that will produce the code. For example, if 5 volts (±1.2mV) will theoretically produce a 12-bit half-scale code of 100000000000, then a converter for which any voltage from 4.997V to 4.999V will produce that code will have absolute error of 1/2(4.997 + 4.999) - 5 volts = -2mV.

Absolute error comprises gain error, zero error, and nonlinearity, together with noise, Absolute-accuracy measurements should be made under a set of standard conditions with sources and meters traceable to an internationally accepted standard.

Accuracy, Relative
Relative accuracy error, expressed in %, ppm, or fractions of an LSB, is the deviation of the analog value at any code (relative to the full analog range of the device transfer characteristic) from its theoretical value (relative to the same range), after the full-scale range (FSR) has been calibrated.

Since the discrete points on the theoretical transfer characteristic lie on a straight line, this deviation can also be interpreted as a measure of nonlinearity (see Linearity).

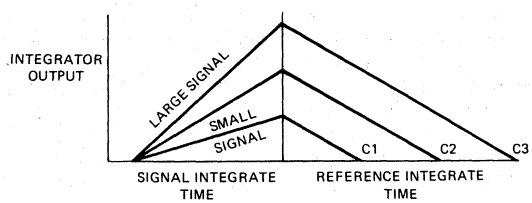
The "discrete points" of an A/D transfer characteristic may be the midpoints of the quantization bands at each code (see Accuracy, Absolute), or—for convenience— the ideal transitions, which are displaced by 1/2LSB.

Aperture Time
This is the interval between the application of the *hold* command to a sample/track-hold and the actual opening of the switch. The aperture time consists of a delay (which depends on the logic and the switching device—50ns for SHA1144) and an uncertainty (due to jitter—20ps max rms for HTS-0025). When a sample-hold is used in an application where timing is critical, the timing of the hold command can be advanced to compensate for the known component of aperture delay. The jitter, however, imposes the ultimate limitation on timing accuracy. When a sample-hold is used with an ADC, the timing uncertainty of the conversion process is reduced by the ratio of aperture jitter to the conversion time, i.e., the maximum frequency which can be handled with less than 1LSB error due to timing is $2^{-n}/(\pi\,\tau_{au})$ instead of $2^{-n}/(\pi\,\tau_c)$, where τ_{au} is the aperture uncertainty and τ_c is the conversion time.

Common Mode Rejection (CMR)
The ability of a device to reject the effect of voltage applied to both input terminals simultaneously. Usually expressed as the log of a "common-mode rejection ratio," e.g., 1,000,000:1 (CMRR) or 120dB (CMR). A CMRR of 1,000,000 to 1 means that a 1V common-mode voltage passes through the amplifier as through it were a differential signal of one microvolt at the input.

Conversion Time and Conversion Rate
The time required for a complete measurement by an ADC is called *conversion time*. For most converters (assuming no significant additional systemic delays), this is identical to the inverse of *conversion rate*. However, in some high-speed converters, because of pipelining, new conversions are initiated before the results of prior conversions have been determined; thus, for example, the MOD-1205 can provide 12-bit output data at a 5MHz word rate (200ns/conversion), even though the time for any one conversion, from start to finish, is two clock periods plus 275ns, or 675ns, at 5MHz.

Dual-Slope Converter
An integrating analog-to-digital converter in which the unknown signal is converted to a proportional time interval, which is then measured digitally. This is done by integrating the unknown for a predetermined time. Then a reference input is switched to the integrator, and integrates "down" from the level determined by the unknown until a "zero" level is reached. The time for the second integration process is proportional to the average of the unknown signal level over the predetermined integrating period. A digital time-interval meter (i.e., counter) is generally used as the output indicator.



Feedthrough
Undesirable signal-coupling around switches or other devices that are supposed to be turned off or provide isolation, e.g., *feedthrough error* in a multiplexer. It is variously specified in %, ppm, fractions of 1 LSB, or fractions of 1 volt, with a given set of inputs, at a specified frequency.

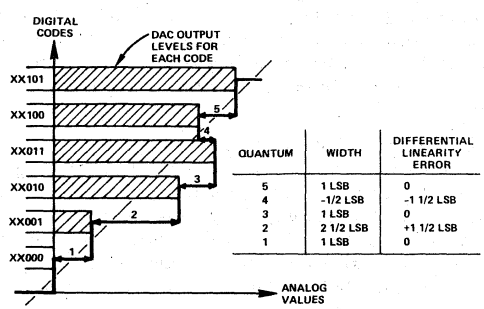
"Flash" Converter
A converter in which all the bit choices are made at the same time. It requires $2^n - 1$ voltage-divider taps and comparators, and a comparable amount of priority encoding logic. An extremely fast scheme, it requires large numbers of precision components. Flash converters are often used for partial conversions in *subranging converters*.

Gain Adjustment
The "gain" of a converter is that analog scale factor setting that provides the nominal conversion relationship, e.g., 10V full scale, in a fixed-reference converter, or 100% of full-scale in a ratiometric converter. Gain- and zero-adjustment principles are discussed under *zero*.

Least Significant Bit (LSB)
In a system in which a numerical magnitude is represented by a series of binary (i.e., two-valued) digits, the "least significant bit" is that digit (or "bit") that carries the smallest value or weight. For example, in the natural binary number 1101 (decimal 13, or $2^3 + 2^2 + 0 + 2^0$), the rightmost "1" is the LSB. Its analog weight, relative to full scale, is 2^{-n}, where n is the number of binary digits. It represents the smallest change that can be resolved by an n-bit converter.

Linearity Error
Linearity error of a converter, expressed in percent or parts-per-million of full-scale range, or fractions of a least-significant bit, is the deviation of the analog values from a straight line, in a plot of the measured conversion relationship. The straight line can be either a "best straight line," determined empirically by manipulation of the gain and/or offset to equalize maximum positive and negative deviations of the actual transfer characteristic from this straight line; or, it can be a straight line passing through the end points of the transfer characteristic after they have been calibrated. Sometimes referred to as "end-point" nonlinearity, the latter is both a more conservative measure and is much easier to verify in actual practice. "End-point" nonlinearity is similar to relative accuracy error (see Accuracy, Relative). Linearity has two components—*differential* and *integral* nonlinearity.

Linearity, Differential and Integral
A digital output code should correspond to a quantum of analog input values exactly 1 LSB in width (2^{-n} of full scale, for an n-bit converter). Any deviation of the measured "step" from the ideal width is called Differential Nonlinearity. It is an important specification, because a differential nonlinearity error greater than 1 LSB can lead to nonmonotonic behavior of of a D/A converter, and missed codes in an A/D converter employing such a DAC. A flagrant example of differential nonlinearity is shown here.



QUANTUM	WIDTH	DIFFERENTIAL LINEARITY ERROR
5	1 LSB	0
4	-1/2 LSB	-1 1/2 LSB
3	1 LSB	0
2	2 1/2 LSB	+1 1/2 LSB
1	1 LSB	0

In the illustration, the horizontal bars represent the measured DAC output values corresponding to 6 adjacent digital codes. The DAC is nonlinear, in that the next-least-significant bit (XX010) is 1½ LSB too large. Thus, instead of the five quanta, or steps, being all equal (= 1 LSB), quantum 2 is 2½ LSB and quantum 4 is -½ LSB. The differential linearity error, the difference between the actual quantum width and the ideal 1 LSB, is +1½ LSB for quantum 2 and -1½ LSB for quantum 4.

When this DAC is used in successive-approximations conversion, it will lead to a missed code. Analog inputs slightly larger than the value of XX100 will be converted to XX100, and analog inputs slightly less than the value of XX100 will be converted to XX010. The code XX011 will not exist; it will be a *missed code.*

Often, instead of a maximum differential nonlinearity specification, there will be a simple specification of "no missed codes", which implies a differential nonlinearity less than 1 LSB.

While differential nonlinearity deals with errors in step size, *integral nonlinearity* has to do with deviations of the overall shape of the conversion response. Even converters that are not subject to differential linearity errors (e.g., integrating types) have integral linearity (sometimes just "linearity") errors.

Power-Supply Sensitivity
The sensitivity of a converter to dc changes in power-supply voltages is normally expressed in terms of percentage change in analog input value (or fractions of the analog equivalent of 1 LSB), corresponding to a given code, for a 1% dc change in the power supply, e.g., $0.05\%/\%\Delta V_S$). Power-supply sensitivity may also be expressed in relation to a specified dc shift of the supply voltage. High-accuracy ADCs intended for battery operation require excellent rejection of large supply-variations.

Quad-Slope Converter
This is an integrating analog-to-digital converter that goes through two cycles of *dual-slope* conversion, once with zero input and once with the analog input being measured. The errors determined during the first cycle are subtracted digitally from the result in the second cycle. The scheme results in an extremely accurate converter. For example, the 13-bit single-chip AD7550 is a CMOS quad-slope A/D converter with typical tempcos (gain and zero temperature coefficients) of 1ppm/°C.

Quantizing Uncertainty (or "Error")
The analog continuum is partitioned into 2^n discrete ranges for n-bit conversion. All analog values within a given range are represented by the same digital code, usually assigned to the nominal midrange value. There is, therefore, an inherent quantization uncertainty of ±½ LSB, in addition to the actual conversion errors. In integrating converters, this "error" is often expressed as "±1 count."

Ratiometric Converter
The output of an A/D converter is a digital number proportional to the ratio of (some measure of) the input to a reference. Most requirements for conversions call for an absolute measurement, i.e., against a fixed reference. In some cases, where the measurement is affected by a changing reference voltage (e.g., the voltage applied to a bridge), it is advantageous to use that same reference as the reference for the conversion, to eliminate the effect of variation. Ratiometric conversion can also serve as a substitute for analog signal division (where the denominator changes but little during the conversion).

Stability
Stability of a converter, usually applies to the insensitivity of its characteristics with time, temperature, etc. All measurements of stability are difficult and time consuming, but stability vs. temperature is sufficiently critical in most applications to warrant universal inclusion in tables of specifications (see "Temperature Coefficients").

Subranging Converters
In this type of converter, an extremely fast conversion produces the most-significant portion of the output word. This portion is converted back to analog with a fast high-accuracy D/A converter and subtracted from the input. The resulting residue is converted to digital at high speed and combined with the results of the earlier conversion to form the output word. In *digitally corrected subranging* (DCS), the two bytes are combined in a manner that corrects for the error of the LSB of the most-significant byte. For example, using 8-bit and 5-bit conversion, and this proprietary technique, a full-accuracy high-speed 12-bit converter can be built.

Successive Approximations
Successive approximations is a high speed method of comparing an unknown against a group of weighted references. The operation of a successive approximations A/D converter is generally similar to the orderly weighing of an unknown quantity on a precision chemical balance, using a set of weights such as: 1 gram, 1/2 gram, 1/4 gram, 1/8 gram, 1/16 gram, etc. The weights are tried in order, starting with the largest. Any weight that tips the scale is removed. At the end of the process, the sum of the weights remaining on the scale will be within one LSB of the actual weight (±½ LSB, if the scale is properly biased — see *zero*).

Temperature Coefficients
In general, temperature instabilities are expressed in %/°C, ppm/°C, as fractions of 1 LSB/°C, or as a change in a parameter over a specified temperature range. Measurements are usually made at room temperature and at the extremes of the specified range, and the temperature coefficient (tempco, T.C.) is defined as the change in the parameter, divided by the corresponding temperature change. Parameters of interest include *gain, linearity, offset* (bipolar), and *zero.* The last three are expressed in % or ppm of full-scale range per Celsius degree.

Gain Tempco: Two factors principally affect converter gain instability with temperature:

a) In fixed-reference converters, the reference source will vary with temperature. For example, the tempco of an AD581L is typically 5ppm/°C.
b) The ratiometric circuitry has a sensitivity to temperature.

Linearity Tempco: Sensitivity of linearity to temperature over the specified range. To avoid missed codes, it is sufficient that the differential nonlinearity error be less than 1 LSB at any temperature in the range of interest. The *differential nonlinearity temperature coefficient* may be expressed as a ratio, as a maximum change over a specified

temperature range, and/or implied by a statement that there are no missed codes when operating within a specified temperature range.

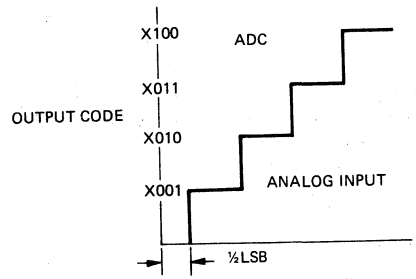
Offset Tempco The temperature coefficient of the all-DAC-switches-off (minus full-scale) point, of a bipolar successive-approximations converter, is dependent on three variables:

1) The tempco of the reference source
2) The voltage stability of the input buffer and the comparator
3) The tracking capability of the bipolar-offset resistors and the gain resistors.

Unipolar Zero The zero tempco of an ADC is dependent only on the zero stability of the integrator and/or the input buffer and the comparator. It may be expressed in $\mu V/^{\circ}C$, or in percent or ppm of full-scale per degree C.

Zero- and Gain-Adjustment Principles

The zero adjustment of a unipolar ADC is set so that the transition from all-bits-off to LSB-on occurs at $\frac{1}{2} \times 2^{-n}$ of nominal full-scale. The gain is set for the final transition



to all-bits-on to occur at F.S. $(1 - \frac{3}{2} \times 2^{-n})$. The "zero" of an offset-binary bipolar ADC is set so that the first transition occurs at -F.S. $(1 - 2^{-n})$ and the last transition at +F.S. $(1 - 3 \times 2^{-n})$. The data sheet instructions should be followed.

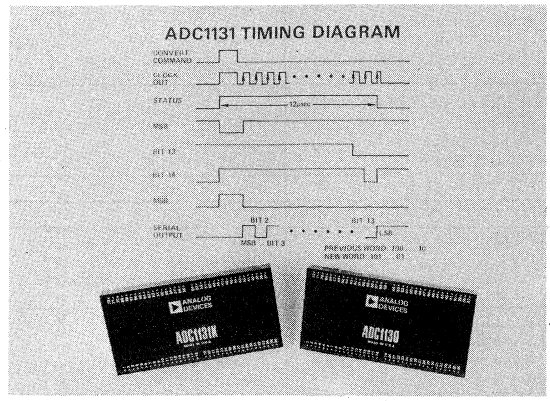
11

14-Bit High Speed Analog-to-Digital Converters

ADC1130, ADC1131

FEATURES
- 14-BIT Resolution and Accuracy
- Fast 12μs Conversion Time (ADC1131J/K)
- Low 10ppm/°C Maximum Gain TC
- User Choice of Input Range
- No Missing Codes

APPLICATIONS
- Wide Band Data Digitizing
- Multi-Channel Computer Interface
- High Accuracy Data Acquisition
- X-Ray Tomography
- Nuclear Accelerator Instrumentation



GENERAL DESCRIPTION

The ADC1130 and ADC1131 are high speed analog-to-digital converters packaged in a small 2″ x 4″ x 0.4″ (51 x 102 x 10mm) module, which perform complete 14-bit conversions in 25μs and 12μs respectively. Using the successive approximations technique, they convert analog input voltages into natural binary, offset binary, or two's complement coded outputs. Data outputs are provided in both parallel and non-return-to-zero serial form.

Four analog input ranges are available: 0 to +20V, 0 to +10V, ±10V, ±5V. The user selects the desired range by making appropriate connections to the module terminals. The ADC1130 and ADC1131 can also be connected so as to perform conversions of less than 14 bit resolution with a proportionate decrease in conversion time.

TIMING

As shown in Figure 1, the leading edge of the convert command set the MSB output to Logic "0" and the CLOCK OUT, STATUS, $\overline{\text{MSB}}$, and BIT 2 through BIT 12 outputs to Logic "1". Nothing further happens until the convert command returns to Logic "0", at which time the clock starts to run and the conversion proceeds.

With the MSB in the Logic "0" state, the internal digital-to-analog converter's output is compared with the analog input. If the D/A output is less than the analog input, the first "0" to "1" clock transition resets the MSB to Logic "1". If the D/A output is greater than the analog input, the MSB remains at Logic "0".

The first "0" to "1" clock transition also sets the BIT 2 output to Logic "0" and another comparison is made. This process continues through each successive bit until the BIT 14 (LSB) comparison is completed. At this point the STATUS and CLOCK OUT return to Logic "0" and the conversion cycle ends.

The serial data output is of the non-return-to-zero (NRZ) format. The data is available, MSB first, 20ns after each of the fourteen "0" to "1" clock transitions.

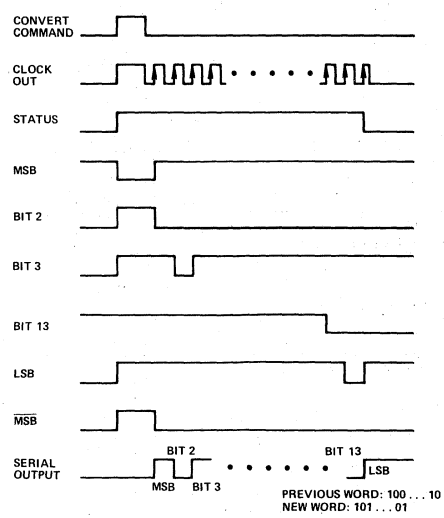


Figure 1. Timing Diagram

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SPECIFICATIONS (typical @ +25°C unless otherwise noted)

MODEL	HIGH SPEED 12μs ADC1131 J	K	MEDIUM SPEED 25μs ADC1130
RESOLUTION, BITS	14	14	14
CONVERSION TIME (max)	12μs	12μs	25μs
ACCURACY			
Integral Nonlinearity Error (LSB)	±1/2 (max)	*	*
Differential Nonlinearity			
Error (LSB)	±1/2 (1 max)	±1/2 (max)	±1/2 (1 max)
Missing Codes	No missing codes	*	*
TEMPERATURE COEFFICIENTS			
Gain ppm/°C	±12 (max)	±7 (+10 max)	±12 max
Unipolar Offset	±0.7 (±3 max)	*	*
Bipolar Offset	±3 (±7 max)	*	*
INPUT VOLTAGE RANGES	±5V, ±10V, +10V, +20V	*	*
INPUT IMPEDANCE (10V RANGE)	2500Ω	*	*
CONVERT COMMAND	Positive Pulse, 200ns min, 400ns max Leading Edge Resets, Trailing Edge Starts, TTL/DTL Compatible	*	*
PARALLEL DATA OUTPUT			
Unipolar	Positive True Binary	*	*
Bipolar	Positive True Offset Binary, Two's Complement	*	*
SERIAL DATA OUTPUT			
Unipolar	Positive True Binary	*	*
Bipolar	Positive True Offset Binary	*	*
STATUS OUTPUT	"1" During Conversion. Complement also available TTL/DTL Compatible.	*	*
LOGIC FANOUTS AND LOADINGS			
Convert Command Input	1TTL Unit Load	*	*
Clock Input	3TTL Unit Loads	*	*
Short Cycle Input	1TTL Unit Load	*	*
Parallel Data Outputs	3TTL Unit Loads/Bit	*	*
Serial Data Output	8TTL Unit Loads	*	*
STATUS Output	2TTL Unit Loads	*	*
$\overline{\text{STATUS}}$ Output	12TTL Unit Loads	*	*
Clock Output	4TTL Unit Loads	*	*
POWER REQUIREMENTS	+15V ±5% @ 40mA	*	*
	−15V ±5% @ 60mA	*	*
	+5V ±5% @ 250mA	*	*
POWER SUPPLY SENSITIVITY			
To ±15V Tracking Supplies			
Gain	±4.5ppm/%Δ V_S	*	*
Zero	±4.5ppm/%Δ V_S	*	*
To ±15V Non-Tracking Supplies			
Gain	±10ppm/%Δ V_S	*	*
Zero	±7ppm/%Δ V_S	*	*
TEMPERATURE RANGE			
Operating	0 to +70°C	*	*
Storage	−55°C to +85°C	*	*

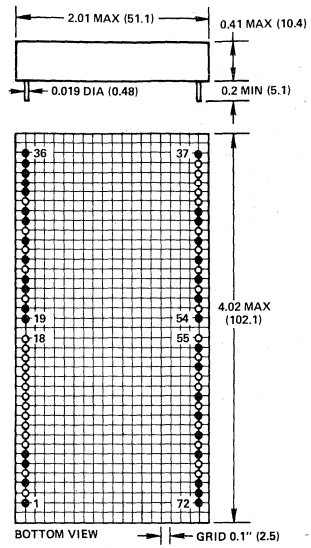
*Same Specifications as ADC1131J.

NOTES:
[1] Offset (zero) and gain errors are adjustable to zero by means of external potentiometers. See Figure 5 for proper connection.
[2] Recommended power supply: Analog Devices model 923.

Specifications subject to change without notice.

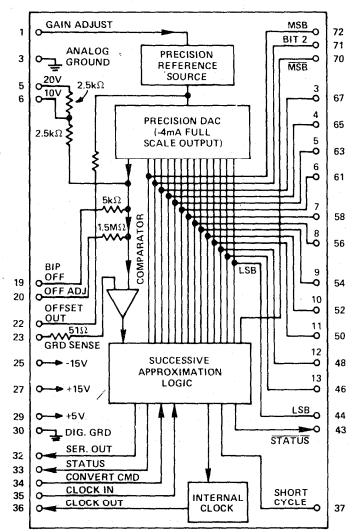
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTE:
Terminal pins installed only in shaded hole locations.
Module weight: 3.5 ounces (99.3 grams).

BLOCK DIAGRAM AND PIN DESIGNATIONS



ANALOG INPUT CHARACTERISTICS

The input circuit of the ADC1130 and ADC1131 are shown in block diagram form.

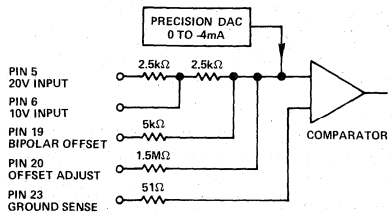


Figure 2. Input Circuit Block Diagram

When the converters are connected as a unipolar device, Pin 19 is left open circuit and, thus, no offset current is applied to the comparator input. The 0 to +10V input signal applied to Pin 6 (or the 0 to +20V input signal applied to Pin 5) develops a 0 to +4mA current which is compared to the 0 to -4mA output of the D/A converter. A voltage between +15V and -15V can be applied to Pin 20 from the wiper of a 100kΩ potentiometer to adjust the zero point by ±40LSB. To reduce the range of this trim padding resistors should be used.

With the offset output, Pin 22, connected to Pin 19, a +2mA offset current is applied to the comparator input. The ADC1130 and ADC1131 will then accept bipolar inputs of ±5V at Pin 6, or ±10V at Pin 5 and compare the 0 to +4mA sum of the offset and input signal currents to the 0 to -4mA D/A converter output. The offset adjustment potentiometer is once again used as described in the preceding paragraph.

Signal ground sense, Pin 23, should normally be jumpered to analog ground, Pin 3. In the event that an offset voltage is developed in the ground wiring, it may be possible to eliminate its effect by connecting Pin 23 directly to the signal or analog ground of the device feeding the analog input signal to the ADC. In any case, Pin 23 must not be left open.

If a high input impedance is required, it can be achieved by using a high speed operational amplifier as an input buffer.

PARALLEL DATA OUTPUT

These converters produce natural Binary Coded outputs when configured as a unipolar device. As a bipolar device, they can produce either Offset Binary or Two's Complement output codes. The most significant bit is represented by Pin 72 (MSB output) for Binary and Offset Binary codes, or by Pin 70 ($\overline{\text{MSB}}$ output) for the Two's Complement code. Tables I and II illustrate the relationship between analog input and digital output for all three codes.

ANALOG INPUT		DIGITAL OUTPUT
0 to +10V Range	0 to +20V Range	Binary Code
+9.9994V	+19.9988V	11111111111111
+5.0000V	+10.0000V	10000000000000
+1.2500V	+2.5000V	00100000000000
+0.0006V	+0.0012V	00000000000001
+0.0000V	+0.0000V	00000000000000

Table 1. Nominal Unipolar Input-Output Relationships

±5V Range	±10V Range	Offset Binary Code	Two's Complement Code
+4.9994V	+9.9988V	11111111111111	01111111111111
+2.5000V	+5.0000V	11000000000000	01000000000000
+0.0006V	+0.0012V	10000000000001	00000000000001
+0.0000V	+0.0000V	10000000000000	00000000000000
-5.0000V	-10.0000V	00000000000000	10000000000000

Table 2. Nominal Bipolar Input-Output Relationships

SERIAL DATA OUTPUT

The serial data output, available on Pin 32, is of the non-return-to-zero format. The data is transmitted MSB first and is Binary coded for unipolar units and Offset Binary coded for bipolar units.

Figure 3, shown below, indicates one method for transmitting data serially using only three wires (plus a digital ground). The data is clocked into a receiving shift register using the delayed clock output of the converter.

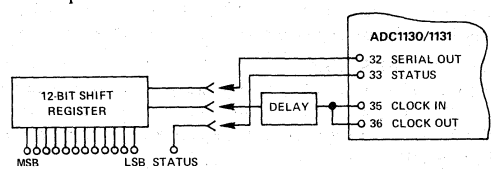


Figure 3. Serial Data Transmission

The timing diagram presented in Figure 4 shows that the converter's clock output must be delayed by an amount of time greater than or equal to the sum of the receiving shift register setup time plus the 20ns clock output to serial output delay.

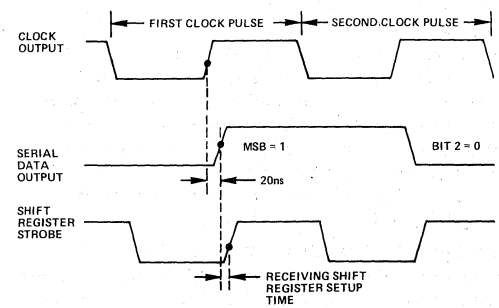


Figure 4. Serial Data Timing Diagram

The 50ns span between the time that the last serial output bit is available and the time that the STATUS output returns to zero insures that the data in the shift register will be valid on the "1" to "0" transition of the STATUS signal.

GAIN AND OFFSET ADJUSTMENTS

The potentiometers used for making gain and offset adjustments are connected as shown in Figure 5. Note that a jumper

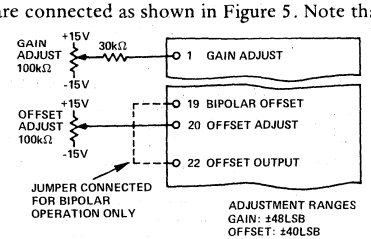


Figure 5. Adjustment Connections

is connected between Pin 19 and Pin 22 for bipolar operation; these pins *must* be left open for unipolar operation.

Proper gain and offset calibration requires great care and the use of extremely sensitive and accurate reference instruments. The voltage standard used as a signal source must be very stable. It should be capable of being set to within 1μV of the desired value at both ends of its range.

The gain and offset calibrations will be independent of each other if the offset adjustment is made first. These adjustments are not made with zero and full scale input signals and it may be helpful to understand why. An A/D converter will produce a given digital output for a small range of input signals, the nominal width of the range being one LSB. If the input test signal is set to a value which should cause the output of the converter to be on the verge of switching from one digital value to the adjacent digital value, the unit can be calibrated so that it does change values at just that point. With a high speed convert command rate and a visual display, these adjustments can be performed in a very accurate and sensitive way. Analog Devices' *Analog-Digital Conversion Notes* gives more detailed information on testing and calibrating A/D and D/A converters.

OFFSET CALIBRATION

For the 0 to +10V unipolar range set the input voltage precisely to +0.0003V; for 0 to +20V units set it to +0.0006V. Adjust the zero potentiometer until the converter is just on the verge of switching from 00 . . . . 0 to 00 . . . . 1.

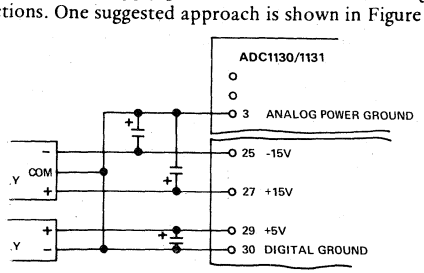
For the ±5V bipolar range set the input voltage precisely to -4.9997V; for ±10V units set it to -9.9994V. Adjust the zero potentiometer until offset binary coded units are just on the verge of switching from 00 . . . . 0 to 00 . . . . 1 and two's complement coded units are just on the verge of switching from 100 . . . 0 to 100 . . . 1.

GAIN CALIBRATION

Set the input voltage precisely to +19.9982V for 0 to +20V units, +9.9991V for 0 to +10V units, +4.9991V for ±5V units, or +9.9982V for ±10V units. Note that these values are 1½LSB's less than nominal full scale. Adjust the gain potentiometer until binary and offset binary coded units are just on the verge of switching from 11 . . . 0 to 11 . . . 1 and two's complement coded units are just on the verge of switching from 011 . . . 10 to 011 . . . 11.

POWER SUPPLY AND GROUNDING CONNECTIONS

These converters do not have an internal connection between analog power ground and digital ground and, thus, a connection must be provided in the external circuitry. The choice of an optimum "star" point for these grounds is an important consideration in the performance of the system. No strict rules can be given, only the general guidelines that the grounding should be arranged in such a manner as to avoid ground loops and to minimize the coupling of voltage drops (on the high current carrying logic supply ground) to the sensitive analog circuit sections. One suggested approach is shown in Figure 6.



6. Power Supply and Grounding Connections

The ±15V and +5V power supplies must be externally bypassed with 15μF (+35V tantalum) capacitors. These capacitors should be connected between Pin 27 and Pin 3, between Pin 25 and Pin 3, and between Pin 29 and Pin 30. Capacitor connections should be made as close to the module pins as possible.

CLOCK CONNECTIONS

When the converters are used with their own internal clock, Pin 36 is simply jumpered to Pin 35. When the internal clock is not used, Pin 36 is grounded and an external clock capable of driving three TTL loads is connected to Pin 35. The convert command should be synchronized with the external clock.

REPETITIVE CONVERSIONS

When making repetitive conversions, a new convert command may be initiated any time after the "1" to "0" transition of the STATUS output. The STATUS output may not, however, be connected directly to the CONVERT COMMAND input for the purpose of automatically generating convert command pulses.

SHORT CYCLE CONNECTIONS

When the converters are operated as a 14-bit device, Pin 37 is left open. If, however, it is to perform conversions of less than 14 bits, Pin 37 is connected to the N+1 bit output (where N is the number of bits in the conversion). The conversion time in this mode of operation is T_C x N/14 where T_C is the conversion time of the particular model when operated at 14-bit resolution.

THE AC1536 MOUNTING CARD

The AC1546 mounting card is available to assist in the application of the ADC1130 and ADC1131. This 4.5" x 6.0" (114 x 152mm) printed circuit card, shown in Figure 7, has sockets which allow the converter to be plugged directly onto it. It includes the necessary gain and zero adjustment potentiometers and bypass capacitors; it mates with a Cinch 251-22-30-160 (or equivalent) dual 33 pin edge connector which is supplied with every card.

The mounting card has an on board amplifier which can be used as an input buffer. The input voltage range is programmed by means of jumpers which the user installs as shown below.

Input Range	Without Buffer Amp. Install Jumper	With Buffer Amp.[1] Install Jumper
0 to +10V	D-C	A-C
0 to +20V	D-B	
±5V	D-C, F-G	A-C, F-G
±10V	D-B, F-G	A-B, F-G

[1] Install resistor R1 15k ohms 1% where indicated on the card.

ANALOG GROUND SENSE	
Local[1]	Install Jumper K-L
Remote	Remove Jumper K-L

[1] Mounting cards are shipped with factory installed jumper K-L.

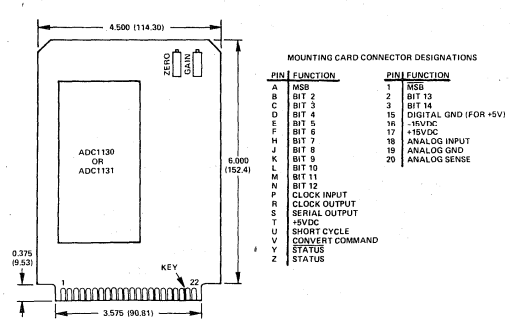


Figure 7. AC1536 Mounting Card

Low Cost 16-Bit Analog-to-Digital Converter

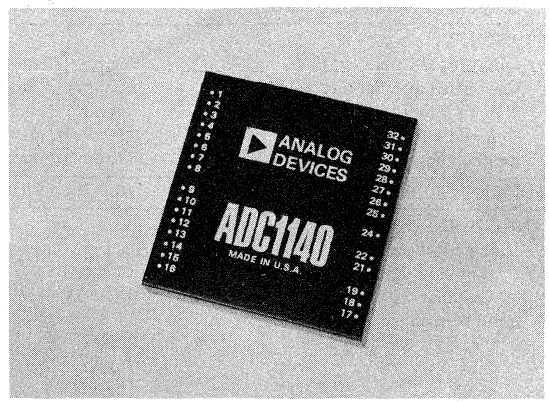
ADC1140

FEATURES

Guaranteed Nonlinearity: ±0.003% FSR max
35μs Maximum Conversion Time
Small Size 2" × 2" × 0.4"
Wide Power Supply Operation: ±12V to ±17V
Low Cost

APPLICATIONS

Process Control Data Acquisition
Seismic Data Acquisition
Nuclear Instrumentation
Medical Instrumentation
Pulse Code Modulation Telemetry
Industrial Scales
Robotics



GENERAL DESCRIPTION

The ADC1140 is a low cost 16-bit successive-approximation analog-to-digital converter having a 35μs maximum conversion time. This converter provides high accuracy, high stability, and low power consumption all in a 2" × 2" × 0.4" module.

High accuracy performance such as integral, and differential nonlinearity of ±0.003% FSR max are both guaranteed. Guaranteed stability such as differential nonlinearity TC of ±2ppm/°C maximum, offset TC of ±30μV/°C maximum, gain TC of ±12ppm/°C maximum, and power supply sensitivity of ±0.002% of FSR/% V_S are also provided by the ADC1140.

The ADC1140 makes extensive use of both integrated circuit and thin-film components to obtain excellent performance, small size, and low cost. The internal 16-bit DAC incorporates Analog Devices proprietary thin-film resistor technology and proprietary CMOS current-steering switches. A low noise reference, low power comparator, and low power successive-approximation register are also used to optimize the ADC1140's design (shown in Figure 1).

The ADC1140 can operate with power supplies ranging from ±12V to ±17V and has provisions for a user supplied external reference. Four analog input voltage ranges are selectable via pin programming: ±5V, ±10V, 0 to +5V and 0 to +10V. Bipolar coding is provided in the offset binary and two's complement formats with unipolar coding displayed in true binary.

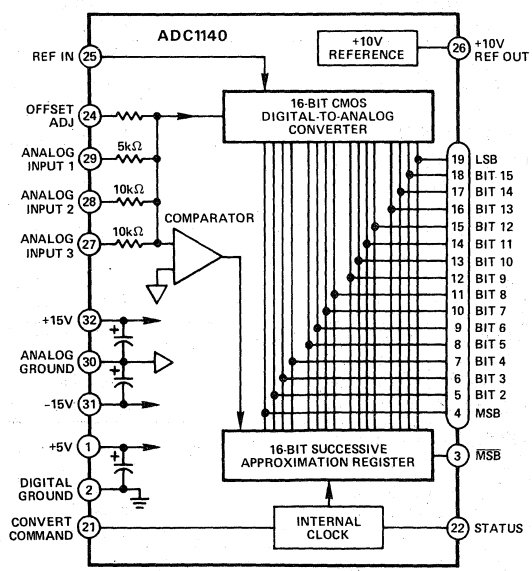


Figure 1. ADC1140 Functional Block Diagram

11

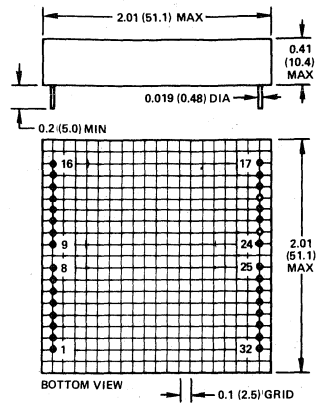
SPECIFICATIONS (typical @ +25°C ±V_S = ±15V, V_{CC} = +5V, V_{REF} = +10.0V unless otherwise specified)

Model	ADC1140
RESOLUTION	16 Bits
CONVERSION TIME	35μs max
ACCURACY[1]	
Nonlinearity Error	±0.003% FSR[2] max
Differential Nonlinearity Error	±0.003% FSR[2] max
STABILITY	
Differential Nonlinearity	±2ppm/°C max
Gain (with internal reference)	±12ppm/°C max
(without internal reference)	±4ppm/°C max
Unipolar Offset	±30μV/°C max
Bipolar Offset	±7ppm/°C max
POWER SUPPLY SENSITIVITY	±0.002% FSR/% V_S
ANALOG INPUT	
Voltage Ranges	
Bipolar	±5V, ±10V
Unipolar	0 to +5V, 0 to +10V
Input Resistance	
0 to +5V	2.5kΩ
0 to +10V, ±5V	5.0kΩ
±10V	10.0kΩ
External Reference Input[3]	
Voltage Range	0 to +12V
Input Resistance	2.5kΩ
DIGITAL INPUT	
Convert Command	Positive Pulse, 100ns Width min Negative Edge Triggered
Logic Loading	1TTL Load
DIGITAL OUTPUT	
Parallel Output Data	
Unipolar	Binary (BIN)
Bipolar	Offset Binary (OBIN) Two's Complement
Output Drive	1TTL Load
Status	Logic "1" During Conversion
Output Drive	1TTL Load
INTERNAL REFERENCE VOLTAGE	+10V, ±0.3%
External Load Current	
(Rated Performance)	2mA max
Temperature Stability	±8.5ppm/°C max
POWER REQUIREMENTS[4]	
Voltage (Rated Performance)	±15V ±3%, +5V ±3%
Voltage (Operating)	±12V to ±17V, +4.75V to +5.25V
Supply Current Drain ±15V	±25mA
+5V	150mA
TEMPERATURE RANGE	
Specified	0 to +70°C
Operating	-25°C to +85°C
Storage	-55°C to +85°C
SIZE	2" X 2" X 0.4" (51 X 51 X 10.4mm)
Weight	1.2 oz (33g)

[1] Offset and gain error are adjustable to zero by means of external potentiometers. See Figure 3 for proper connection.
[2] FSR means Full Scale Range.
[3] Rated performance is specified with +10.0V reference.
[4] Recommended Power Supply: Analog Devices Model 923.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



TERMINAL PINS INSTALLED ONLY IN SHADED HOLE LOCATIONS.

MATING PINS

AC1577 (2 REQUIRED)

PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	+5V	32	+15V
2	DIGITAL GROUND	31	-15V
3	MSB	30	ANALOG GROUND
4	MSB	29	ANALOG IN 1
5	BIT 2	28	ANALOG IN 2
6	BIT 3	27	ANALOG IN 3
7	BIT 4	26	+10V REF OUT
8	BIT 5	25	REFERENCE IN
9	BIT 6	24	OFFSET ADJUST
10	BIT 7	23	NOT USED
11	BIT 8	22	STATUS
12	BIT 9	21	CONVERT COMMAND
13	BIT 10	20	NOT USED
14	BIT 11	19	LSB
15	BIT 12	18	BIT 15
16	BIT 13	17	BIT 14

OPERATION

For operation, the only connections necessary to the ADC1140 are the power supplies, the analog input, the convert command pulse, and a connection between pins 25 and 26 in order to supply the internal precision reference voltage to the DAC (see Figure 2). If an external reference is used this connection is not required (see Figure 7). To obtain the optimum performance see the following sections: Analog Input Characteristics, Input Range Pin Programming, Gain Calibration, Offset Calibration, and Power Supply and Grounding Connections.

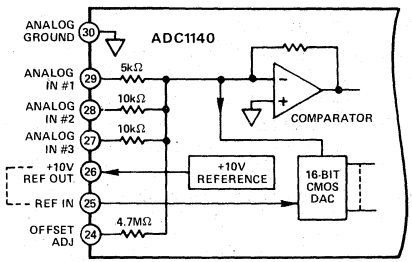


Figure 2. Analog Input Block Diagram

ANALOG INPUT CHARACTERISTICS

The analog input section consists of three analog input terminals. Analog input range selection is accomplished by pin programming as shown in Table 1.

In the unipolar mode, a 0 to +10V or a 0 to +5V input signal develops a 0 to +2mA current that is compared to the 0 to -2mA (shown in Figure 2) current output of the DAC.

In the bipolar mode, a +1mA offset current from the reference is applied to the comparator input via pin programming connections. The ADC1140 can then accept either ±5V or ±10V inputs. These inputs again will be converted to current and compared with the DAC's 0 to -2mA current output.

Input Signal Range	Coding	Connect Input Signal To Pin(s)	Connect Pin 26 To Pin*	Connect Pin 30 To Pin(s)
±10V	OBIN, Two's Comp	28	27	29, 2
±5V	OBIN, Two's Comp	29	27	28, 2
0 to +5V	BIN	27, 28, 29	Open	2
0 to +10V	BIN	27, 28	Open	29, 2

*If Internal Reference is used, Pins 25 and 26 must be connected together (see Figure 3 and the gain calibration section).

Table 1. Analog Input Voltage Pin Programming

OPTION OFFSET & GAIN CALIBRATION

Initial offset and gain errors can be adjusted to zero by potentiometers as shown in Figure 3. Proper offset and gain calibration requires great care and the use of extremely sensitive and accurate reference instruments. The voltage standard used as a signal source must be very stable. It should be capable of being set to within 1μV of the desired value at both ends of its range. The potentiometers selected should be of the good quality Cermet type. Multi-turn potentiometers having ten to fifteen turns and 100ppm/°C temperature coefficients will be adequate. The temperature coefficients contributed by these Cermet potentiometers will be less than 0.1ppm/°C.

By adjusting the offset first, gain and offset adjustments will remain independent of each other.

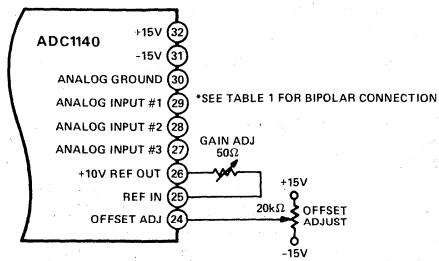


Figure 3. Offset and Gain Calibration

OFFSET CALIBRATION

For 0 to +10V range, set the input voltage precisely to +76μV; for 0 to +5V range, set it at +38μV. Adjust the zero potentiometer until the binary coded converter is just on the verge of switching from 000 . . . 00 to 000 . . . 01.

For ±5V range, set the input voltage precisely to -4.999924V; for ±10V range, set it at -9.999847V. Adjust the zero potentiometer until the offset binary coded units are just on the verge of switching from 000 . . . 00 to 000 . . . 01 and the two's comp. coded units are just on the verge of switching from 100 . . . 0 to 100 . . . 1.

GAIN CALIBRATION

Set the input voltage precisely at +9.99977V for 0 to +10V input range, +4.99977V for ±5V input range, +9.99954V for ±10V input range, or +4.99988V for 0 to +5V input range, adjust the gain potentiometer until binary and offset binary coded units are just on the verge of switching from 111 . . . 0 to 111 . . . 1 and two's comp. coded units are just on the verge of switching from 011 . . . 10 to 011 . . . 11. Note that these values are 1 1/2 LSBs less than nominal full scale.

POWER SUPPLY AND GROUNDING CONNECTIONS

The analog power ground (pin 30) and digital ground (pin 2) are not connected internally in the ADC1140, thus the connection must be made externally. The choice of an optimum "star" point is an important consideration in avoiding ground loops and to minimize coupling between the analog and digital sections. One suggested approach is shown in Figure 4.

Because the ADC1140 contains high quality tantalum capacitors on each of the power supply inputs to ground, external bypass capacitors are not required.

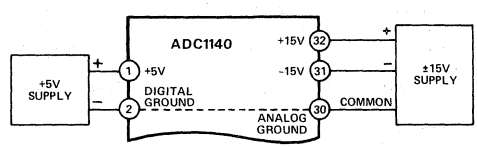


Figure 4. Power Supply and Grounding Techniques

ADC1140 TIMING

Conversion is initiated with the negative going edge of the Convert Command pulse as shown in Figure 5. The Convert Command pulse width must be a minimum of 100ns. Once the conversion process is initiated, it cannot be retriggered until after the end of conversion.

With the negative edge of the Convert Command pulse, all internal logic is reset. The MSB is set low with the remaining digitial outputs set to logic high state, and the status line is set high and remains high thru the full conversion cycle.

During conversion each bit, starting with the MSB, is sequentially switched low at the rising edge of the internal clock. The DAC output is then compared to the analog input and the bit decision is made. Each comparison lasts one clock cycle with the complete 16-bit conversion taking 35μs maximum. At this time, the STATUS line goes low signifying that the low conversion is complete.

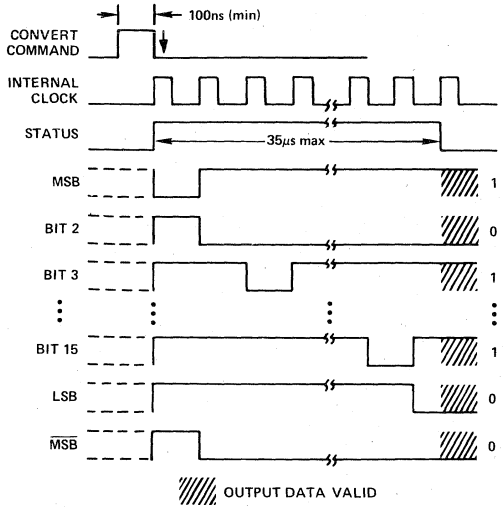


Figure 5. ADC1140 Timing Diagram

ANALOG INPUT/OUTPUT RELATIONSHIPS

The ADC1140 produces a true binary coded output when configured as a unipolar device. Configured as a bipolar device, it can produce either offset binary or two's complement output codes. The most significant bit (MSB) is displayed on pin 4 for the binary and offset binary codes or on pin 3 for the two's complement code. Table 2 shows the unipolar analog input/digital output relationships. Table 3 shows the bipolar analog input/digital output relationships for offset binary code and two's complement codes.

Analog Input		Digital Output
0 to +5V Range	0 to +10V Range	Binary Code
+4.999924V	+9.99985V	1111 1111 1111 1111
+2.50000V	+5.00000V	1000 0000 0000 0000
+1.25000V	+2.50000V	0100 0000 0000 0000
+0.62500V	+1.25000V	0010 0000 0000 0000
+0.000076V	+0.000153V	0000 0000 0000 0001
+0.00000V	+0.00000V	0000 0000 0000 0000

Table 2. Unipolar Input/Output Relationships

Analog Input		Digital Output	
±5V Range	±10V Range	Offset Binary Code	2's Complement Code
+4.99985V	+9.99970V	1111 1111 1111 1111	0111 1111 1111 1111
+2.50000V	+5.00000V	1100 0000 0000 0000	0100 0000 0000 0000
+0.000153V	+0.000305V	1000 0000 0000 0001	0000 0000 0000 0001
+0.00000V	+0.00000V	1000 0000 0000 0000	0000 0000 0000 0000
-5.00000V	-10.00000V	0000 0000 0000 0000	1000 0000 0000 0000

Table 3. Bipolar Input/Output Relationships

HIGH RESOLUTION DATA ACQUISITION SYSTEM

Shown in Figure 6 is a high resolution data acquisition system. Here the SHA1144, a high resolution sample-hold amplifier, is used to drive the ADC1140. Conversion is initiated by the negative edge of the convert command pulse. At this time the STATUS pulse goes low causing the SHA1144 to go from the sample mode to the hold mode. When the conversion is complete, 35μs later, the STATUS pulse goes low, thus placing the SHA1144 in the sample mode.

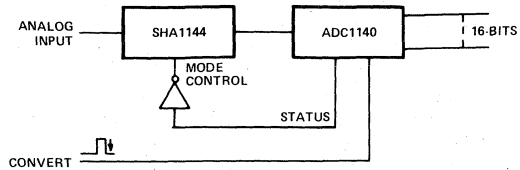


Figure 6. High Resolution Data Acquisition System

EXTERNAL REFERENCE

The ADC1140 is capable of operating with an external +10.0V reference. Simply disconnect the gain trim potentiometer from pin 26 and connect it to the external reference as shown in Figure 7. The external reference output must appear as a low impedance and must remain very stable during conversion to insure that accuracy is maintained. Gain error is adjusted as previously discussed in the gain calibration section.

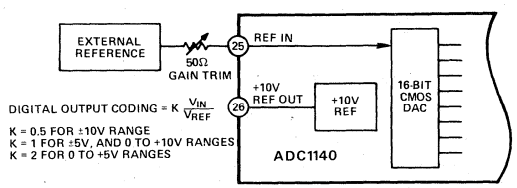


Figure 7. External Reference

The ADC1140 is only tested and specified for a +10.0V reference voltage but nonstandard external voltages can be used with the digital output coding being determined by the formula shown in Figure 7.

PIA INTERFACE

The ADC1140 can be used with a PIA to interface directly to a microprocessor. As shown in Figure 8 the 16-bit output of the ADC1140 is split into two 8-bit bytes. Part A of the PIA is programmed to read the eight most-significant-bits while Part B reads the eight least-significant-bits. Output CB2 is used to start the ADC1140 conversion process. CB1, of the PIA, is used to sense the STATUS of the ADC1140 so that the end of conversions can be determined. The control bus, address bus, and data bus are then connected directly to the microprocessor.

With the use of PIAs, control of one or more ADC1140s can be accomplished in many different configurations.

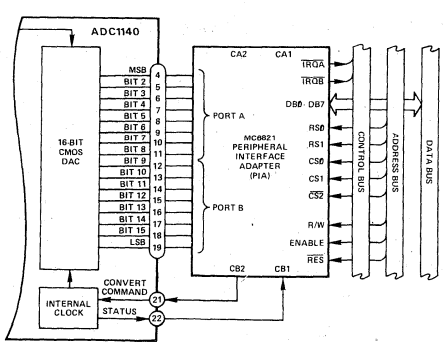


Figure 8. ADC1140 Interface to PIA

Ultra High Speed 8- and 10-Bit A/D Converters

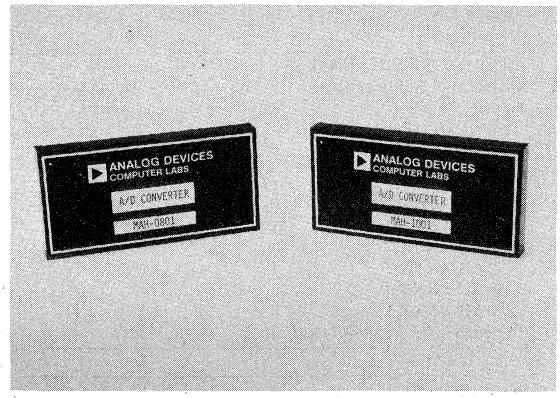
MAH-0801, -1001

FEATURES

High Speed at Low Cost
8-Bits @ 750ns max
10-Bits @ 1μs max
Monotonic Over Temperature
Differential Nonlinearity ±1/4LSB typ
Parallel and Serial Outputs
Pin and Function Compatible with 4130, 4131

APPLICATIONS

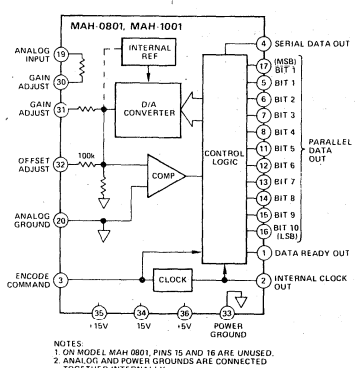
High Speed Data Acquisition
Real Time Waveform Analysis
Radar Signal Processing
Analytical Instruments



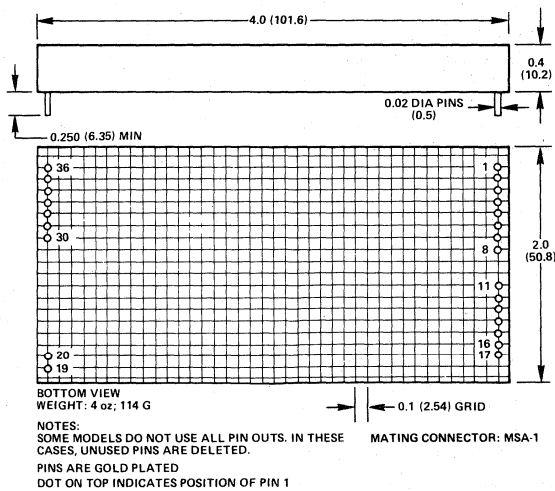
GENERAL DESCRIPTION

The MAH series of high-speed analog-to-digital converters represent the latest "state-of-the-art" in high speed successive approximation technology. They are the fastest and most accurate complete converters of their type, featuring internal reference, clock, timing, encoding, and control logic functions. The MAH series A/Ds should be considered in applications where completeness of design function, ease of interface, and speed are required. These modules make maximum use of the latest monolithic and hybrid parts to minimize total parts complexity and increase reliability. They are designed to be form, fit, and function compatible with the T.P. 4130 and 4131, with advantages over the latter in overall accuracy without any sacrifice in speed.

In almost all applications, these A/Ds require the use of fast sample-and-hold. Depending upon the application, either the ADI THC or THS series of ultra-fast sample-and-holds are recommended.



MAH-0801 and MAH-1001 Block Diagram



NOTES:
SOME MODELS DO NOT USE ALL PIN OUTS. IN THESE CASES, UNUSED PINS ARE DELETED.
PINS ARE GOLD PLATED
DOT ON TOP INDICATES POSITION OF PIN 1

MATING CONNECTOR: MSA-1

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SPECIFICATIONS (typical @ +25°C unless otherwise noted)

MODEL	UNITS	MAH-0801	MAH-1001
RESOLUTION FS @ Full Scale	Bits	8	10
ACCURACY (Relative to Full Scale)	±% FS	0.02	*
Quantization Error	LSB	±1/2	*
Nonlinearity	LSB (max)	±1/4	±1/2
Differential Nonlinearity	LSB (max)	±1/4	±1/2
	LSB (typ)	±1/8	±1/4
Missing Codes		No Missing Codes 0 to +70°C	
Monotonicity		Monotonic 0 to +70°C	
TEMPERATURE COEFFICIENTS			
Differential Nonlinearity	±ppm/°C	3	*
Gain	±ppm/°C	20	*
Zero Offset (Unipolar)	±μV/°C	10	*
Zero Offset (Bipolar)	±ppm/°C	15	*
INPUT			
Ranges (Full Scale)			
MAH-XXXX-1	V	0 to -5	*
MAH-XXXX-2	V	0 to -10	*
MAH-XXXX-3	V	±5	*
MAH-XXXX-4	V	±10	*
MAH-XXXX-5	V	±1.024	*
Impedance (Function of Option)	Ω/V	100	*
OVERVOLTAGE	V	To Twice Peak Input FS Without Damage.	
CONVERSION TIME[1]	ns max	750	1000
	ns typ	700	950
ENCODE COMMAND			
Logic Levels (1 Standard TTL Load)	V	"0" = 0 to +0.4, "1" = +2 to +5.5	
Function		Positive-going edge resets converter. Trailing edge starts conversion.	
Duration (Width)	ns min (max)	50 (150)	*
Rise and Fall Times	ns max	20	*
Repetition Rate	kHz max	1333	1000
LOGIC OUTPUTS			
Levels TTL (Same as Encode Command)			
Drive Capability		Data and Data Ready—10 Std TTL Loads, Clock—10 TTL Loads	
Parallel Data		8 or 10 lines of data held until start of next Encode Command	
Coding (Unipolar)		CBN	*
(Bipolar)		COB/C2SC	*
Serial Data		MSB first, successive pulse output during conversion, NRZ.	
Coding		Same as parallel output except 2SC not available.	
Clock		Pulse train of 9 or 11 internal clock pulses, gated on during the conversion period.	
POWER REQUIREMENTS			
+14.5V to +15.5V	mA max	50	*
-14.5V to -15.5V	mA max	30	*
+5V ±5%	mA max	250	*
TEMPERATURE RANGE			
Operating	°C	0 to +70	*
Storage	°C	-55 to +85	
PHYSICAL CHARACTERISTICS			
Case		Diallyl Phthalate per MIL-M-14 Type SDG-F	

NOTE:
[1] Total conversion time from leading edge of encode command pulse to trailing edge of data ready pulse with 50ns wide encode command.
*Specifications same as MAH-0801.
Specifications subject to change without notice.

OUTPUT CODING

The logic output coding is shown true relative to the analog input to the A/D. If an inverting track and hold—such as the Analog Devices THC series—or an inverting op amp is used ahead of the A/D, the true logic coding is inverted relative to the system input. This yields the systemic coding as follows:

Scale	Input Voltage	Complementary Straight Binary
-FS -1LSB	-9.9900V	1111 1111 11
-3/4 FS	-7.5000V	1100 0000 00
-1/2 FS	-5.0000V	1000 0000 00
-1/4 FS	-2.5000V	0100 0000 00
-1LSB	-0.0010V	0000 0000 01
0	0.0000V	0000 0000 00

NOTE
(0 to -10V) for MAH-1001-2; LSB = 10mV for MAH-1001-1, apply input voltage factor of 1/2.

Table 1. MAH-0801 and MAH-1001 Unipolar Operation for Options 1 and 2

Binary (BIN) in place of Complementary Binary (CBN) for options 1 and 2; Offset Binary (OBN) in place of Complementary Offset Binary (COB) for options 3, 4 and 5; Two's Complement (2SC) in place of Complementary Two's Complement (C2SC).

Scale	Input Voltage	Complementary Offset Binary	Complementary Two's Complement
-FS -1LSB	-4.9900V	1111 1111 11	0111 1111 11
-3/4 FS	-3.7500V	1110 0000 00	0110 0000 00
-1/2 FS	-2.5000V	1100 0000 00	0100 0000 00
0	0.0000V	1000 0000 00	0000 0000 00
+1/2 FS	+2.5000V	0100 0000 00	1100 0000 00
+3/4 FS	+3.7500V	0010 0000 00	1010 0000 00
+FS -1LSB	+4.9900V	0000 0000 01	1000 0000 01
+FS	+5.0000V	0000 0000 00	1000 0000 00

NOTES:
(-5V to +5V) for MAH-1001-3; LSB = 10mV for MAH-1001-4 apply input voltage factor of 2.

Table 2. MAH-0801 and MAH-1001 Bipolar Operation for Options 3 and 4

Scale	Input Voltage	Complementary Offset Binary	Complementary Two's Complement
-FS -1LSB	-1.022V	1111 1111 11	0111 1111 11
-1/2 FS	-0.512V	1100 0000 00	0100 0000 00
0	-0.000V	1000 0000 00	0000 0000 00
+1/2 FS	+0.512V	0100 0000 00	1100 0000 00
+FS	+1.024V	0000 0000 00	1000 0000 00

NOTE
(-1.024V to +1.024V) for MAH-1001-5; LSB = 2mV.

Table 3. MAH-0801 and MAH-1001 Bipolar Operation for Option 5

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CALIBRATION AND ADJUSTMENT

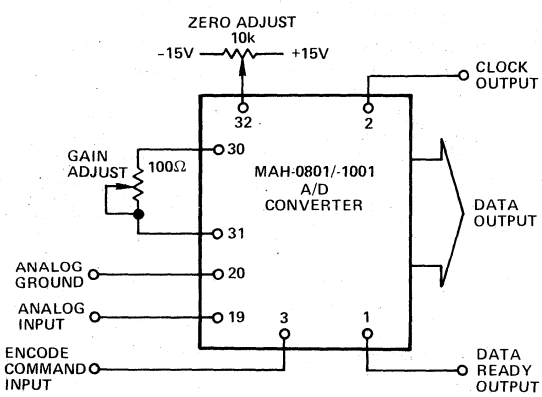


Figure 1. MAH-0801 and MAH-1001 Hookup

PROCEDURE:
1. APPLY ENCODE COMMAND PULSE TO THE ENCODE COMMAND INPUT (PIN 3).
2. CONNECT A PRECISION VOLTAGE SOURCE TO THE ANALOG INPUT (PIN 19) AND ANALOG GROUND (PIN 20). ADJUST THIS SOURCE FOR +1/2LSB. VARY THE ZERO ADJUST POTENTIOMETER FOR AN LSB FLUTTER (THIS WILL APPEAR AS AN EQUAL UNCERTAINTY AT THE OUTPUT BETWEEN THE CODES 0000 .... 0000 AND 0000 .... 0001).
3. WITH THE PRECISION VOLTAGE SOURCE ADJUSTED TO -FS +1/2LSB, ADJUST THE GAIN POTENTIOMETER FOR A FLUTTER BETWEEN CODES 1111 .... 1110 AND 1111 .... 1111.

Unipolar Operation

PROCEDURE:
1. APPLY AN ENCODE COMMAND TO THE ENCODE COMMAND INPUT (PIN 3).
2. CONNECT A PRECISION VOLTAGE SOURCE TO THE ANALOG INPUT (PIN 19) AND ANALOG GROUND (PIN 20). ADJUST THIS SOURCE TO +FS -1/2LSB. THE ZERO ADJUST POTENTIOMETER FOR A FLUTTER BETWEEN VARY CODES 0000 .... 0000 AND 0000 .... 0001.
3. ADJUST THE VOLTAGE SOURCE TO -FS +1/2LSB. ADJUST THE GAIN POTENTIOMETER FOR A FLUTTER BETWEEN THE CODES 1111 .... 1110 AND 1111 .... 1111.

Bipolar Operation

TIMING DIAGRAM

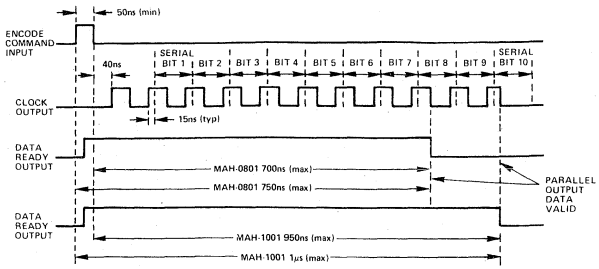


Figure 2. MAH-0801 and MAH-1001 Timing Diagram

APPLICATIONS

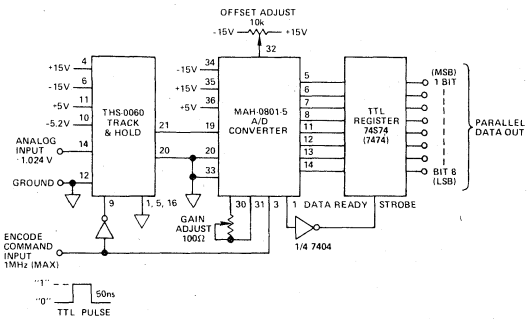


Figure 3. Depicts a Complete 8-Bit, 1MHz Conversion System Using the THS-0060 Track-and-Hold and the MAH-0801-5 Low-Voltage Input A/D Converter

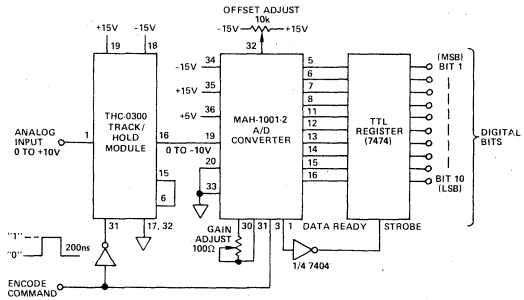


Figure 4. Depicts the MAH-1001-2 A/D Converter Used with the THC-0300 Track-and-Hold

NOTES ON USAGE

The use of a large ground plane is highly recommended. Tie all grounds for both the ADC and T&H together. Make the distance from the ADC to the system ground as short as possible with as low an impedance as possible. Bypass each power supply run with a ceramic (0.1µF) and tantalum (3.3µF) capacitor. Keep the analog input as far away from the digital outputs as practical. Avoid the use of twisted pair cables for digital outputs wherever possible. The use of coax cable for analog inputs is recommended wherever practical to avoid digital feedback.

PIN DESIGNATIONS
MAH-0801, MAH-1001

PIN	FUNCTION	PIN	FUNCTION
1	DATA READY OUT	15	BIT 9 OUT
2	INTERNAL CLOCK OUT	16	BIT 10 OUT (LSB)
3	ENCODE COMMAND IN	17	BIT 1 OUT (MSB)
4	SERIAL OUTPUT	19	ANALOG INPUT
5	BIT 1 OUT (MSB)	20	ANALOG GROUND
6	BIT 2 OUT	30	GAIN ADJUST
7	BIT 3 OUT	31	GAIN ADJUST
8	BIT 4 OUT	32	OFFSET ADJUST
11	BIT 5 OUT	33	POWER GROUND
12	BIT 6 OUT	34	-15V POWER IN
13	BIT 7 OUT	35	+15V POWER IN
14	BIT 8 OUT	36	+5V POWER IN

NOTES:
On Model MAH-0801, Pins 15 and 16 are deleted.
Power and Analog grounds are internally connected.

ORDERING INFORMATION

The 8- and 10-bit versions of the MAH series may be ordered with various options according to the chart below.

MAH-0801 **-1**

RESOLUTION AND ACCURACY	ANALOG INPUT RANGE
MAH-0801 = 8 Bits	-1 0 to -5V FS
MAH-1001 = 10 Bits	-2 0 to -10V FS
	-3 ±5V FS
	-4 ±10V FS
	-5 ±1.024V FS

Ultra High Speed 8-, 10-, and 12-Bit A/D Converters

MAS-0801, -1001, -1202

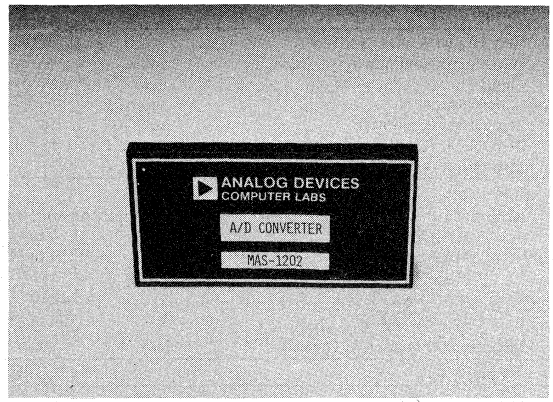
FEATURES

High Speed at Low Cost
- **8 Bits 1μs max**
- **10 Bits 1.5μs max**
- **12 Bits 2μs max**

No Missing Codes Over Temperature
Low Power
Industry Standard Pin Out
Parallel and Serial Outputs

APPLICATIONS

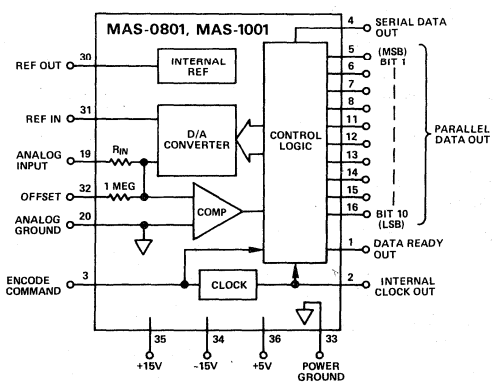
High Speed Data Acquisition
Real Time Waveform Analysis
Radar Signal Processing
Analytical Instruments



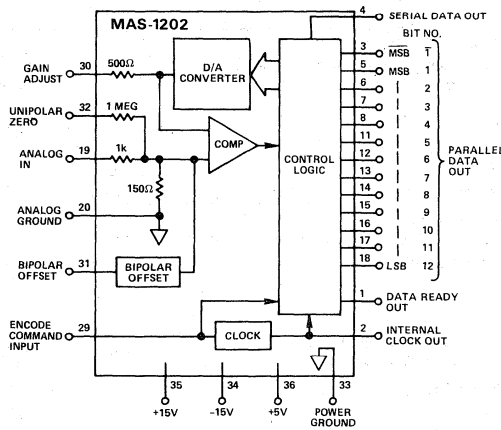
GENERAL DESCRIPTION

The MAS series of high speed analog to digital converters represent the "state of the art" in application of the successive approximation conversion technique by providing highest speed at lowest cost. With monotonicity guaranteed over temperature these reliable modules are form, fit and function compatible with popular industry standards from Datel and Philbrick (for new designs consider the HAS series of hybrid converters).

In most applications these A/Ds should be used with a fast sample hold such as the THS/THC series.



MAS-0801 and MAS-1001 Block Diagram



MAS-1202 Block Diagram

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SPECIFICATIONS (typical @ +25°C unless otherwise noted)

Model	Units	MAS-0801	MAS-1001	MAS-1202
RESOLUTION FS = Full Scale	Bits	8	10	12
ACCURACY (Relative to Full Scale)	±% FS	0.2	0.05	0.012
Quantization Error	LSB	±1/2	*	*
Nonlinearity	LSB (max)	±1/2	*	*
Differential Nonlinearity	LSB (max)	±1/2	*	*
Missing Codes		No Missing Codes 0 to +70°C		
TEMPERATURE COEFFICIENTS				
Differential Nonlinearity	±ppm/°C	3	*	*
Gain	±ppm/°C	20	*	30
Gain (Option-P)	±ppm/°C	5	*	NA
Zero Offset (Unipolar)	±μV/°C	10	*	100
Zero Offset (Bipolar)	±ppm/°C	15	*	*
Zero Offset (Option-P)	±ppm/°C	5	*	NA
INPUT				
Ranges (Full Scale)		Options MAS-0801 and MAS-1001 ONLY		STANDARD
MAS-XXXX-1	V	0 to -5	*	0 to +10/±5
MAS-XXXX-2	V	0 to -10	*	NA
MAS-XXXX-3	V	±5	*	NA
MAS-XXXX-4	V	±10	*	NA
MAS-XXXX-5	V	±1.024	*	NA
Impedance (Function of Option)	Ω/V	100	*	1150Ω
OVERVOLTAGE	V	To Twice Peak Input FS Without Damage.		
CONVERSION TIME[1]	μs max	1	1.5	2
	μs typ	0.8	1.3	1.8
ENCODE COMMAND				
Logic Levels (1 Standard TTL Load)	V	"0" = 0 to +0.4, "1" = +2 to +5.5		
Function		Positive-going edge resets converter, Trailing edge starts conversion for 8- and 10-bit versions.		
Duration (Width)	ns min	50	*	100
Rise and Fall Times	ns max	20	*	*
Repetition Rate	kHz max	1000	666	500
LOGIC OUTPUTS				
Levels TTL (Same as Encode Command)				
Drive Capability		Data and Data Ready — 4 Std TTL Loads, Clock — 6TTL Loads		
Parallel Data		8, 10 or 12 lines of data held until next Encode Command		
Coding (Unipolar)		CBN	*	BIN
(Bipolar)		COB/2SC	*	OBN/2SC
Serial Data		MSB first, successive pulse output during conversion, NRZ.		
Coding		Same as parallel output except 2SC not available.		
Clock		Pulse train of 9, 11 or 13 internal clock pulses, gated on during the conversion period.		
POWER REQUIREMENTS				
+14.5V to +15.5V	mA	70	*	80
-14.5V to -15.5V	mA	30	*	20
+5V ±5%	mA	150	*	*
TEMPERATURE RANGE				
Operating	°C	0 to +70	*	*
Storage	°C	-55 to +85	*	*
PHYSICAL CHARACTERISTICS				
Case		Diallyl Phthalate per MIL-M-14 Type SDC-F		

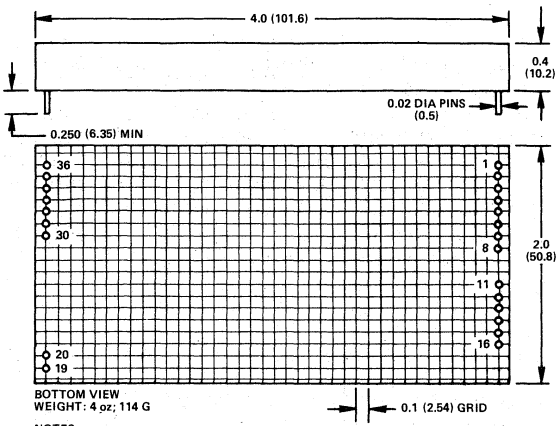
NOTE:
[1] Total conversion time from leading edge of encode command pulse to trailing edge of data ready pulse with 50ns wide encode command.

*Specifications same as MAS-0801.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

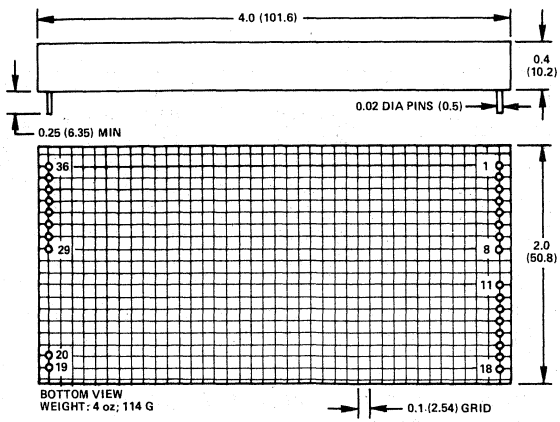
Dimensions shown in inches and (mm).



NOTES:
SOME MODELS DO NOT USE ALL PIN OUTS. IN THESE CASES, UNUSED PINS ARE DELETED.
PINS ARE GOLD PLATED
DOT ON TOP INDICATES POSITION OF PIN 1

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTES:
PINS ARE GOLD PLATED
DOT ON TOP INDICATES POSITION OF PIN 1

PIN DESIGNATIONS
MAS-0801, MAS-1001

PIN	FUNCTION	PIN	FUNCTION
1	DATA READY OUT	15	BIT 9 OUT
2	INTERNAL CLOCK OUT	16	BIT 10 OUT (LSB)
3	ENCODE COMMAND IN	19	ANALOG INPUT
4	SERIAL OUTPUT	20	ANALOG GROUND
5	BIT 1 OUT (MSB)	30	REFERENCE OUT
6	BIT 2 OUT	31	REFERENCE INPUT
7	BIT 3 OUT	32	OFFSET
8	BIT 4 OUT	33	POWER GROUND
11	BIT 5 OUT	34	-15V POWER IN
12	BIT 6 OUT	35	+15V POWER IN
13	BIT 7 OUT	36	+5V POWER IN
14	BIT 8 OUT		

PIN DESIGNATIONS
MAS-1202

PIN	FUNCTION	PIN	FUNCTION
1	DATA READY	16	BIT 10 OUT
2	INTERNAL CLOCK OUT	17	BIT 11 OUT
3	BIT 1 OUT ($\overline{\text{MSB}}$)	18	BIT 12 OUT (LSB)
4	SERIAL DATA OUT	19	ANALOG INPUT
5	BIT 1 OUT (MSB)	20	ANALOG GROUND
6	BIT 2 OUT	29	ENCODE COMMAND IN
7	BIT 3 OUT	30	GAIN ADJUST
8	BIT 4 OUT	31	BIPOLAR OFFSET
11	BIT 5 OUT	32	UNIPOLAR ZERO
12	BIT 6 OUT	33	POWER GROUND
13	BIT 7 OUT	34	-15V POWER IN
14	BIT 8 OUT	35	+15V POWER IN
15	BIT 9 OUT	36	+5V POWER IN

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ORDERING INFORMATION

The 8- and 10-bit versions of the MAS series may be ordered with various options according to the chart below.

MAS-0801	P	-1	-CBN
RESOLUTION AND ACCURACY	TEMPCO	ANALOG INPUT RANGE	LOGIC OUTPUT CODING (See Note 1)
MAS-0801 = 8 Bits MAS-1001 = 10 Bits	For ±5ppm/°C tempco at slightly higher cost, add "P". For standard tempco, leave blank.	-1 0 to -5V FS -2 0 to -10V FS -3 ±5V FS -4 ±10V FS -5 ±1.024V FS	CBN = Complementary Binary (Options 1 and 2) COB = Complementary Offset Binary (Options 3, 4 and 5) C2SC = Complementary Two's Complement (Options 3, 4 and 5)

NOTES:
For 12-bit performance order the MAS-1202 which has no options.
The mating connector for the MAS series is the MSA-1.

OUTPUT CODING

The logic output coding is shown true relative to the analog input to the A/D. If an inverting track and hold—such as the Analog Devices THC series—or an inverting op amp is used ahead of the A/D, the true logic coding is inverted relative to the system input. This yields the systemic coding as follows:

Scale	Input Voltage	Complementary Straight Binary
-FS -1LSB	-9.9900V	1111 1111 11
-3/4 FS	-7.5000V	1100 0000 00
-1/2 FS	-5.0000V	1000 0000 00
-1/4 FS	-2.5000V	0100 0000 00
-1LSB	-0.0010V	0000 0000 01
0	0.0000V	0000 0000 00

NOTE
(0 to -10V) for MAS-1001-2; LSB = 10mV for MAS-1001-1, apply input voltage factor of 1/2.

Table 1. MAS-0801 and MAS-1001 Unipolar Operation for Options 1 and 2

Scale	Input Voltage	Complementary Offset Binary	Complementary Two's Complement
-FS -1LSB	-1.022V	1111 1111 11	0111 1111 11
-1/2 FS	-0.512V	1100 0000 00	0100 0000 00
0	-0.000V	1000 0000 00	0000 0000 00
+1/2 FS	+0.512V	0100 0000 00	1100 0000 00
+FS	+1.024V	0000 0000 00	1000 0000 00

NOTE
(-1.024V to +1.024V) for MAS-1001-5; LSB = 2mV.

Table 3. MAS-0801 and MAS-1001 Bipolar Operation for Option 5

Binary (BIN) in place of Complementary Binary (CBN) for options 1 and 2; Offset Binary (OBN) in place of Complementary Offset Binary (COB) for options 3, 4 and 5; Two's Complement (2SC) in place of Complementary Two's Complement (C2SC).

Scale	Input Voltage	Complementary Offset Binary	Complementary Two's Complement
-FS -1LSB	-4.9900V	1111 1111 11	0111 1111 11
-3/4 FS	-3.7500V	1110 0000 00	0110 0000 00
-1/2 FS	-2.5000V	1100 0000 00	0100 0000 00
0	0.0000V	1000 0000 00	0000 0000 00
+1/2 FS	+2.5000V	0100 0000 00	1100 0000 00
+3/4 FS	+3.7500V	0010 0000 00	1010 0000 00
+FS -1LSB	+4.9900V	0000 0000 01	1000 0000 01
+FS	+5.0000V	0000 0000 00	1000 0000 00

NOTES:
(-5V to +5V) for MAS-1001-3; LSB = 10mV for MAS-1001-4 apply input voltage factor of 2.

In Table 2, complementary 2SC is accomplished by factory option.

Table 2. MAS-0801 and MAS-1001 Bipolar Operation for Options 3 and 4

Scale	Input Voltage	Straight Binary
+FS -1LSB	+9.9976V	1111 1111 1111
+7/8 FS	+8.7500V	1110 0000 0000
+3/4 FS	+7.5000V	1100 0000 0000
+1/2 FS	+5.0000V	1000 0000 0000
+1/4 FS	+2.5000V	0100 0000 0000
+1LSB	+0.0024V	0000 0000 0001
0	0.0000V	0000 0000 0000

NOTE
Unipolar Operation (0 to +10V)

Table 4. MAS-1202 Unipolar Operation (0 to +10V)

Scale	Input Voltage	Straight Binary	Two's Complement
+FS -1LSB	+4.9976V	1111 1111 1111	0111 1111 1111
+3/4 FS	+3.7500V	1110 0000 0000	0110 0000 0000
+1/2 FS	+2.5000V	1100 0000 0000	0100 0000 0000
0	0.0000V	1000 0000 0000	0000 0000 0000
-1/2 FS	-2.5000V	0100 0000 0000	1100 0000 0000
-3/4 FS	-3.7500V	0010 0000 0000	1010 0000 0000
-FS +1LSB	-4.9976V	0000 0000 0001	1000 0000 0001
-FS	-5.0000V	0000 0000 0000	1000 0000 0000

NOTE
In Table 5, TWO'S COMPLEMENT (2SC) is accomplished by using the MSB output for Bit 1.

Table 5. MAS-1202 Bipolar Operation (-5V to +5V)

8-Bit Video Analog-to-Digital Converter

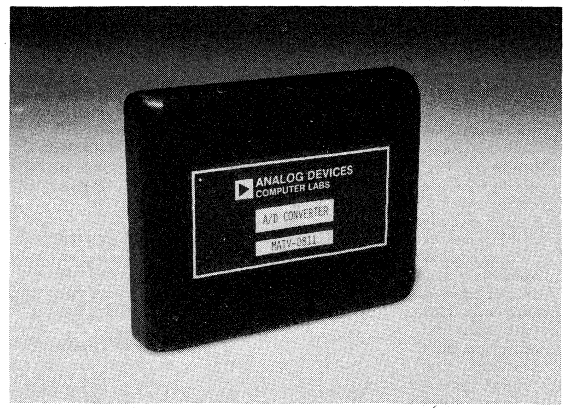
MATV-0811, -0816, -0820

FEATURES

- 8-Bit Accuracy – Guaranteed Monotonic
- Ultra-High Speed – dc to 20MHz Word Rates
- Most Economical Video A/D
- Smallest Available Complete A/D – 5.5″ X 4.38″ X 0.85″
- Self Contained – Includes Input Buffer, Encoder, Reference, Timing, and Buffered Parallel Output

APPLICATIONS

- Digitize Color Television at Up to Three or Four Times NTSC or PAL Color Subcarrier Frequencies
- Video Time Base Correction and Frame Synchronization
- Radar Signal Processing
- Real Time Transient and Continuous Spectrum Analysis

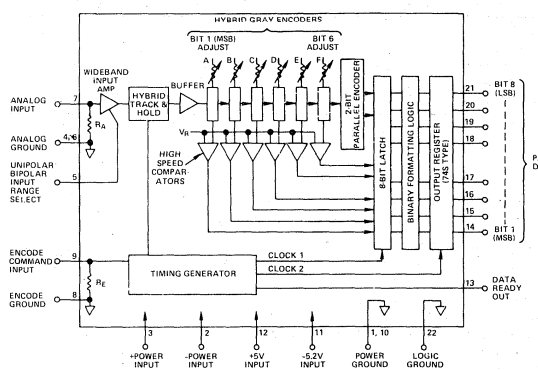


GENERAL DESCRIPTION

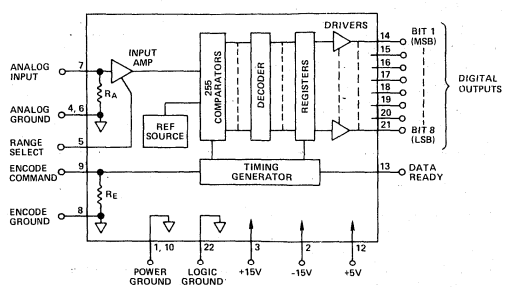
The Analog Devices' MATV series of A/D converters represent a major breakthrough in high-speed A/D technology. Providing conversion word rates from dc to 11MHz, 16MHz and 20MHz the MATV-0811, MATV-0816 and MATV-0820 are the lowest cost A/D converters in their performance class. As complete devices, they require only the addition of external power to accomplish precision video A/D conversion.

The use of internal hybrid microcircuit construction allows these modular A/D's to occupy a volume of only 21 cubic inches—about 1/5 the volume of available comparable devices. They are housed in metal cases which not only shield the circuits from external RF interference, but aid in efficient heat dissipation. A choice of analog input voltages is available, including the industry standard 0 to +1V at 75Ω. The encode command input, data ready output, and the digital bit outputs are all TTL compatible. Designed to operate from either ±12V or ±15V analog and +5V digital supplies (MATV-0811 and MATV-0816 also require -5.2V), the MATV series dissipate less than 8 watts. Their weight is < 10 ounces due to enclosure rather than encapsulation. This technique facilitates rapid, inexpensive factory repair and aids in reliable printed circuit board mounting by the customer without extensive mechanical constraints or system engineering.

Relative dc accuracy is 0.2% of full scale ±1/2LSB when operating over the frequency range of dc to 20MHz. The MATV series is designed to digitize color television signals at rates up to 20MHz and is also ideally suited for other analog to digital conversion requirements, such as radar signal processing, laser pulse analysis, transient analysis, and medical electronics applications where real-time analysis and display of large quantities of information are required.



MATV-0811, MATV-0816 Block Diagram



R_A AND R_E ARE DETERMINED BY THE ANALOG INPUT IMPEDANCE AND ENCODE COMMAND INPUT IMPEDANCE, RESPECTIVELY.

MATV-0820 Block Diagram

SPECIFICATIONS (typical @ +25°C and nominal power supply voltages unless otherwise noted)

MODEL	UNITS	MATV-0811	MATV-0816	MATV-0820
RESOLUTION (FS = Full Scale)	Bits/% FS	8/0.4	*	*
LSB Weight	% FS	0.4	*	*
ACCURACY (relative) at dc	typ	±0.15% ±1/2LSB	*[1]	*
	max	±0.2% ±1/2LSB	*[1]	*
Monotonicity		GUARANTEED	*	*
Differential Nonlinearity vs Temperature	% FS/°C	0.01	*	0.005
Linearity and Gain vs Temperature	% FS/°C	0.02	*	0.01
DYNAMIC CHARACTERISTICS				
AC Linearity @ Encode Rate[2]	MHz	11	15	20
Analog Input Frequency				
DC to 3.6MHz	Spurious Signals are			
	> dB below FS	50	*	*
3.6MHz to 5.5MHz		45	*	*
Conversion Rate (Encode Word Rate)	MHz max	11	16[1]	20
Conversion Time[3]	ns	150±20	120±20	35±10+1/Encode Rate
Aperture Uncertainty (Jitter)	ps max	±30	*	*
Aperture Time	ns	3	*	12
Signal to Noise Ratio				
(rms signal to rms noise)	dB min	48	*	*
(peak signal to rms noise)	dB min	58	*	*
Noise Power Ratio[4]	dB min	37	*	*
Transient Response[5]	ns	50	*	*
Overvoltage Recovery Time[6]	ns	60	*	*
Differential Gain[7]	%	3	*	*
Differential Phase	Degrees	1	*	*
Bandwidth				
Small Signal 3dB	MHz	20	*	*
Large Signal 3dB	MHz	15	*	*
Flat ±0.1dB, dc through	MHz	5.5	*	*
INPUT[8]				
Voltage Range				
Unipolar (Pin 5 Grounded)	V	0 to 1	*	*
Bipolar (Pin 5 open)	V	±0.5	*	*
Impedance (Terminated to Ground)	Ω	75	*	*
ENCODE COMMAND INPUT[8]				
Logic Levels, TTL Compatible		"0" = 0 to +0.4V	*	*
		"1" = +2.4V to +5V	*	*
Impedance (terminated to ground)	Ω	75 ±5%	*	*
Rise and Fall Times (10% to 90%) max	ns	10	*	*
Duration/Width 50% points (see timing diagram)	ns min	10	*	20
	ns max	50% duty cycle	40	*
Frequency (random or periodic)	dc to MHz	11	16	20
DIGITAL DATA OUTPUT[8]				
Format		Eight Parallel Bits NRZ		
Logic Levels, TTL		(Same as Encode Command)		
Drive Capability (not short circuit protected)	TTL Loads	10 Std	10 Schottky	
Time Skew	ns max	15	10	10
Coding		Straight Binary (BIN)		
DATA READY OUTPUT				
Format[9]		RZ	*	*
Logic Levels, TTL		(Same as Encode Command)		
Drive Capability		10 Std	10 Schottky	
Width	ns	40±10	35±5	25±5
POWER REQUIREMENTS[10]				
MATV-0811, MATV-0816/MATV-0820				
+15V ±2%/+11.8V to +15.5V	mA max	210	*	70
−15V ±2%/−11.8V to −15.5V	mA max	180	*	400
+5V ±5%/+5V +5%	mA max	450	540	200
−5.2V ±5%	mA max	280	*	N/A
TEMPERATURE RANGE				
Operating (case)	°C	0 to +70	*	*
Storage	°C	−55 to +85	*	*

*Same as MATV-0811.

NOTES:

[1] Applies to a customer specified operating frequency, ±10%. Outside this range, accuracy may degrade to ±0.3% ±1/2LSB.

[2] AC linearity expressed in terms of spurious in-band signals generated at specified encode rates.

[3] Pipeline delay not related to encode rate.

[4] DC to 5MHz while noise BW with slot frequency at 500kHz.

[5] Time to achieve 8-bit (0.2%) accuracy after F.S. step input.

[6] For signals not exceeding 10% overvoltage, the A/D will recover to 8-bit accuracy within 60ns after the signal returns to the specified range. Overvoltage inputs greater than 150% of F.S. may damage input circuits and should be avoided.

[7] At maximum encode rate, 20 IRE unit subcarrier, not including quantization effects.

[8] Consult factory for other voltage, impedance and logic level options.

[9] The leading edge of the data ready pulse occurs approximately 10ns before output data changes. The trailing edge is recommended for strobing data into external circuits.

[9] For MATV-0811, the leading edge of the Data Ready pulse occurs approximately 15ns before output data changes. The trailing edge is recommended for strobing data into external circuits.

For MATV-0816, the leading edge of the Data Ready pulse occurs approximately 10ns before output data changes. The trailing edge is recommended for strobing data into external circuits.

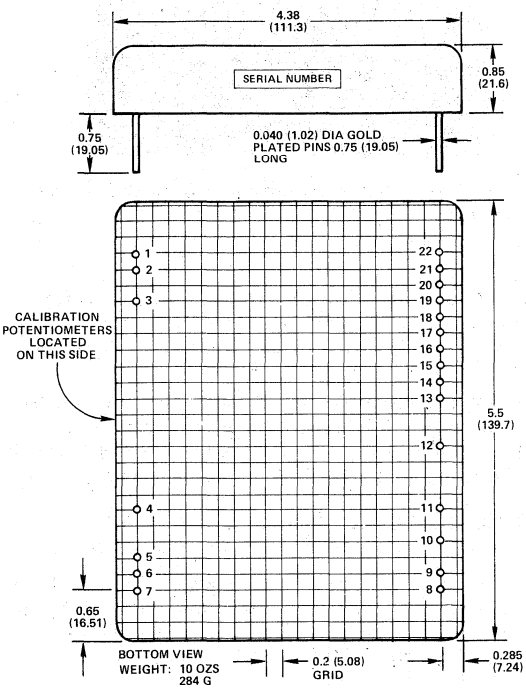
For MATV-0820, the leading edge of the Data Ready pulse occurs approximately simultaneously with output data changes. The trailing edge is recommended for strobing data into external circuits. This provides a minimum of 20ns set-up time for external registers.

[10] The A/D's are calibrated at the factory at either ±12V or ±15V as a no-cost option. Other operating voltages within this range may be specified by the user at slight additional cost.

Specifications subject to change without notice.

MECHANICAL OUTLINE AND DIMENSIONS

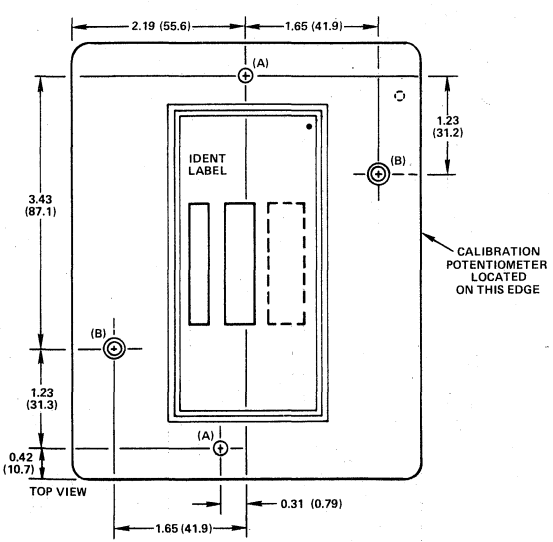
Dimensions shown in inches and (mm)



PINS ARE GOLD PLATED PER MIL-G-5204, TYPE II

NOTES:
DIMENSIONS AND LOCATION OF HOLD DOWN HOLES FOR MATV-0820 ARE SHOWN ON THE MECHANICAL OUTLINE FIGURE BELOW. NOT AVAILABLE ON MATV-0811 AND -0816.

DOT ON TOP INDICATES POSITION OF PIN 1.



(A) LOCATIONS ARE HOLES (0.16" TO 0.18" DIA.) THRU THE A/D SUITABLE FOR SECURING THE UNIT TO A MOTHER BOARD, ETC.
(B) LOCATIONS ARE EQUIPPED WITH #6-32 CLINCH NUTS (0.3" DEEP) SUITABLE FOR ATTACHING HEAT SINK, ETC.

DOT ON TOP INDICATES POSITION OF PIN 1.

MATV SERIES
PIN DESIGNATIONS

PIN	FUNCTION	COMMENTS
1	POWER GROUND	*
2	- POWER INPUT	-11.8V (MIN); -16.5V (MAX)
3	+ POWER INPUT	+11.8V (MIN); +16.5V (MAX)
4	ANALOG GROUND	*
5	RANGE SELECT	UNIPOLAR = GROUND BIPOLAR = OPEN
6	ANALOG GROUND	*
7	ANALOG INPUT	OPTIONAL
8	ENCODE GROUND	*
9	ENCODE COMMAND	TTL, +5V (MAX)
10	POWER GROUND	*
11	NO CONNECTION 0820 -5.2V POWER INPUT 0811, 0816	 -5V (MIN), -5.5V (MAX)
12	+5V POWER INPUT	+4.75V (MIN); +5.25V (MAX)
13	DATA READY OUTPUT	TTL LEVELS
14	BIT 1 OUTPUT (MSB)	TTL LEVELS
15	BIT 2 OUTPUT	TTL LEVELS
16	BIT 3 OUTPUT	TTL LEVELS
17	BIT 4 OUTPUT	TTL LEVELS
18	BIT 5 OUTPUT	TTL LEVELS
19	BIT 6 OUTPUT	TTL LEVELS
20	BIT 7 OUTPUT	TTL LEVELS
21	BIT 8 OUTPUT (LSB)	TTL LEVELS
22	DIGITAL LOGIC GND.	*

*ALL GROUNDS ARE INTERNALLY CONNECTED

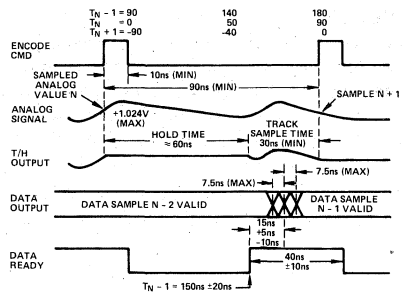


Figure 1. MATV-0811 Timing Diagram at Maximum Sample Rate of 11MHz

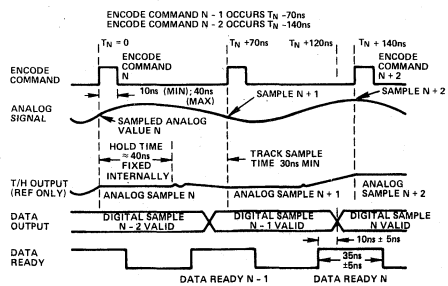
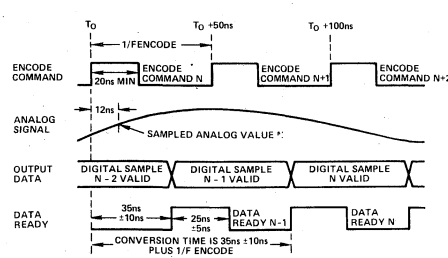


Figure 2. MATV-0816 Timing Diagram at Sample Rate of 14.3MHz



NOTE:
2 ENCODE COMMAND PULSES ARE REQUIRED TO OBTAIN FIRST "DATA READY".

Figure 3. MATV-0820 Timing Diagram Shown at an Encode Frequency of 20MHz

11

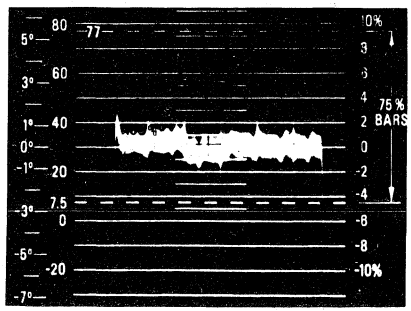


Figure 4. Typical Differential Gain of MATV-0816 Operating at 15MHz Word Rates

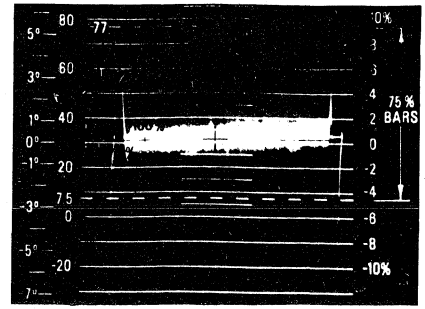


Figure 5. Typical Differential Phase of MATV-0816 Operating at 15MHz Word Rates

ORDERING INFORMATION

Each MATV series A/D converter will be calibrated at ±15V as a standard. Order by model number either MATV-0811, MATV-0816 or MATV-0820.

Optional Versions

The MATV series A/D's are available with a variety of options, including analog input range and impedance, encode command input impedance, encode word rate, power supply voltage calibration, etc. Any option other than what is shown on the data sheet will have longer delivery, since each non-standard device is built on a per order basis.

A complete listing of optional designators is available from either the factory or your local Analog Devices' sales office.

Device Marking

The MATV series A/D that you order will be marked with a series of alphanumerics which specifically designate the options built into the device. For the standard devices, these will be as follows:

MATV-0811 will be marked MATV-0811-1-BIN-15 for older devices, or MATV-0811-AA150 for newer devices.

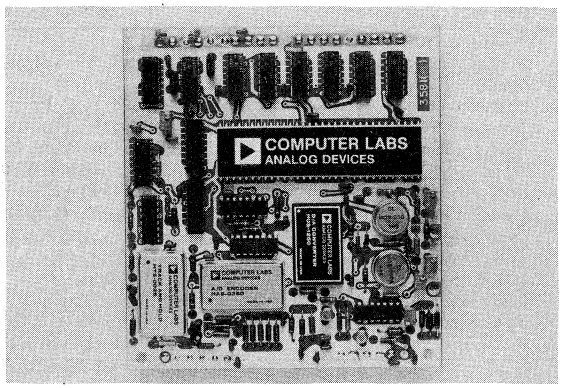
MATV-0816 will be marked MATV-0816-0175 BIN 75143150 for older devices, or MATV-0816 ABBA143150 for newer devices.

MATV-0820 will be marked MATV-0820-0175 BIN 75 for older devices, or MATV-0820 ABAA for newer devices.

This information is provided so that there will be no confusion as to why information other than the basic model number appears on the device identification label, which might cause problems at a customers' incoming inspection.

10-Bit Video Analog to Digital Converter

MOD-1005



FEATURES

- 10 Bits @ 5MHz Word Rate
- One-27 Sq. In. PC Board
- Built-In Track-and-Hold — 25ps Aperture Uncertainty
- 20MHz Analog Input Bandwidth
- TTL Compatible
- Low (10-Watt) Power Dissipation
- Signal-To-Noise Ratio Greater Than 58dB
- Noise Power Ratio Greater Than 49dB
- Completely Repairable

APPLICATIONS

- Radar Digitizing
- Digital Communications
- Real Time Spectrum Analysis
- High Resolution TV

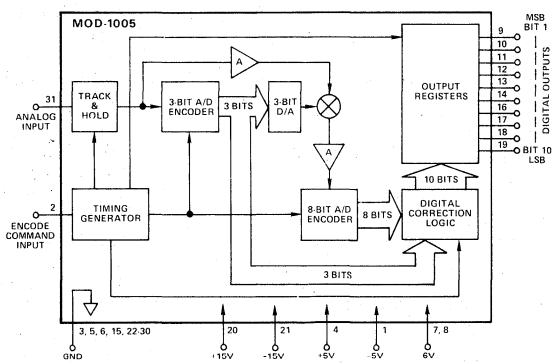
GENERAL DESCRIPTION

Analog Devices' model MOD-1005 is a very high-speed A/D converter capable of digitizing video input signals to 10-bit accuracy at random or periodic word rates of dc through 5MHz. The MOD-1005 is truly a breakthrough in high-speed A/D technology. It is the most cost effective A/D in this speed category, combining small size and low power dissipation with low cost.

The MOD-1005 is constructed on a single printed circuit card which is intended for mounting on a system mother-board, and occupies only 27 square inches. Within this A/D is the required sample/track and hold amplifier, encoder, timing circuits and output latches for a true simultaneous, all-parallel digital output.

The encode command input and digital outputs are TTL compatible. The A/D requires only an external encode command pulse and external power supplies for operation. NO external parts are required. Gain and offset potentiometers are provided on the card. The A/D is fully repairable either at the factory or in the field.

The MOD-1005 is ideally suited for systems requiring the ultimate in conversion speed and accuracy. Such applications include radar digitizing, digital communications, spectrum analysis, and many others. Each MOD-1005 is backed by Analog Devices' limited one year warranty.



Block Diagram

11

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

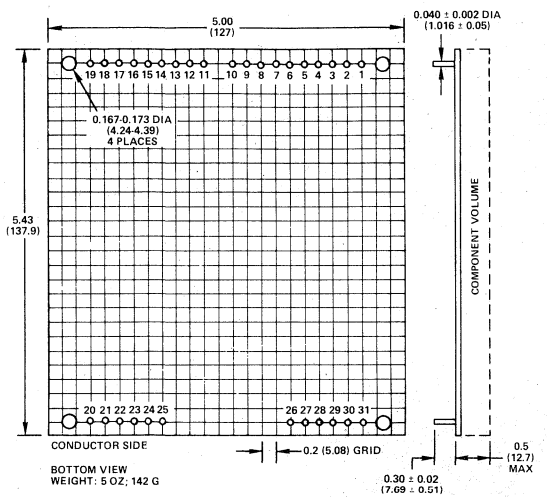
MODEL	MOD-1005
RESOLUTION (FS = FULL SCALE)	10 Bits (0.1% FS)
LSB WEIGHT	4mV
ACCURACY (INCLUDING LINEARITY) @ DC	±0.05% Full Scale ±1/2LSB
Monotonicity	Guaranteed
Differential Nonlinearity vs. Temperature	0.0005% of FS/°C
Gain vs. Temperature	0.01% of FS/°C
DYNAMIC CHARACTERISTICS	
AC Linearity[1]	Spurious Signals >59dB below FS
Conversion Time	See Text
Conversion Rate (Word Rate)	dc to 5MHz
Aperture Uncertainty (Jitter)	±25ps max
Aperture Time	45ns (±10ns from unit to unit)
Signal to Noise Ratio (rms signal to rms noise)	58dB min at 500kHz analog input
Noise Power Ratio[2]	49dB min
Transient Response (Full Scale Step Input)	10-Bit (0.05%) Accuracy within 50ns
Overvoltage Recovery Time	
Recovers to 10-bit accuracy after 2 X FS input overvoltage in	200ns
Input Bandwidth (small signal, 3dB)	20MHz min
Input Bandwidth (large signal, 3dB)	15MHz min flat within ±0.1dB, dc through 5MHz
INPUT	
Voltage Range	±2.048V FS ±4V Absolute max
Impedance	50Ω
Offset Voltage	Adjust to 0 with On Board Potentiometer
Offset vs. Temperature	0.01% Full Scale/°C
Bias Current	1nA max
ENCODE COMMAND INPUT	
Logic Levels, TTL Compatible	"0" = 0 to +0.4V "1" = +2.4V to +5V
Logic Loading	2 Standard TTL Gates
Rise and Fall Times	10ns max
Duration Min/Max	20ns/60% of Duty Cycle
Frequency (Random or Periodic)	dc to 5MHz
Sample Delay	45ns (unit to unit tolerance is ±10ns)
DIGITAL DATA OUTPUT	
Format	10 Parallel Bits, NRZ
Logic Levels, TTL Compatible	"0" = 0 to +0.4V "1" = +2.4V to +5V
Drive (Not Short Circuit Protected)	Up to 1 Schottky TTL or 2 Standard TTL Loads
Time Skew	10ns max
Coding	2's Complement (2SC)
Conversion Time	See Text on the Next Page
POWER REQUIREMENTS	typ/max
+15V ±5%	150/170mA
-15V ±5%	150/170mA
-6V ±4%	300/350mA
+5V ±5%	350/400mA
-5V ±5%	500/550mA
Power Consumption	10 Watts
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	-55°C to +85°C
Cooling Requirements	100 Linear Feet Per Min (LFPM)
PHYSICAL CHARACTERISTICS	
Construction	Single Printed Circuit Card

NOTES:
[1] AC linearity expressed in terms of spurious in-band signals generated as specified encode rates, with dc to 2.5MHz analog input.
[2] DC to 2.4MHz white noise BW with Slot frequency of 512kHz.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches (mm).



PIN DESIGNATIONS

PIN	FUNCTION
1	-5V
2	ENCODE COMMAND
3	GND*
4	+5V
5	GND*
6	GND*
7	-6V
8	-6V
9	BIT 1 MSB
10	BIT 2
11	BIT 3
12	BIT 4
13	BIT 5
14	BIT 6
15	GND*

PIN	FUNCTION
16	BIT 7
17	BIT 8
18	BIT 9
19	BIT 10 LSB
20	+15V
21	-15V
22	GND*
23	GND*
24	GND*
25	GND*
26	GND*
27	GND*
28	GND*
29	GND*
30	GND*
31	ANALOG INPUT

*ALL GROUND PINS ARE CONNECTED TOGETHER WITHIN THE MOD-1005

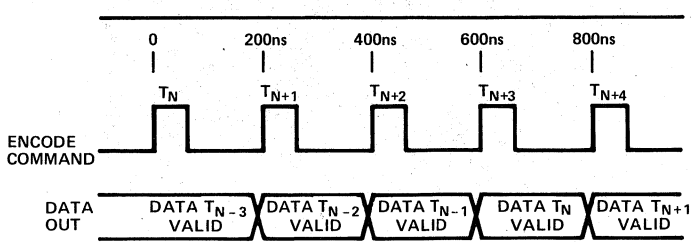
ORDERING INFORMATION

Order model number MOD-1005 A/D converter. Mating pin sockets for the MOD-1005 are model number MSB-2 (31 required per A/D).

CONVERSION TIME

Output data is valid two encode command clock periods plus 200ns after application of an initial encode command pulse. Due to the pipeline delay effect of the A/D, a total of three encode command pulses are required to shift the data to the output of the A/D. For example, with a 5MHz encode rate, data is valid 600ns after the application of the first encode command pulse — assuming that two pulses occur after the first.

Use of the trailing edge of the encode command is recommended for strobing output data into external register (see Figure 1).



DATA T_N (THE RESULT OF ENCODE COMAND T_N) OCCURS TWO CONVERSION PERIODS PLUS 200ns AFTER ENCODE COMMAND T_N. FOR A 5MHz WORD RATE AS SHOWN, DATA IS VALID 200ns AFTER THE THIRD ENCODE COMMAND PULSE OR T_N + 600ns. IN ALL CASES, THREE ENCODE COMMAND PULSES ARE REQUIRED FOR TRANSFER OF DATA TO THE OUTPUT, DUE TO THE PIPELINE DELAY EFFECT THROUGH THE A/D. NO DATA READY PULSE IS SUPPLIED.

Figure 1. MOD-1005 Timing Diagram

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GROUND CONNECTIONS

It should be noted that the MOD-1005 PC board has 13 ground pins. These are all connected to the ground plane on the board. For best results it is recommended that ALL of these pins be connected to a massive system or "mother board" ground plane.

CALIBRATION PROCEDURE (MOD-1005)

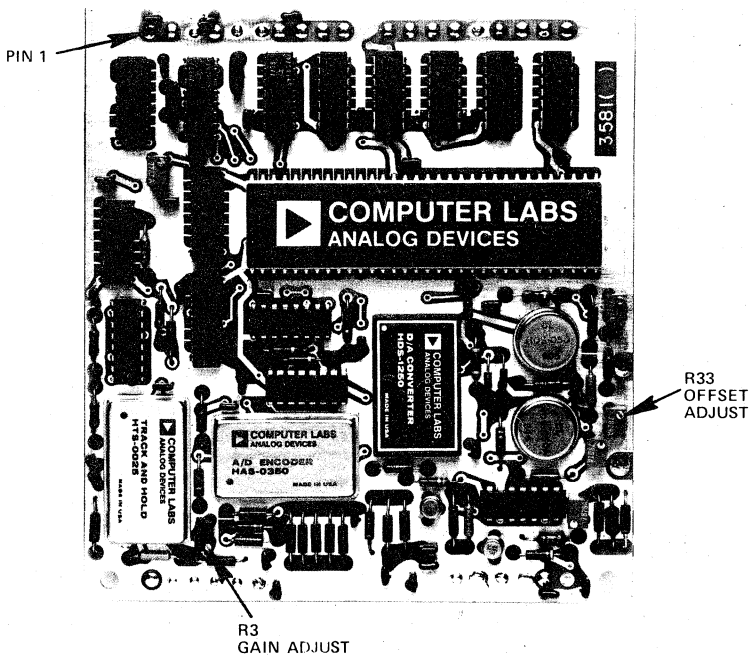
The MOD-1005 A/D is precisely calibrated at the factory before shipment, and should need no further calibration. However, if slight readjustments of the A/D are required in the system, the following procedure should be followed. It should be remembered that the output coding of this A/D is 2SC.

Offset Adjustment

The offset is adjusted by varying potentiometer R33 with 0 volts applied to the analog input. To obtain the proper output code, observe that the digital output is changing between 1 1 1 1 1 1 1 1 1 1 and 0 0 0 0 0 0 0 0 0 0 at this adjustment level. When properly adjusted a digital code of 0 0 0 0 0 0 0 0 0 0 will represent analog input 1LSB above zero volts, and a digital code of 1 1 1 1 1 1 1 1 1 1 will represent an analog input of 1LSB below zero volts.

Gain Adjustment

The gain is adjusted by varying potentiometer R3. This adjustment is made by applying +2.042V (FS -1 1/2LSB) to the analog input and while monitoring the digital output, adjust R3 for the output code varying between 0 1 1 1 1 1 1 1 1 0 and 0 1 1 1 1 1 1 1 1 1 (FS). If the user needs to offset the entire range of the A/D, this can be accomplished by readjusting R33 as required. However, in this procedure, the offset should always be adjusted first.



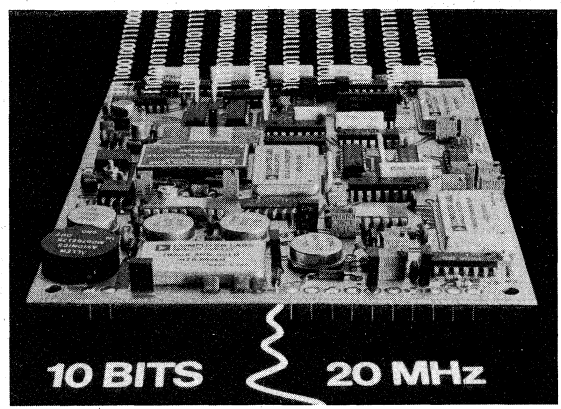
A/D Converter Assembly

10-Bit Video Analog to Digital Converter

MOD-1020

FEATURES
10-Bits @ 20MHz Word Rates
One 35 Sq. In. PC Board
Built-In Track-and-Hold — 25ps Aperture
15MHz Large-Signal Input Bandwidth
ECL Compatible
Signal-to-Noise Ratio Greater Than 56dB
Noise Power Ratio Greater Than 45dB

APPLICATIONS
Television Digitizing
Radar Digitizing
Medical Instrumentation
Digital Communications
Spectrum Analysis
Sonar Digitizing



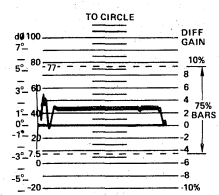
GENERAL DESCRIPTION

The Analog Devices' model MOD-1020 is an ultra-high-speed A/D converter capable of digitizing video input signals to 10-bit accuracy at word rates through 20MHz. The MOD-1020 is another in the series of state-of-the-art A/D converters from Analog Devices that employs the unique digital correcting subranging (DCS) conversion technique to virtually eliminate errors normally associated with subranging type A/D converters. No other A/D converter commercially available offers the user the speed and accuracy attainable with the MOD-1020.

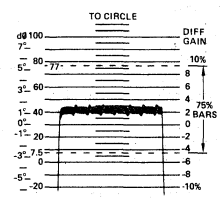
The MOD-1020 is constructed on a single printed circuit card which is intended for mounting on a system mother board and occupies only 35 square inches. The A/D is complete with internal track-and-hold, encoder, timing circuitry, references, and latched output. It produces a true all-parallel digital output.

The encode command input, digital outputs, and data ready output are balanced ECL compatible. The A/D requires only an external encode command input pulse and external power supplies for operation. The analog input impedance is at least 500Ω, so that the user can easily terminate the A/D with lower impedances in his system. Gain and offset potentiometers are provided on the card so that the A/D can be operated in either the unipolar or bipolar modes. The A/D is fully repairable.

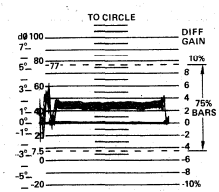
The MOD-1020 is ideally suited for systems requiring the ultimate in conversion speed and accuracy. Such applications include radar digitizing, digital communications (baseband digitizing), composite color television digitizing, spectrum analysis, medical instrumentation, and many others. Each MOD-1020 is backed by Analog Devices' limited one-year warranty.



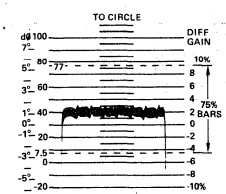
Differential Phase — Generator and Vectorscope Back-to-Back No A/D Conversion



Differential Gain — Generator and Vectorscope Back-to-Back No A/D Conversion



Differential Phase — Model MOD-1020 ADC and Model 4120E DAC Back-to-Back 14.4MHz Conversion (Word) Rate



Differential Gain — Model MOD-1020 and Model 4120E DAC Back-to-Back 14.4MHz Conversion (Word) Rate

The above waveforms were obtained utilizing a Tektronix Model 149A N.T.S.C. Test Signal Generator with a 20 IRE unit TV test signal output. The display (output) was obtained using a Tektronix Model 520A Vectorscope.

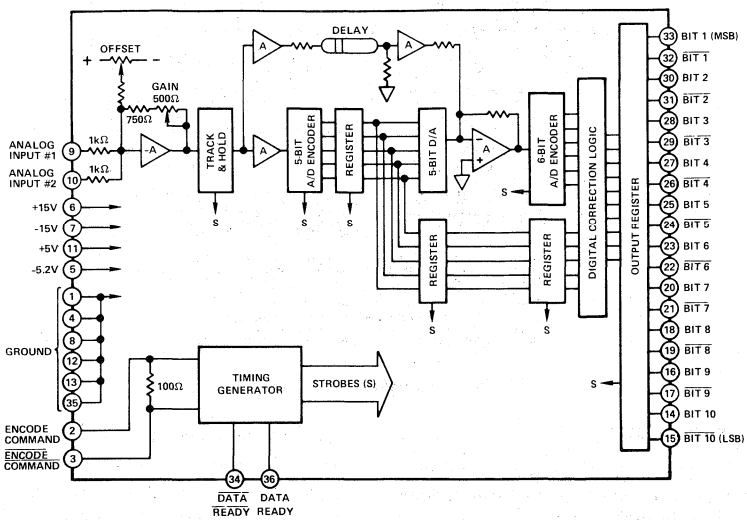
11

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

MODEL	MOD-1020
RESOLUTION (FS = FULL SCALE)	10 Bits (0.1% FS)
LSB WEIGHT	1mV or 2mV Depending on Analog Input Range
ACCURACY (INCLUDING LINEARITY) @ DC	±0.05% Full Scale ±1/2LSB
Monotonicity	Guaranteed 0 to +70°C
Nonlinearity vs. Temperature	0.0005% of FS/°C
Gain vs. Temperature	0.015% of FS/°C
DYNAMIC CHARACTERISTICS	
AC Linearity[1] (dc to 1MHz)	Spurious Signals ≥60dB below FS
(1MHz to 5MHz)	Spurious Signals ≥55dB below FS
(5MHz to 10MHz)	Spurious Signals ≥50dB below FS
Conversion Time	See Text and Timing Diagram
Conversion Rate[2]	dc to 20MHz (See Note and Ordering Information)
Aperture Uncertainty (Jitter)	±25ps max
Aperture Time (Delay)	5ns (±2ns unit-to-unit tolerance)
Signal to Noise Ratio[3]	56dB min
Signal to Noise Ratio[4]	65dB min
Noise Power Ratio[5]	45dB min, 47dB typ
Transient Response[6]	50ns
Overvoltage Recovery[7]	50ns
Input Bandwidth (small signal, 3dB)[8]	30MHz
Input Bandwidth (large signal, 3dB)[9]	15MHz; Flat within 0.2dB, dc to 10MHz
Two-Tone Linearity (@ Input Frequency);	
60kHz; 62kHz	In-Band Spurious Signals ≥60dB below FS
4.998MHz; 5.000MHz	In-Band Spurious Signals ≥55dB below FS
9.996MHz; 9.998MHz	In-Band Spurious Signals ≥50dB below FS
Differential Gain[10]	1% with 20 IRE Unit Reference
Differential Phase[10]	0.5° with 20 IRE Unit Reference
ANALOG INPUT (See Notes on Input Range in Text)	
Voltage Range	1V p-p or 2V p-p, Depending on Hook-Up
	Either Unipolar or Bipolar
	±4V Absolute max Input
Impedance	1000Ω (2V Input Range)
	500Ω (1V Input Range)
Offset	Adjustable to Zero with On-Card Potentiometer (R4)
Offset vs. Temperature	0.01%/°C
ENCODE COMMAND INPUT	
Logic Levels, ECL Compatible	"0" = -1.7V
(Balanced Input)	"1" = -0.9V
Impedance	100Ω Line-to-Line
Rise and Fall Times	5ns max
Duration (min/max)	10ns/70% of Duty Cycle
Frequency	Specified by Customer, dc to 20MHz (See Ordering Information)
DIGITAL OUTPUT DATA	
Format	10 Parallel Bits, NRZ
Logic Levels, ECL Compatible	"0" = -1.7V
(Balanced Outputs)	"1" = -0.9V
Drive	75Ω to 100Ω, Line-to-Line
Time Skew	5ns max
Coding	Binary (BIN); 2's Complement (2SC)
DATA READY OUTPUT	
Logic Level, ECL Compatible	"0" = -1.7V
(Balanced Output)	"1" = -0.9V
Rise and Fall Times	5ns max
Duration	25ns ±3ns
Conversion Time	Output data is valid two clock perios plus 185 ±20ns after the application of an initial Encode Command pulse—assuming that two pulses occur after the first. Use of the trailing edge of the Data Ready pulses are required to shift the data to the output. For example, with a 20MHz encode rate, data is valid 285 ±20ns after the application of the first Encode Command pulse—assuming that two pulses occur after the first. Use of the trailing edge of the Data Ready pulse is recommended for strobing output data into external registers.
POWER REQUIREMENTS	
+15V ±5%	200mA
-15V ±5%	200mA
+5V ±5%	100mA
-5.2V ±5%	2.7A
Power Consumption	21 Watts
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	-55°C to +85°C
Cooling Requirements	500 Linear Feet per Minute (LFPM)
PHYSICAL CHARACTERISTICS	
Construction	Single Printed Circuit Card

NOTES:
[1] AC linearity expressed in terms of spurious in-band signals generated at 20MHz encode rate at the analog frequencies ( ) shown.
[2] To be specified by the customer. See text and ordering information.
[3] RMS signal to rms noise ratio with 500kHz analog input.
[4] Peak-to-peak signal to rms noise ratio with 500kHz analog input.
[5] DC to 8.2MHz white noise bandwidth with slot frequency of 3.886MHz and an encode rate of 20MHz.
[6] Recovers to 10-bit accuracy after 2 X FS input overvoltage in time specified.
[7] For full-scale step input, attains 10-bit accuracy in time specified.
[8] With analog input signal 40dB below FS.
[9] With FS analog input.
[10] Applies to devices optimized for video applications. Differential gain and phase are measured and optimized for ADC's which have the following encode rate optional designators (see Ordering Information): "107" (3 X NTSC subcarrier); "133" (3 X PAL); "143" (4 X NTSC); "177" (4 X PAL).

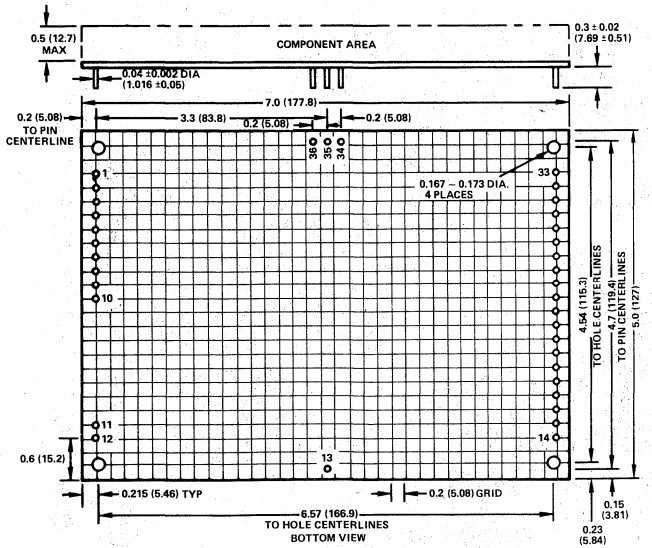
Specifications subject to change without notice.



MOD-1020 Block Diagram

OUTLINE DIMENSIONS

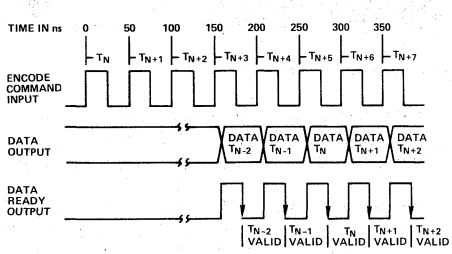
Dimensions shown in inches and (mm).



PIN DESIGNATIONS

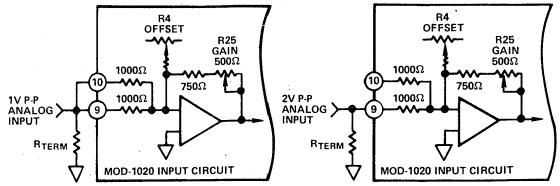
PIN	FUNCTION	PIN	FUNCTION
1	GROUND	19	$\overline{\text{BIT 8}}$
2	ENCODE COMMAND	20	BIT 7
3	$\overline{\text{ENCODE COMMAND}}$	21	$\overline{\text{BIT 7}}$
4	GROUND	22	$\overline{\text{BIT 6}}$
5	-5.2V	23	BIT 6
6	+15V	24	$\overline{\text{BIT 5}}$
7	-15V	25	$\overline{\text{BIT 5}}$
8	GROUND	26	$\overline{\text{BIT 4}}$
9	ANALOG INPUT #1	27	BIT 4
10	ANALOG INPUT #2	28	BIT 3
11	+5V	29	$\overline{\text{BIT 3}}$
12	GROUND	30	BIT 2
13	GROUND	31	$\overline{\text{BIT 2}}$
14	BIT 10	32	$\overline{\text{BIT 1}}$
15	$\overline{\text{BIT 10}}$	33	BIT 1
16	BIT 9	34	DATA READY
17	$\overline{\text{BIT 9}}$	35	GROUND
18	BIT 8	36	DATA READY

ALL GROUND PINS ARE CONNECTED TOGETHER WITHIN THE ADC.



OUTPUT DATA ARE VALID TWO CLOCK PERIODS PLUS 185 ±20ns AFTER THE APPLICATION OF AN INITIAL ENCODE COMMAND PULSE. DUE TO THE PIPE-LINE DELAY EFFECT THROUGH THE A/D, A TOTAL OF THREE ENCODE COMMAND PULSES ARE REQUIRED TO SHIFT THE DATA TO THE OUTPUT. IN THIS EXAMPLE, WITH AN ENCODE RATE OF 20MHz, DATA ARE VALID 285 ±20ns AFTER THE APPLICATION OF THE FIRST ENCODE COMMAND PULSE. THIS ASSUMES THAT TWO ADDITIONAL ENCODE COMMAND PULSES OCCUR AFTER THE FIRST, AS SHOWN. THE OUTPUT DATA CHANGES STATE TWO ENCODE PERIODS PLUS 160 ±20ns AFTER THE APPLICATION OF THE FIRST ENCODE COMMAND PULSE. AS SHOWN, THE TRAILING EDGE OF THE DATA READY PULSE IS RECOMMENDED FOR STROBING OUTPUT DATA INTO EXTERNAL REGISTERS. IN THESE WAVEFORMS, THE ENCODE COMMAND AND DATA READY REFER TO THE POSITIVE "TRUE" INPUT AND OUTPUTS.

MOD-1020 Timing Diagram



ZIN	RTERM
50Ω	56.2Ω
75Ω	88.7Ω
93Ω	115.0Ω

1V P-P INPUT OPTION

(RTERM RESISTORS ARE 1%, 1/8W, MF)

ZIN	RTERM
50Ω	52.3Ω
75Ω	80.6Ω
93Ω	102.0Ω

2V P-P INPUT OPTION

FOR 1V P-P INPUT RANGE, CONNECT ANALOG INPUT TO PIN 9, AND CONNECT PINS 9 AND 10 TOGETHER. UNTERMINATED INPUT IMPEDANCE IS 500Ω. GAIN ADJUSTMENT RANGE (R25) IS ±20% MIN. FOR 2V P-P INPUT RANGE, CONNECT ANALOG INPUT TO PIN 9. PIN 10 IS LEFT DISCONNECTED. UNTERMINATED INPUT IMPEDANCE IS 1000Ω. GAIN ADJUSTMENT RANGE (R25) IS ±20%.

TO OBTAIN THE DESIRED TERMINATED INPUT IMPEDANCE, CONNECT THE APPROPRIATE EXTERNAL TERMINATING RESISTOR BETWEEN THE ANALOG INPUT PIN(S) AND GROUND, AS SHOWN IN THE ABOVE EXAMPLES. INPUT IMPEDANCES GREATER THAN 100Ω WILL RESULT IN LOSS OF INPUT BANDWIDTH AND SHOULD BE AVOIDED.

THE OFFSET POTENTIOMETER (R4) HAS SUFFICIENT RANGE TO ALLOW THE USER TO OPERATE THE ADC IN EITHER THE UNIPOLAR OR BIPOLAR MODE. THE ADC'S ARE CALIBRATED IN THE BIPOLAR CONFIGURATION AT THE FACTORY.

MOD-1020 Analog Input Range Options

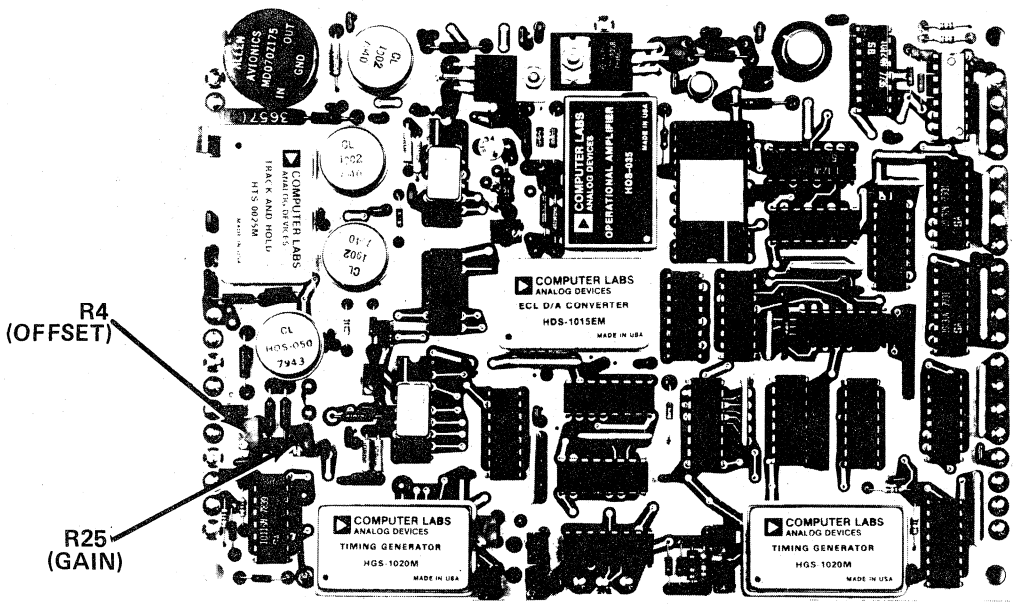
OFFSET AND GAIN ADJUSTMENT

The offset of the ADC is adjusted by varying potentiometer R4. Apply an input voltage to the analog input corresponding to positive full scale. Adjust R4 such that the digital output is changing between 1111111111 and 1111111110.

The gain of the ADC is adjusted by varying potentiometer R25. Apply an input voltage to the analog input that corresponds to negative full scale. Adjust R25 such that the digital output is changing between 0000000000 and 0000000001.

In the foregoing, the ADC is calibrated to have a unipolar positive transfer function. If bipolar input range is required, adjust R4 to offset the entire input by one-half of the full scale input.

In setting the gain, always adjust R4 first to obtain the correct setting for full scale positive input.



Location of Adjustment Potentiometers

ORDERING INFORMATION

IMPORTANT—THE ENCODE RATE OF THE MOD-1020 MUST BE SPECIFIED BY THE CUSTOMER AS SHOWN BELOW:

ORDER MODEL NUMBER: MOD-1020- "XXX", where "XXX" is to be specified by the customer. "XXX" represents the encode word rate in MHz with the decimal place assumed to be (but not shown) between the second and third places. Full 10-bit accuracy will be maintained within ±12% of this specified frequency, up to a maximum of 21MHz. For example, a device specified as MOD-1020-200 is for operation at 20.0MHz and will maintain accuracy from 17.6MHz to 21MHz.

For encode rates of 10MHz or less, the MOD-1020 will maintain full accuracy from dc to 10MHz. For encode frequencies of 10MHz or less, order MOD-1020-100.

Mating sockets for the MOD-1020 are model number MSB-2 (36 required per A/D).

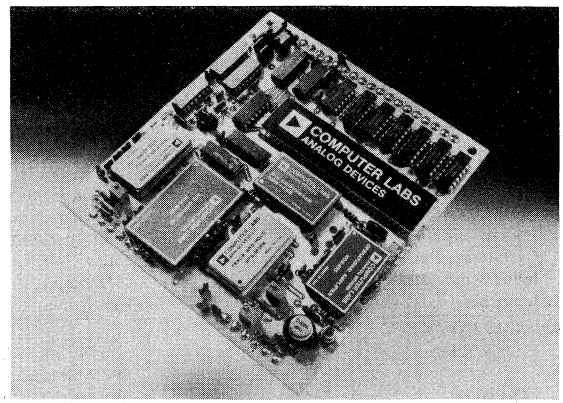
ANALOG DEVICES

12-Bit Video Analog to Digital Converter

MOD-1205

FEATURES
- 12 Bits @ 5MHz Word Rate
- One-27 Sq. In. PC Board
- Built-In Track-and-Hold — 25ps Aperture Uncertainty
- 15MHz Analog Input Bandwidth
- TTL Compatible
- Low (13-Watt) Power Dissipation
- Signal-to-Noise Ratio Greater Than 66dB
- Noise Power Ratio Greater Than 56dB
- Completely Repairable

APPLICATIONS
- Radar Digitizing
- Digital Communications
- Real Time Spectrum Analysis
- Signature Analysis



GENERAL DESCRIPTION

Analog Devices' model MOD-1205 is a very high-speed A/D converter capable of digitizing video input signals to 12-bit accuracy at random or periodic word rates of dc through 5MHz. The MOD-1205 is truly a breakthrough in high-speed A/D technology. It utilizes the latest state-of-the-art conversion technique called digital correcting subranging (DCS) to effectively eliminate errors normally associated with subranging type ADCs. It is the most cost effective A/D in this speed category, combining small size and low power dissipation with low cost.

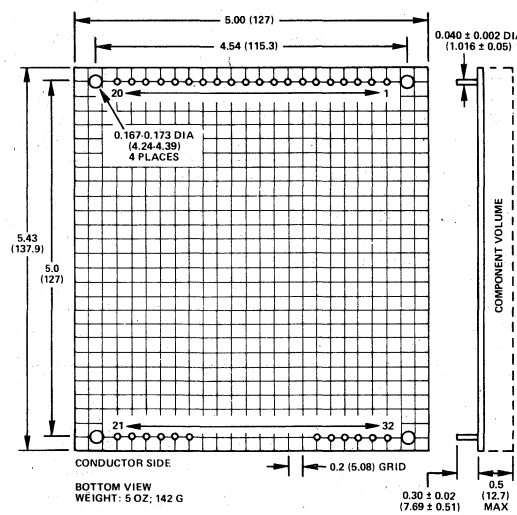
The MOD-1205 is constructed on a single printed circuit card which is intended for mounting on a system mother board and occupies only 27 square inches. Within this A/D is the required sample/track-and-hold amplifier, encoder, timing circuits and output latches for a true simultaneous, all-parallel digital output.

The encode command input and digital outputs are TTL compatible. The A/D requires only an external encode command pulse and external power supplies for operation. NO external parts are required. Gain and offset potentiometers are provided on the card. The A/D is fully repairable either at the factory or in the field.

The MOD-1205 is ideally suited for systems requiring the ultimate in conversion speed and accuracy. Such applications include radar digitizing, digital communications, spectrum analysis, and many others. Each MOD-1205 is backed by Analog Devices' limited one year warranty.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



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SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

MODEL	MOD-1205
RESOLUTION (FS = FULL SCALE)	12 Bits (0.024% FS)
LSB WEIGHT	1mV
ACCURACY (INCLUDING LINEARITY) @ DC	±0.0125% Full Scale ±1/2LSB
Monotonicity	Guaranteed (0 to +70°C)
Nonlinearity vs. Temperature	0.0005% of FS/°C, max
Gain vs. Temperature	0.002% of FS/°C, typ; 0.005% of FS/°C, max
DYNAMIC CHARACTERISTICS	
AC Linearity[1] (dc to 1MHz)	Spurious Signals >70dB below FS, max
(1MHz to 2.5MHz)	Spurious Signals >65dB below FS, max; >68dB, typ
Conversion Time	See Text and Timing Diagram
Conversion Rate (Word Rate)	dc to 5MHz
Aperture Uncertainty (Jitter)	±25ps max
Aperture Time	30ns (±10ns from unit to unit)
Signal to Noise Ratio[2]	66dB min; 68dB, typ
Noise Power Ratio[3]	56dB min, 58dB typ
Transient Response[4]	12-Bit (0.0125%) Accuracy within 200ns
Overvoltage Recovery Time[5]	200ns
Input Bandwidth (small signal, 3dB)	15MHz min
Input Bandwidth (large signal, 3dB)	10MHz min; flat within ±0.1dB, dc through 5MHz
ANALOG INPUT	
Voltage Range	±2.048V FS
	±4V Absolute max
Impedance	400Ω with pin 30 open, 50Ω with pin 30 grounded
Offset Voltage	Adjust to 0 with On Board Potentiometer
Offset vs. Temperature	0.002% FS/°C, typ; 0.005% of FS/°C, max
Bias Current	1nA max
ENCODE COMMAND INPUT	
Logic Levels, TTL Compatible	"0" = 0 to +0.4V
	"1" = +2.4V to +5V
Logic Loading	2 Standard TTL Gates
Rise and Fall Times	10ns max
Duration min/max	25ns/50% of Duty Cycle
Frequency (Random or Periodic)	dc to 5MHz
DIGITAL DATA OUTPUT	
Format	12 Parallel Bits, NRZ
Logic Levels, TTL Compatible	"0" = 0 to +0.4V
	"1" = +2.4V to +5V
Drive (Not Short Circuit Protected)	Up to 1 Schottky TTL or
	2 Standard TTL Loads
Time Skew	10ns max
Coding	Offset Binary (OBN) or 2's complement (2SC)
Conversion Time	See Text on the Next Page
POWER REQUIREMENTS	
+15V ±5%	200mA
-15V ±5%	150mA
-6V ±4%	700mA
+5V ±5%	800mA
Power Consumption	13 Watts
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	-55°C to +85°C
Cooling Requirements	500 Linear Feet Per Min (LFPM) @ +70°C
PHYSICAL CHARACTERISTICS	
Construction	Single Printed Circuit Card

NOTES:
[1] AC linearity expressed in terms of spurious in-band signals generated at specified encode rates at analog input frequencies ( ).
[2] rms signal to rms noise at 500kHz analog input.
[3] dc to 2.4MHz white noise bandwidth with slot frequency of 512kHz.
[4] For full-scale step input, attains 12-bit accuracy in time specified.
[5] Recovers to 12-bit accuracy after 2 X FS input overvoltage in time specified.

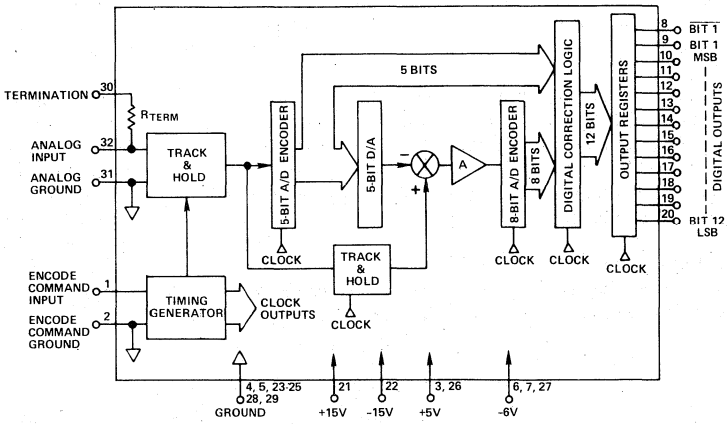
Specifications subject to change without notice.

PIN	FUNCTION
1	ENCODE COMMAND
2	GND*
3	+5V
4	GND*
5	GND*
6	-6V
7	-6V
8	$\overline{\text{BIT 1}}$
9	BIT 1 (MSB)
10	BIT 2
11	BIT 3
12	BIT 4
13	BIT 5
14	BIT 6
15	BIT 7
16	BIT 8

PIN	FUNCTION
17	BIT 9
18	BIT 10
19	BIT 11
20	BIT 12 (LSB)
21	+15V
22	-15V
23	GND*
24	GND*
25	GND*
26	+5V
27	-6V
28	GND*
29	GND*
30	TERMINATION
31	GND*
32	ANALOG INPUT

*ALL GROUND PINS ARE CONNECTED TOGETHER WITHIN THE MOD-1205

Pin Designations



NOTE: WITH PIN 30 OPEN, ANALOG INPUT IMPEDANCE IS 400Ω. WITH PIN 30 GROUNDED, ANALOG IMPEDANCE IS 50Ω.

MOD-1205 Block Diagram

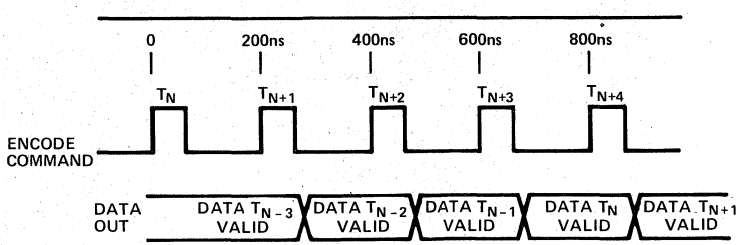
ORDERING INFORMATION

Order model number MOD-1205 A/D converter. Mating pin sockets for the MOD-1205 are model number MSB-2 (32 required per A/D).

CONVERSION TIME

Output data is valid two encode command clock periods plus 275ns ±25ns after application of an initial encode command pulse. Due to the pipeline delay effect of the A/D, a total of three encode command pulses are required to shift the data to the output of the A/D. For example, with a 5MHz encode rate, data is valid 675ns ±25ns after the application of the first encode command pulse—assuming that two pulses occur after the first.

Use of the trailing edge of the encode command is recommended for strobing output data into external register (see Figure 1).



DATA T_N (THE RESULT OF ENCODE COMMAND T_N) OCCURS TWO CONVERSION PERIODS PLUS 275ns ±25ns AFTER ENCODE COMMAND T_N. FOR A 5MHz WORD RATE AS SHOWN, DATA IS VALID 275ns ±25ns AFTER THE THIRD ENCODE COMMAND PULSE OR T_N + 675ns ±25ns. IN ALL CASES, THREE ENCODE COMMAND PULSES ARE REQUIRED FOR TRANSFER OF DATA TO THE OUTPUT, DUE TO THE PIPELINE DELAY EFFECT THROUGH THE A/D. NO DATA READY PULSE IS SUPPLIED.

Figure 1. MOD-1205 Timing Diagram

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GROUND CONNECTIONS

It should be noted that the MOD-1205 PC board has 9 ground pins. These are all connected to the ground plane on the board. For best results it is recommended that ALL of these pins be connected to a massive system or "mother board" ground plane.

CALIBRATION PROCEDURE (MOD-1205)

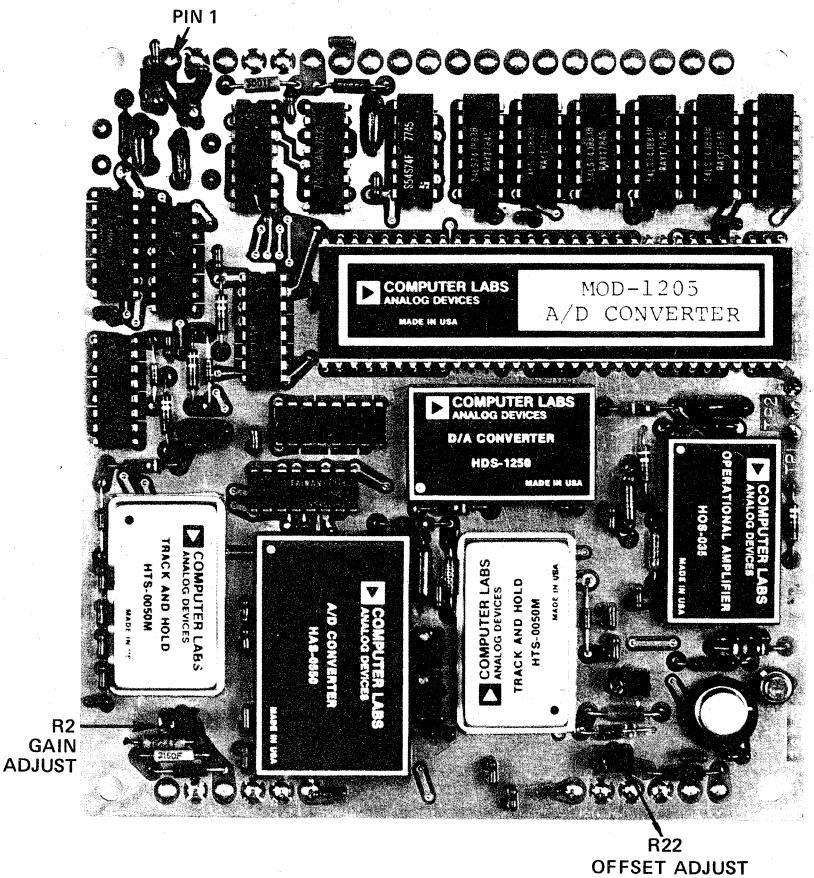
The MOD-1205 A/D is precisely calibrated at the factory before shipments and should need no further calibration. However, if slight readjustments of the A/D are required in the system, the following procedure should be followed. This procedure refers to a binary output.

Offset Adjustment

The offset is adjusted by varying potentiometer R22 with 0 volts applied to the analog input. To obtain the proper output code, observe that the digital output is changing between 1 0 0 0 0 0 0 0 0 0 0 0 and 0 1 1 1 1 1 1 1 1 1 1 1 at this adjustment level. When properly adjusted a digital code of 1 0 0 0 0 0 0 0 0 0 0 0 will represent analog input 1LSB above zero volts, and a digital code of 0 1 1 1 1 1 1 1 1 1 1 1 will represent an analog input of 1LSB below zero volts.

Gain Adjustment

The gain is adjusted by varying potentiometer R2. This adjustment is made by applying +2.0465V (FS -1 1/2LSB) to the analog input and while monitoring the digital output, adjust R2 for the output code varying between 1 1 1 1 1 1 1 1 1 1 1 0 and 1 1 1 1 1 1 1 1 1 1 1 1 (FS). If the user needs to offset the entire range of the A/D, this can be accomplished by a readjusting R22 as required. However, in this procedure, the offset should always be adjusted first.



Location of Adjustment Potentiometers

Voltage-to-Frequency & Frequency-to-Voltage Converters

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451 100kHz to 20kHz Adjustable Frequency to Voltage Converter	12-11
453 1kHz to 200kHz Adjustable Frequency to Voltage Converter	12-11
454 20kHz Voltage to Frequency Converter	12-7
456 10kHz Voltage to Frequency Converter	12-7
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460 1MHz Voltage to Frequency Converter	12-17

Selection Guide
Voltage-to-Frequency & Frequency-to-Voltage Converters

In this Selection Guide, V/F and F/V Converters are listed in separate tables, in order of increasing maximum frequency range. Complete descriptions, specifications, and applications information can be found in the data sheets. General information regarding VFCs and FVCs can be found in the following pages. Specifications are typical at rated supply voltage and load, and T_A = +25°C, except where noted.

VOLTAGE-TO-FREQUENCY CONVERTERS

Max F.S. Frequency	Model	Brief Description	Vol I Page	Vol II Page
10kHz	450	0.005% max nonlinearity, max tempcos: offset – 20μV/°C; gain – 25ppm/°C	–	12-7
10kHz	456	0.02% max nonlinearity, max tempcos: offset – 100μV/°C; gain – 80ppm/°C	–	12-7
20kHz	454	0.005% max nonlinearity, max tempcos: offset – 20μV/°C; gain – 25ppm/°C	–	12-7
100kHz	AD537	0.07% max nonlinearity, low power, max tempcos: offset – 1μV/°C (K); gain – 50ppm/°C (K)	12-7	–
100kHz	458	0.01% nonlinearity, max tempcos: offset – 30μV/°C; gain – 5ppm/°C	–	12-17
500kHz	ADVFC32	±0.01% of max nonlinearity, max tempcos: offset – 30μV/°C; gain – 100ppm/°C	12-17	–
1MHz	460	0.015% nonlinearity, max tempcos: offset – 30μV/°C; gain – 15ppm/°C	–	12-17
1MHz	AD650	±0.01% max nonlinearity, max tempcos: offset – 10μV/°C; gain – 100ppm/°C	12-15	–

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FREQUENCY-TO-VOLTAGE CONVERTERS

Max F.S. Frequency	Model	Brief Description	Vol I Page	Vol II Page
100Hz–20kHz Adjustable	451	0.008% max nonlinearity, 30ms to full scale, max gain tempco – 50ppm/°C	12-21	12-11
1kHz–200kHz Adjustable	453	0.008% max nonlinearity, 4ms to full scale, max gain tempco – 50ppm/°C	12-21	12-11

Orientation

Voltage-to-Frequency & Frequency-to-Voltage Converters

VOLTAGE-TO-FREQUENCY CONVERTERS

Voltage-to-frequency converters (VFC's) convert analog voltage or current levels to pulse trains or square waves in a logic-compatible form (usually TTL) at frequencies that are accurately proportional to the analog quantity. The output continuously tracks the input signal, responding directly to changes in the input signal; external-clock synchronization is not required. V/f converters find applications in analog-to-digital converters with high resolution, long-term high-precision integrators, two-wire high-noise-immunity digital transmission, and digital voltmeters.

FREQUENCY-TO-VOLTAGE CONVERTERS

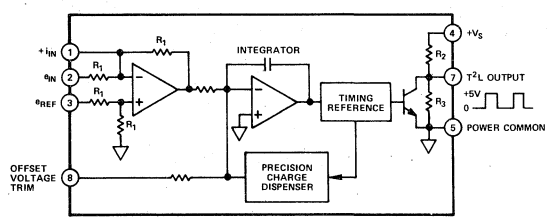
Frequency-to-voltage converters (FVC's) perform the inverse operation; they accept a wide variety of periodic waveforms and produce an analog output proportional to frequency. Combining adjustable threshold, gain, and output offset with low linearity-error, F/V converters offer economical solutions to a wide variety of applications where it is required to convert frequency to an analog voltage. Examples are motor-speed controllers, power-line frequency monitors, and VCO stabilization circuits. In analog-to-analog data transmission, they convert serially transmitted data in the form of pulse streams back to analog voltage.

Applications of both forms of conversion, as appropriate to specific device types, are illustrated with varying degrees of detail on the individual data sheets.

FACTORS IN CHOOSING VFC's AND FVC's

Voltage-to-frequency converters are available from Analog Devices in both module- and monolithic-IC- form. The output of modular types, ranging from 10kHz to 1MHz F.S., is a train of pulses of constant height and width, with very low duty cycle for small analog inputs. The technical data in this volume embrace exceptionally high performance (low-drift and high-resolution) V/F converters, in the form of encapsulated modules. As the Selection Guide indicates, there is also technical data, to be found in Volume I, on a range of monolithic V/F converters, including ADI's unique AD537, which has symmetrical square-wave output, and both voltage and temperature references—and including devices screened to the requirements of MIL-STD-883B and chips for hybrid assembly. Apart from performance specifications, the tradeoffs between module and IC are as follows: modular VFCs have the advantages of completely specified performance; they do not rely on the specifications of critical external components, because the complete self-contained functional package requires no external components; trims are optional. IC's, on the other hand, have the advantages of lower cost and smaller size, and—in the case of the AD537—versatility of output and input connections, lower offset drift, flexibility of frequency range, low power, single-supply operation, low external-component count, plus built-in voltage—and temperature—references. Modules offer better linearity, lower gain drift, and higher full-scale frequencies.

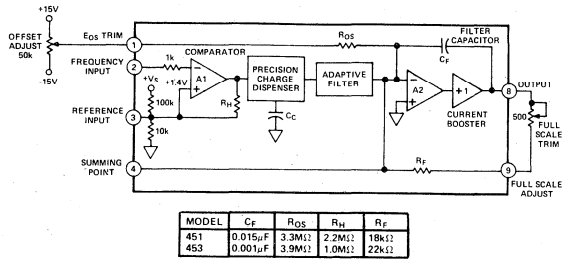
The most-popular VFC designs (Figure 1) contain an integrator, which charges at a rate proportional to the value of the input signal. Each time the integrator's charge has been increased by a precisely metered increment, the threshold crossing produces a pulse of accurately known area. The pulse serves both as the output (via a buffer) and as a subtractive charge



MODEL	FULL SCALE OUTPUT	R_1	R_2	R_3
458	100kHz	20kΩ	10kΩ	4.7kΩ
460	1MHz	10kΩ	2kΩ	910Ω

Figure 1. Block Diagram — Models 458, 460 VFC's

increment to reduce the integrator's net charge. The next pulse is triggered when the net integral has again reached the threshold. The relationship between the pulse rate and the input level is linear.



MODEL	C_F	R_{OS}	R_H	R_F
451	0.015μF	3.3MΩ	2.2MΩ	18kΩ
453	0.001μF	3.9MΩ	1.0MΩ	22kΩ

Figure 2. Block Diagram — Models 451 & 453 FVCs

Frequency-to-voltage-converter modules (Figure 2) average a train of equal-area pulses that are generated internally by a precision charge dispenser, in response to each crossing of an input threshold. The analog output voltage is proportional to the sum of the pulse areas over a given period.

SPECIFICATIONS

The salient specifications for VFC's are *(non)linearity*, as a percentage of full-scale frequency; *frequency range*, the greater the frequency range, the greater the resolution for a given counting period; *full-scale-calibration error*; *gain-temperature coefficient*, in ppm of signal per °C, where "gain" is the ratio of full-scale frequency to full-scale voltage, *input-offset temperature coefficient*; *overrange capability*, within rated specifications, and *step response*, the worst-case time interval required for the frequency to respond to a full-scale-step input change.

For FVC's, important specs, in addition to accuracy specs corresponding to the above, include *output ripple* (for specified input frequencies), *threshold* (for recognition that another cycle has been initiated, and for versatility in interfacing various types of sensors directly), *hysteresis*, to provide a degree of insensitivity to noise superimposed on a slowly-varying input waveform, and *dynamic response* (important in motor control).

Definitions of some critical specifications, and the conditions for adjusting or measuring them, are detailed on individual data sheets.

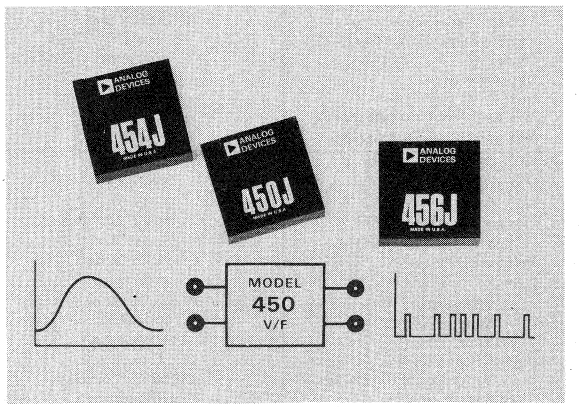
ANALOG DEVICES

Low-Cost, High Performance, 10/20kHz Voltage to Frequency Converters

MODELS 450, 454, 456

FEATURES
- Low Cost
- Low Nonlinearity: ±50ppm max; Model 450K, 454K
- High Stability: ±25ppm/°C max; Model 450K, 454K
- Versatility: Voltage or Current Inputs; Model 454J/K
  - 10V or 20V Full Scale Inputs
  - Bipolar Inputs; Model 454J/K
- Wide Dynamic Range: >86dB; Model 454J/K
- Meet MIL-STD-202E Environmental Testing
- TTL/DTL Compatible Output

APPLICATIONS
- Long Term Precision Integrator
- Ratiometric Measurements
- High CMV Analog Isolator
- A/D Converter with 13-Bit Accuracy
- 2 Wire High Noise Immunity Digital Transmission



GENERAL DESCRIPTION

Models 450, 454 and 456 comprise a new family of modular voltage to frequency converters that provide exceptional linearity and temperature stability over a wide input signal dynamic range. Available in two convenient full scale frequency ranges of 10kHz or 20kHz, these new low cost models can be easily applied to perform ±0.01% analog measurements while directly interfacing with digital circuits.

WHERE TO USE MODELS 450, 454 AND 456

Pin compatible with existing popular models, these new designs offer economical solutions to a range of demanding applications; in Chemical Analysis and Gas Chromatography – as long-term precision integrators; in Process Control and Remote Data Acquisition Systems – two wire data transmission over long distances; in 3½ digit DVM's – as low-cost A/D converters featuring monotonic 13-bit performance and no missing codes; in Blood Analysis – accurate ratiometric measurements over wide dynamic range; in Medical Instruments – isolation using single low cost optical isolator; in Test Instrumentation – as low cost programmable square wave generators.

MODEL SELECTION GUIDE

These compact modules are available in six versions with performance features aimed at meeting key application requirements:

Economy, 10kHz: Model 456 offers the lowest cost for applications requiring 0.1% (10-bit) accuracy. Available in two selection grades, model 456J has 0.03% max nonlinearity with 120ppm/°C max gain drift; model 456K offers 0.02% max nonlinearity and 80ppm/°C gain drift.

High Performance, 10kHz: For all general purpose applications, model 450 should be considered. Nonlinearity is 0.01% max (450J) and 0.005% max (450K) with full scale gain drift guaranteed at 50ppm/°C max (450J) and 25ppm/°C max (450K). Model 450K can achieve 0.005% (14-bit) accuracy over the 1mV to +15V signal range.

Versatility: Model 454 accepts 0 to +20V or 0 to 0.67mA inputs and can be operated with bipolar signals up to ±10V. Nonlinearity is 0.01% max (454J) and 0.005% max (454K); gain drift is 50ppm/°C max (454J) and 25ppm/°C max (454K).

DESIGN APPROACH – PRECISION CHARGE BALANCE

All models incorporate a superior charge balance technique that results in high linearity and temperature stability. Linearity is maintained for inputs below 1mV and operation is free of latch-up.

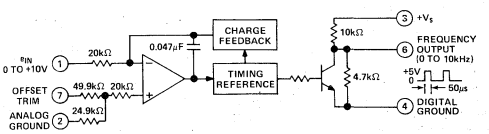


Figure 1. Block Diagram – Models 450 and 456

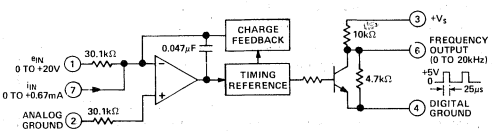


Figure 2. Block Diagram – Model 454

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For detailed information, contact factory.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise noted)

MODEL	ECONOMY 10kHz 456 J | K	HIGH PERFORMANCE 10kHz 450 J | K	VERSATILE 20kHz 454 J | K
TRANSFER FUNCTION			
Voltage Input	$f_{OUT} = (10^3 \frac{Hz}{V}) e_{IN}$	$f_{OUT} = (10^3 \frac{Hz}{V}) e_{IN}$	$f_{OUT} = (10^3 \frac{Hz}{V}) e_{IN}$
Current Input	–	–	$f_{OUT} = (3 \times 10^4 \frac{Hz}{mA}) i_{IN}$
ANALOG INPUT			
Voltage Signal Range (e_{IN})	0 to +10V max	0 to +10V max	0 to +20V max
Current Signal Range (i_{IN})	–	–	0 to 0.67mA min
Overrange	50% min	50% min	10% min
Impedance (e_{IN})	20kΩ	20kΩ	30kΩ
Impedance (i_{IN})	–	–	0Ω
Max Safe Input Voltage (e_{IN})	+25V, $-V_S$	+25V, $-V_S$	+25V, $-V_S$
Max Safe Input Current (i_{IN})	–	–	+1mA
ACCURACY			
Warm-Up Time	1 minute	1 minute	1 minute
Nonlinearity			
e_{IN} = +1mV to +15V	±0.03% max | ±0.02% max	±0.01% max | ±0.005% max	–
e_{IN} = +1mV to +22V	–	–	±0.01% max ±0.005% max
Full Scale Error[1]	(+½, +1½)% max	(+½, +1½)% max	(+½, +1½)% max
Gain			
vs. Temperature (0 to +70°C)	±120ppm/°C max | ±80ppm/°C max	±50ppm/°C max | ±25ppm/°C max	±50ppm/°C max | ±25ppm/°C max
vs. Supply Voltage	±400ppm/%	±200ppm/% max	±200ppm/% max
vs. Time	±150ppm/day	±100ppm/day	±100ppm/day
Input Offset Voltage[1]	±10mV	±5mV max	±5mV max
vs. Temperature (0 to +70°C)	±100μV/°C max	±50μV/°C | ±20μV/°C max	±50μV/°C | ±20μV/°C max
vs. Supply Voltage	±10ppm/%	±10ppm/% max	±10ppm/% max
vs. Time	±20μV/day	±10μV/day	±10μV/day
RESPONSE			
Settling Time for +10V Step Input	120μs	120μs	120μs
Overload Recovery Time	15ms	15ms	22ms
OUTPUT[2]			
Waveform	train of TTL/DTL compatible pulses	train of TTL/DTL compatible pulses	train of TTL/DTL compatible pulses
Pulse Width	50μs	50μs	25μs
Rise/Fall Time	200ns/100ns	200ns/100ns	200ns/100ns
Pulse Polarity	positive	positive	positive
Logic "1" (High) Level	+2.4V min	+2.4V min	+2.4V min
Logic "0" (Low) Level	+0.4V max	+0.4V max	+0.4V max
Capacitive Loading	1000pF max	1000pF max	1000pF max
Fan Out Loading	10 TTL loads min	10 TTL loads min	10 TTL loads min
Impedance	3.3kΩ	3.3kΩ	3.3kΩ
POWER SUPPLY[3]			
Voltage, Rated Performance	±15V dc	±15V dc	±15V dc
Voltage, Operating	±(12 to 18)V dc	±(12 to 18)V dc	±(12 to 18)V dc
Current, Quiescent	(+15, -9)mA	(+15, -9)mA	(+15, -9)mA
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	0 to +70°C	0 to +70°C
Operating	-25°C to +80°C	-25°C to +80°C	-25°C to +80°C
Storage	-55°C to +85°C	-55°C to +85°C	-55°C to +85°C
CASE SIZE	1.5" x 1.5" x 0.4"	1.5" x 1.5" x 0.4"	1.5" x 1.5" x 0.4"

[1] Adjustable to zero; refer to Adjustment Procedure.
[2] Protected for continuous short-circuit to ground. CAUTION: DO NOT SHORT OUTPUT TO -15V SUPPLY.
[3] Recommended ADI power supply: model 904, ±15V @ 50mA.
Specifications subject to change without notice.

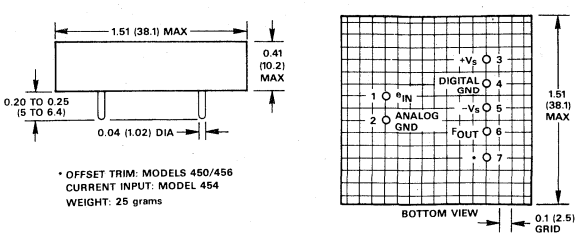
All Units Meet the Requirements of MIL-STD-202E as Outlined Below

TEST	METHOD	CONDITION
High Temperature Storage	108A	D (Non-Operating)
Moisture Resistance	106D	(10 Days)
Solderability	208C	
Thermal Shock	107D	A (5 Cycles)
Terminal Strength	211A	A (Pull Test; 10 lbs)
Temperature Cycling	102A	D (-55°C/+85°C)
Vibration	204C	B (15g Peak)
Barometric Pressure	105C	B (50,000 Feet)

TABLE 1. Environmental Specifications

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



MATING SOCKET AC1047

VOLTAGE TO FREQUENCY OPERATION

Models 450, 454 and 456 provide accurate conversion of analog signals into a train of constant width and constant amplitude pulses at a rate directly proportional to the analog signal amplitude. The output continuously tracks the input signal responding directly to changes in the input signal; external clock synchronization is not required. The output pulse train is TTL/DTL compatible, permitting direct interface to low cost digital processing circuits.

Dynamic Range: Models 450 and 456 accept unipolar, single ended input signals from 0V to +10V with 50% minimum overrange. The corresponding output frequency is dc to 10kHz as shown in Figure 3. Model 454 is designed for either bipolar or unipolar single ended input signals. It accepts 0V to +20V or 0mA to 0.67mA input signals directly with 10% min overrange; the corresponding output frequency is dc to 20kHz.

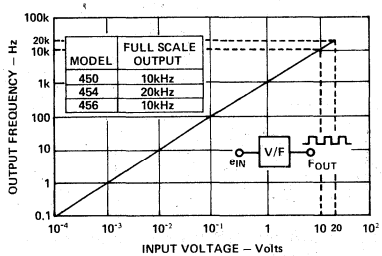


Figure 3. Voltage-to-Frequency Transfer Curve

ADJUSTMENT PROCEDURE

All models may be used directly with no external trim potentiometers required. Overall accuracy and dynamic range may be improved by using two optional trim adjustments as shown in Figures 6 and 7; FULL SCALE and OFFSET adjust. Low temperature coefficient trims must be used to maintain the drift specifications of the V/F model. The T.C. of the trim pot will add to the FULL SCALE DRIFT for each model as follows:

$$\text{FULL SCALE DRIFT CONTRIBUTION} = \left[\frac{R_{ext}}{R_{ext} + 20k\Omega^*}\right] \times \left[\text{T.C. } R_{ext}\right] /^\circ C$$

*30kΩ, model 454

Calibration Procedure: Allow a five minute warm-up after initial power turn on. Using a precision, stable voltage source, set the input voltage, e_{IN}, to +1.00mV. Adjust the OFFSET trim, R_O, for an output pulse interval of 1 second (1Hz). Set the input voltage to +10.000V and adjust the FULL SCALE trim for an output pulse interval of 100μs (10kHz). The V/F may now be used without further adjustment.

PERFORMANCE SPECIFICATIONS

Nonlinearity: Nonlinearity is specified as a % of full scale input: 10V for models 450 and 456; 20V for model 454 – and is guaranteed for each model over the specified input range: 0.005% max, models 450K and 454K; 0.01% max, models 450J and 454J; 0.03% max, model 456J and 0.02% max, model 456K. Typical nonlinearity performance is illustrated for model 450J in Figure 4. Below 1mV input, nonlinearity error remains within the specified limits, but is masked by zero offset stability, input noise and adjustment accuracy.

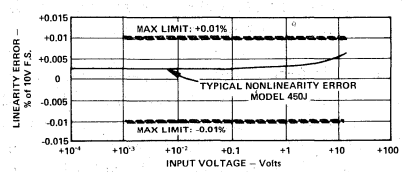


Figure 4. Model 450J: Nonlinearity Error Versus Input Signal

Gain Temperature Stability: Gain drift is specified in ppm of input signal and is guaranteed for each model over the 0 to +70°C temperature range. The curves of Figure 5 illustrate the drift limits for all models; typical performance is half the guaranteed limits.

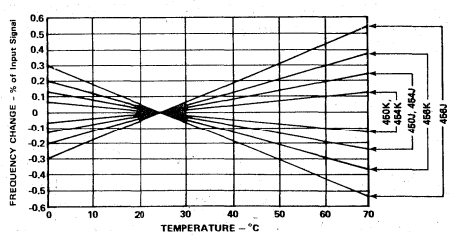


Figure 5. Gain Frequency Drift (Worst Case)

12

V/F INTERCONNECTION

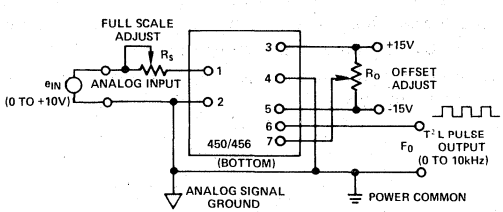


Figure 6. Models 450/456

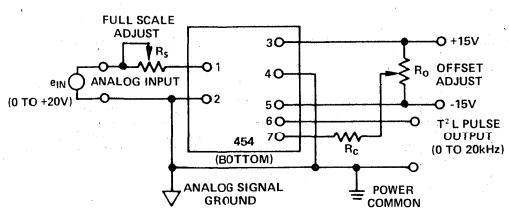


Figure 7. Model 454

EXTERNAL CONNECTIONS FOR VOLTAGE TO FREQUENCY OPERATION, WITH OPTIONAL INPUT OFFSET VOLTAGE AND FULL SCALE OUTPUT FREQUENCY ADJUSTMENTS

R_S = FULL SCALE ADJUSTMENT; 500Ω (Use low T.C. Cermet, <50ppm/°C or equivalent)
R_O = INPUT OFFSET ADJUSTMENT; 50kΩ (Use low T.C. Cermet, <50ppm/°C or equivalent)
R_C = 20MΩ

CAUTION: DO NOT SHORT OUTPUT TO -15V

OUTPUT FREQUENCY SCALING

Lowering Full Scale Frequency: The full scale frequency of a V/F converter can be reduced by three techniques; (1) adding a series trim potentiometer, such as 10kΩ, with the input; (2) adding a voltage divider network at the input; or (3) adding a digital divider at the output. Both input techniques (1) and (2), degrade the full scale gain drift by the added T.C. of the input resistors. By using a frequency divider connected to the V/F output, full scale frequency can be conveniently reduced without degradation of the converter's full scale drift performance. By adding successive frequency dividers, as illustrated in Figure 8, a precision, low-cost, voltage controlled square wave generator can be designed.

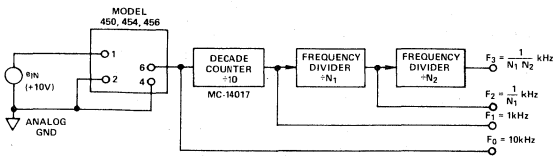
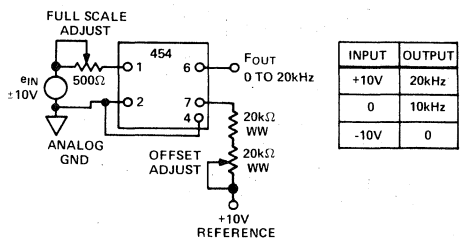


Figure 8. Voltage Controlled Square Wave Generator Using Digital Dividers and V/F Converter

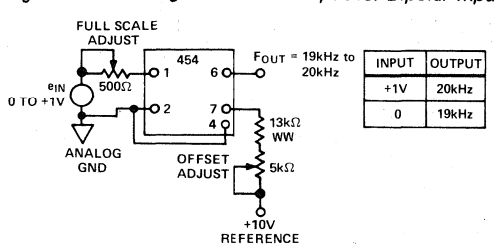
Offsetting Full Scale Frequency; Model 454: The summing input terminal of model 454 (i_{IN} terminal) may be used to conveniently offset the output frequency to permit bipolar input signals up to ±10V, as well as improve the dynamic response to low level input signals. As shown in Figure 9, a current is fed through an external resistor from a voltage reference to the current terminal. A low cost precision +10V voltage reference, such as ADI model AD2700, is recommended to retain the stability and accuracy of model 454.

As illustrated in Figure 10, the output may also be scaled up so that low amplitude signals – (i.e. e_{IN} = 1V – will give full scale output frequency – (e_o = 20kHz). The step response for a 1 volt input change improves to only 50μs, compared to 1ms before offsetting.



INPUT	OUTPUT
+10V	20kHz
0	10kHz
-10V	0

Figure 9. Offsetting Model 454 Output for Bipolar Inputs



INPUT	OUTPUT
+1V	20kHz
0	19kHz

Figure 10. Offsetting Model 454 Output for Improved Dynamic Response

SQUARE WAVE OUTPUT

Using a type D flip-flop connected to the output of the V/F converter offers a simple low cost technique to obtain a voltage controlled, variable frequency, square wave signal; see Figure 11. Using model 454 with current offsetting, a 10kHz full scale square wave output can be achieved with 10V input signal.

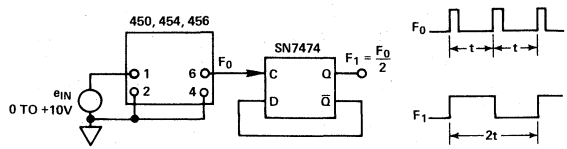


Figure 11. Square Wave Output Using Type D Flip-Flop

CMOS/HNIL COMPATIBLE OUTPUT

The circuit shown in Figure 12 may be used to shift the output of the 450, 454 or 456 from 0 to +5V to 0 to +12V, to provide a 4V noise immunity for driving high noise immunity logic (HNIL) and CMOS logic.

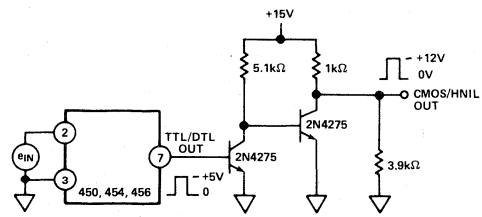


Figure 12. Circuit for Shifting the Output of the 450, 454, 456 to Drive CMOS/HNIL Logic

DYNAMIC RESPONSE

Overload Recovery: All models can safely withstand input overloads up to +25V, $-V_S$. Overload recovery time will depend on input polarity. Worst case overload recovery occurs following a sustained negative overload. Following removal of the overload, the input must be driven positive to restore normal operation. The recovery time depends upon the input voltage applied after removal of the overload and is given by:

$$\text{Model 450/456: } t_r \text{ (ms)} = \frac{15}{E \text{ (Volts)}}$$

$$\text{Model 454: } t_r \text{ (ms)} = \frac{22}{E \text{ (Volts)}}$$

where E is the voltage applied following overload. Recovery from positive overloads up to the max safe input occurs essentially instantaneously after removal of the overload condition.

Step Response: The output settling time for step input changes is a function of the final output frequency. Settling time is specified as 20μs plus 2 output pulses of the new frequency. For a 10V step input, the settling time will be 120μs. Figure 13 shows typical timing relationships between input and output for input voltages of 2V and 10V.

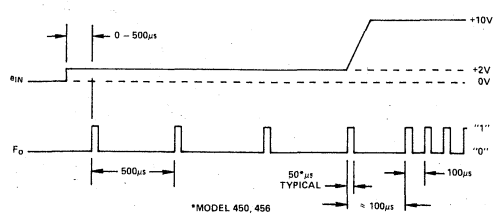


Figure 13. Timing Waveforms; Input/Output

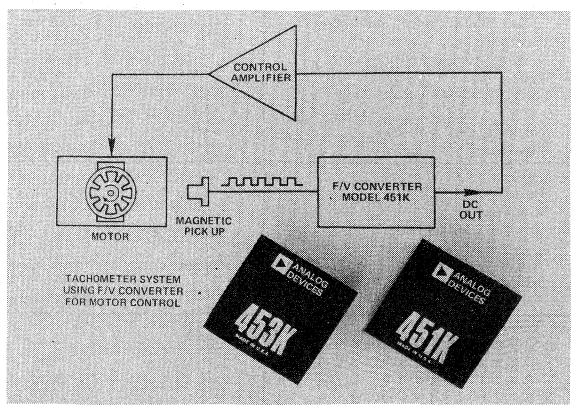
ANALOG DEVICES

Low-Cost, Versatile, 10/100kHz Frequency to Voltage Converters

MODELS 451, 453

FEATURES
- **Low Cost**
- **Versatility: Adjustable Threshold, Gain & Output Offset**
- **Guaranteed Low Nonlinearity: 80ppm Max, 451L and 453L**
- **Accepts TTL, CMOS, HNIL, Sinewave, Pulse, Squarewave and Triangle Wave Input Signals**
- **No External Components to Meet Rated Performance**
- **+20mA Output to Operate Relays and Meters**
- **Low Profile Package, 0.4" Case Height**
- **Meet MIL-STD-202E Environmental Testing**

APPLICATIONS
- **Motor Control and Speed Monitor**
- **Line Frequency Monitor and Alarm Indicator**
- **Fluid Flow Measurements and Control**
- **FM Demodulation and VCO Stabilization**
- **Frequency vs. Amplitude Response Measurements**



GENERAL DESCRIPTION

Models 451 and 453 are low cost 10kHz and 100kHz frequency to voltage converters that feature excellent low nonlinearity to less than 80ppm, output current of +20mA and the capability of interfacing with TTL, HNIL, CMOS, sinewave, squarewave, pulse and triangular input signals. External components are not required to achieve rated performance, however, extreme versatility is maintained by allowing access to all critical points of the design. This versatility allows programmable input threshold, gain, and output offset voltage.

Both models 451 and 453 are available in three selections, each offering guaranteed maximum nonlinearity error as well as maximum gain drift error. Models 451J and 453J offer 0.03% max nonlinearity and 100ppm/°C max gain drift. Models 451K and 453K offer 0.015% max nonlinearity and 50ppm/°C max gain drift. Models 451L and 453L offer 0.008% max nonlinearity and 50ppm/°C max gain drift.

WHERE TO USE FREQUENCY TO VOLTAGE CONVERTERS

Pin compatible with existing popular models, these versatile new designs offer economical solutions to a wide variety of applications where it is required to convert frequency to an analog voltage.

Process Control Systems: For motor speed controllers, power line frequency monitoring and fluid flow measurements where flow transducers, such as variable reluctance magnetic pickups, provide pulse train outputs as a linear function of flow rate.

Audio and Accoustic Systems: For wow and flutter measurements with tape recorders and turntables, FM demodulation and speaker response measurements.

Test Instrumentation: For VCO stabilization, analog readout frequency meter, vibrational analysis and frequency versus amplitude X-Y plots where the vertical axis presents the normal amplitude signal and the horizontal axis presents the output signal from the F/V converter.

Data Acquisition Systems: For converting serially transmitted data back to analog voltages.

DESIGN FEATURES AND USER BENEFITS

The combination of low cost and high performance provided by models 451 and 453 offers exceptional quality and value to the OEM designer. These compact modules have been designed to provide maximum versatility, thereby increasing their utility in a broad scope of applications.

Adjustable Input Threshold: Threshold level is externally resistor programmable from 0 to ±12V, permitting simple, direct interface with low level signals, e.g. 10mV p-p, as well as with high level inputs such as CMOS and HNIL logic levels, e.g. 0 to +12V.

Adjustable Gain: Model 451 can be adjusted to provide full scale output voltage for any input frequency from 1kHz to 20kHz. Model 453 can be adjusted to provide full scale output voltage for any input frequency from 1kHz to 200kHz. This adjustable gain feature enables the user to easily match the maximum frequency output from a wide class of frequency transducers to the +10V full scale output from models 451 and 453. Increased signal conversion sensitivity with higher resolution results.

Adjustable Output Offset Voltage: The output offset is adjustable from -10V to +10V, enabling bipolar outputs or expanded scale measurements or setting the input frequency where zero output voltage occurs.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise noted)

MODEL	10kHz FULL SCALE 451 J	10kHz FULL SCALE 451 K	10kHz FULL SCALE 451 L	100kHz FULL SCALE 453 J	100kHz FULL SCALE 453 K	100kHz FULL SCALE 453 L
TRANSFER FUNCTION	$E_O = (10^{-3}$ V/Hz)(F_{IN})			$E_O = (10^{-4}$ V/Hz)(F_{IN})		
FREQUENCY INPUT						
Frequency Range	dc to 10kHz min			dc to 100kHz min		
Overrange	10% min			10% min		
Waveforms	Sine, Square, Triangle, Pulse Train			Sine, Square, Triangle, Pulse Train		
Pulse Width (Pulse Train Input)	20μs min			2μs min		
Threshold	+1.4V			+1.4V		
With External Adjustment	0V to ±12V			0V to ±12V		
Hysteresis	±50mV			±100mV		
Levels (TTL Compatible) High	+1.45V to +12V			+1.5V to +12V		
Low	-12V to +1.35V			-12V to +1.3V		
Max Safe Input Voltage[1]	$\pm V_S$			$\pm V_S$		
Impedance	10MΩ‖10pF			10MΩ‖10pF		
ACCURACY						
Warm-Up Time	one minute			one minute		
Nonlinearity[2]						
F_{IN} = 1Hz to 11kHz	±0.03% max	±0.015% max	±0.008% max	–	–	–
F_{IN} = 1Hz to 110kHz	–	–	–	±0.03% max	±0.015% max	±0.008% max
Gain vs. Temperature[3] (0 to +70°C)	±100ppm/°C max	±50ppm/°C max	±50ppm/°C max	±100ppm/°C max	±50ppm/°C max	±50ppm/°C max
vs. Supply Voltage	±300ppm/%			±350ppm/%		
vs. Time	±30ppm/month			±30ppm/month		
RESPONSE						
Step Response to ±0.5% of Final Value						
F_{IN} = dc to Full Scale	4ms			0.8ms		
F_{IN} = Full Scale to dc	30ms			4ms		
Internal Filter Time Constant	200μs			24μs		
External Filter Time Constant	20ms/μF			20ms/μF		
OUTPUT[4]						
Voltage (F_{IN} = Full Scale)[5]	+9.85V min; +9.95V max			+9.85V min; +9.95V max		
Current (E_O = +10V, -10V)	(+20, -2)mA min			(+20, -2)mA min		
Offset Voltage[6] @ +25°C	±7.5mV max			±7.5mV max		
vs. Temperature (0 to +70°C)	±30μV/°C max			±30μV/°C max		
vs. Supply Voltage	±100μV/% max			±50μV/% max		
vs. Time	±100μV/month			±100μV/month		
Ripple						
F_{IN} = 1Hz	3mV p-p			55mV p-p		
F_{IN} = 10kHz	80mV rms			35mV rms		
F_{IN} = 100kHz	–			35mV rms		
Impedance	0.1Ω			0.1Ω		
Offset Scale Factor[7]	-56μA/V			-45μA/V		
POWER SUPPLY[8]						
Voltage, Rated Performance	±15V dc			±15V dc		
Voltage, Operating	±(12 to 18)V dc			±(12 to 18)V dc		
Current, Quiescent	(+10, -8)mA			(+10, -8)mA		
TEMPERATURE RANGE						
Rated Performance	0 to +70°C			0 to +70°C		
Operating	-25°C to +85°C			-25°C to +85°C		
Storage	-55°C to +85°C			-55°C to +125°C		
MECHANICAL						
Case Size	1.5" x 1.5" x 0.4"			1.5" x 1.5" x 0.4"		
Weight	25 grams			25 grams		

[1] F_{IN} and REF terminals can be shorted to $\pm V_S$ indefinitely without damage.
[2] Nonlinearity error is specified as a percentage of 10V full scale output level.
[3] Gain temperature drift is specified in ppm of output signal level.
[4] OUT terminal can be shorted indefinitely to $\pm V_S$ and ground without damage.
[5] Adjustable to +10.000V using FULL SCALE ADJUST trim pot.
[6] Adjustable to zero using 50kΩ OFFSET ADJUST trim pot.
[7] Current into the SUM PT terminal to offset the output voltage positive.
[8] Recommended power supply, ADI model 904, ±15V @ 50mA output.

Specifications subject to change without notice.

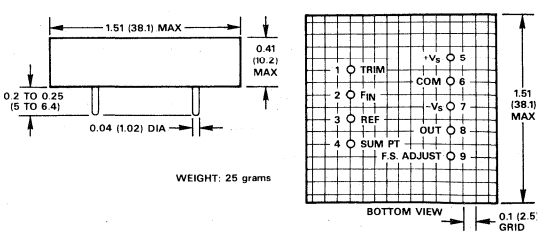
All Units Meet the Requirements of MIL-STD-202E as Outlined Below

TEST	METHOD	CONDITION
High Temperature Storage	108A	D (Non-Operating)
Moisture Resistance	106D	(10 Days)
Solderability	208C	
Thermal Shock	107D	A (5 Cycles)
Terminal Strength	211A	A (Pull Test; 10 lbs)
Temperature Cycling	102A	D (-55°C/+85°C)
Vibration	204C	B (15g Peak)
Barometric Pressure	105C	B (50,000 Feet)

TABLE 1. Environmental Specifications

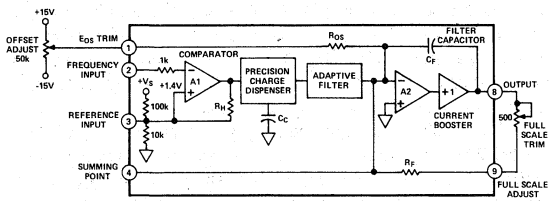
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)



FREQUENCY TO VOLTAGE OPERATION

Models 451 and 453 accept virtually any signal waveshape providing accurate conversion into an output voltage proportional to the input signal frequency. The only restriction is that the input signal must remain above the threshold level for 20μs when using model 451, and 2μs when using model 453. Linear, stable conversion over four decades of input range for model 451 and five decades of input range for model 453, is achieved using a precision charge-dispensing design approach. Figure 1 represents a functional block diagram for both models 451 and 453 frequency to voltage converters.



MODEL	CF	ROS	RH	RF
451	0.015μF	3.3MΩ	2.2MΩ	18kΩ
453	0.001μF	3.9MΩ	1.0MΩ	22kΩ

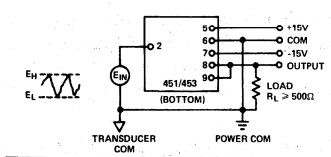
Figure 1. Block Diagram — Models 451 & 453 F/V Converters

THEORY OF OPERATION

Input signals are applied directly to a comparator, A1, which is internally set to provide a +1.4V threshold with ±50mV hysteresis for model 451 and ±100mV hysteresis for model 453. This threshold level offers excellent noise immunity for TTL input levels. Following the input comparator is a precision charge dispensing circuit and output amplifier where the comparator signal is converted to a dc voltage. When the input comparator changes state, C_C is alternately charged from a precision voltage reference and discharged through the summing point of an output amplifier, A2. A fixed amount of charge, Q, is controlled during each charge/discharge cycle. The higher the input frequency, the higher the average current into the summing point of A2. A current to voltage conversion is then accomplished by R_F. The current pulses from the charge dispensing circuit are integrated by C_F to reduce ripple. Added filtering for low frequency input signals is provided by an adaptive filter at the output of the charge dispensing circuit.

BASIC F/V HOOK-UP

Models 451 and 453 can be applied directly to achieve rated performance without external trim potentiometers or other components. Figure 2 illustrates the basic wiring connection for either F/V converter model. Using the basic hookup as shown, full scale output voltage accuracy is +10V, -½% to -1½%. The output offset voltage is 0V to ±7.5mV. The Full Scale and Output Offset errors can be eliminated by using the FINE TRIM PROCEDURE.



MODEL	INPUT VOLTAGE RANGE		INPUT FREQUENCY RANGE
	High (E_H)	Low (E_L)	(F_{IN})
451	+1.45V to +12V	-12V to +1.35V	0 to 11kHz
453	+1.5V to +12V	-12V to +1.3V	0 to 110kHz

Figure 2. Basic Wiring Interconnection

FINE TRIM PROCEDURE

Connect the F/V converter as shown in Figure 3 and allow a five minute warm-up after initial power turn-on. Adjust the OFFSET ADJUST pot, R_O, for an output of 0.000V. The input terminal, F_{IN}, can be left open or tied to COM without affecting OFFSET ADJUST. Using a precision, stable frequency source connected to F_{IN} terminal, set the input frequency to 10.000kHz for model 451 or 100.000kHz for model 453. Adjust the FULL SCALE ADJUST trim pot, R_S, for an output of +10.000V.

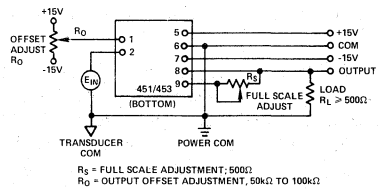


Figure 3. Wiring Interconnection Showing Fine Adjustment Trims for Offset and Full Scale Frequency

ADDITIONAL TRIM CAPABILITY

Adjusting Input Threshold: The input comparator of models 451 and 453 shown in Figure 1, conditions the input signals providing protection against noisy environments as well as preventing double triggering with slow rise-time signals. Input levels up to the supply voltages, $\pm V_S$, will not cause damage to the input comparator.

Threshold voltage level, V_T, is internally set for both models 451 and 453 at +1.4V. Hysteresis, V_H, for model 451 is ±50mV, and ±100mV for model 453. Signals of virtually any waveshape which exceed the combined threshold and hysteresis levels, $V_T \pm V_H$, will trigger the F/V converter. The REF terminal permits the user to conveniently adjust the input threshold over the range from 0 to ±12V to achieve optimum noise rejection or increased triggering sensitivity.

Increasing Threshold for Greater Noise Immunity: Connecting an external resistor from the REF terminal to the positive supply voltage, $+V_S$, increases the input threshold level above +1.4V, offering increased input noise immunity. Optimum noise immunity is generally determined by adjusting the threshold level to a point mid-way between the high and low input signal levels. For example, for a 0 to +12V input swing — representative of CMOS and HNIL logic signals — a 17.6kΩ resistor from +15V to the REF terminal results in a +6V threshold.

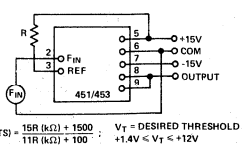


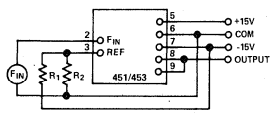
Figure 4. Increasing Threshold Above +1.4V for Greater Noise Immunity

Changes in impedance at the REF terminal result in changes to the hysteresis. Hysteresis levels can be calculated by assuming the comparator output is switching between ±12V. This ±12V signal is attenuated by a resistor-divider network formed by

R_H (see Figure 1) and the parallel combination of all resistors attached at the comparator positive input. For example, with a 17.6kΩ resistor connected to the REF terminal, hysteresis becomes ±35mV for model 451 and ±75mV for model 453. The F/V converter will, therefore, trigger at +6V ±35mV for model 451 and +6V ±75mV for model 453.

Decreasing Threshold for Signals Less Than +1.4V: A resistor connected from the REF terminal to the negative power supply, $-V_S$, will increase the input triggering sensitivity for operation with signals below $+1.4V_{PK}$. As shown in Figure 5, a minimum threshold of zero volts is obtained with a 100kΩ resistor. The triggering level, $V_T \pm V_H$, will be established by the resulting hysteresis levels. With a 100kΩ to -15V, model 451 hysteresis will be ±50mV and model 453 hysteresis will be ±60mV.

To reduce the hysteresis for greater triggering sensitivity, a 1kΩ resistor can be connected from the REF terminal to COM. Signals exceeding ±5mV (10mV p-p) with model 451 and ±15mV (30mV p-p) for model 453, will operate the F/V converter. A 1kΩ resistor from REF to COM is the minimum value recommended to reduce hysteresis and achieve reliable operation.



MODEL	R_1	R_2	THRESHOLD (V_T)	HYSTERESIS (V_H)	TRIGGER LEVELS ($V_T \pm V_H$)
451	∞	∞	+1.4V	±50mV	+1.45V; +1.35V
	100kΩ	∞	0V	±20mV	±20mV (40mV p-p)
	100kΩ	1kΩ	0V	±5mV	±5mV (10mV p-p)
453	∞	∞	+1.4V	±100mV	+1.5V; +1.3V
	100kΩ	∞	0V	±60mV	±60mV (120mV p-p)
	100kΩ	1kΩ	0V	±15mV	±15mV (30mV p-p)

Figure 5. Decreasing Threshold Below +1.4V to Increase Triggering Sensitivity for Low Level Input Signals

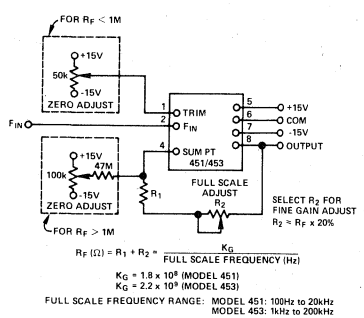


Figure 6. Selecting External Gain Resistor R_F

Adjusting Gain: Connect the FULL SCALE ADJUST terminal to the OUTPUT terminal to set the gain of model 451 at 10^{-3}V/Hz for a 10kHz full scale input frequency and the gain of model 453 at 10^{-4}V/Hz for a 100kHz full scale input frequency. Connecting an external resistor from the SUM PT terminal to the OUTPUT terminal and leaving the FULL SCALE ADJUST terminal open, facilitates gain adjustment. Model 451 can be adjusted over the range from 10^{-1}V/Hz to 5 x 10^{-4}V/Hz resulting in a full scale input frequency from 100Hz to 20kHz respectively. The gain of model 453 can be adjusted over the range from 10^{-2}V/Hz to 5 x 10^{-5}V/Hz resulting in a full scale input frequency from 1kHz to 200kHz respectively. The gain adjustment procedure is capable of increasing full scale frequency beyond the rated ranges for each model, however, nonlinearity will increase above 300ppm.

When using large values of R_F to externally set gain of the F/V converter, the output amplifier gain increases resulting in an increase in sensitivity when using the OFFSET ADJUST trim pot. For improved resolution in high gain applications ($R_F >$ 1MΩ), an alternate method of trimming offset is shown in Figure 6.

Offsetting the Output: The output of models 451 and 453 can be offset over the range from -10V to +10V, enabling scale expansion for increased signal sensitivity as well as bipolar output swings up to 20V p-p.

Current introduced at the SUM PT terminal results in shifts of the output voltage directly proportional to the Offset Scale Factor, K_S. For model 451, K_S = -56μA/V and for model 453, K_S = -45μA/V. The offset current can be generated using an external resistor from a voltage reference to the SUM PT terminal. A stable, well regulated supply voltage, such as ADI's model 904 is recommended. To shift the output positive, 0 to +10V, connect the current resistor to the negative, $-V_S$ supply. To shift the output negative, 0 to -10V, connect the current resistor to the positive, $+V_S$, supply.

The example using model 451 illustrated in Figure 7 provides a 0 to +5V output change in response to a 5kHz to 10kHz input change. With this input, a bipolar output from -2.5V to +2.5V can be obtained by increasing the output voltage shift from -5V, (R_C = 53.6kΩ) to -7.5V, (R_C = 35.7kΩ).

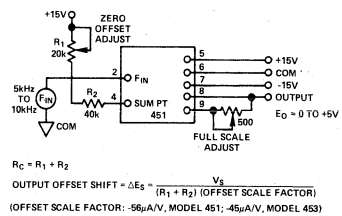


Figure 7. Selecting External Output Offset Resistor, R_C

SCALE EXPANSION

By combining both gain and output offset voltage adjustments, signals which exhibit a center frequency with small frequency changes, can be converted with improved resolution. Representative signals benefiting from the Scale Expansion procedure outlined below, are tachometer and frequency modulated signals. In the case of tachometer outputs, the speed is often set at an idle point and changes in output frequency represent changes in motor loading conditions. In the case of FM signals, the F/V converter can be applied such that the carrier frequency produces zero output. The resulting output voltage from the F/V converter represents the modulating signal.

Procedure for Scale Expansion: The following procedure incorporates both gain and output offset adjustments to achieve scale expansion. An example is illustrated in Figure 8 for an FM signal with a 50kHz carrier frequency and ±5kHz modulating signal.

1) Determine the Gain: $G = \Delta E_O/\Delta F_{IN}$ where ΔE_O is the total output voltage change desired in volts, and ΔF_{IN} is the total input frequency change in Hz.

2) Calculate the external gain resistor, R_F;
$R_F(\Omega) = G(1.8 \times 10^7)$, model 451
$R_F(\Omega) = G(2.2 \times 10^8)$, model 453

3) Calculate the Output Offset Shift, ΔE_S, required to achieve the desired maximum output voltage, E_O (max) with the max input frequency, F_{IN} (max), and the new gain;

$$\Delta E_S \text{ (volts)} = G\, F_{IN} \text{ (max)} - E_O \text{ (max)}$$

4) Calculate the offset current resistor, R_C;

$$R_C\,(\Omega) = \frac{V_S\, G}{(\Delta E_S)\,(k_s)}$$

$k_s = 56 \times 10^{-9}$, model 451
$k_s = 45 \times 10^{-10}$, model 453

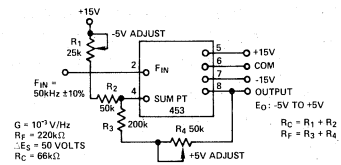


Figure 8. Application of Model 453 in FM Demodulation

INTERFACING SIGNALS WITH DC OFFSETS > 10V

Signals with dc levels up to ±10V can be directly connected to the input terminal of models 451 and 453. Capacitive coupling, as shown in Figures 9 and 10, is used for inputs with dc offsets greater than ±10V. The 1MΩ resistor illustrated in Figure 9 provides a dc return path to power common for the input comparator bias current. Threshold adjustments can be made following the capacitor, to set the F/V input sensitivity to match the ac signal peak-to-peak amplitude. Signals as low as 10mV p-p with model 451 and 30mV p-p model 453 are acceptable. Refer to Figures 4 and 5.

AC signals greater than $\pm V_S$ should be attenuated with a resistive divider network following the capacitor. When large input transients ($>\pm V_S$) are possible due to either a noisy environment or power turn-on surges, protection is provided with the addition of two diodes as shown in Figure 10.

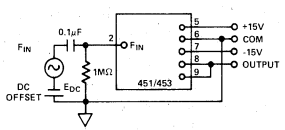


Figure 9. Interfacing Signals With DC Offsets Greater Than ±10V

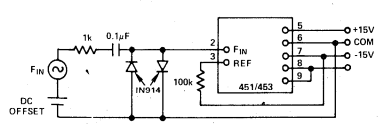


Figure 10. Input Diode Protection for High Voltage Transients

PERFORMANCE SPECIFICATIONS

Nonlinearity: Nonlinearity error is specified as a % of 10V full scale output voltage and is guaranteed for each model over the specified input range. Model 451 is rated over 1Hz to 11kHz range and model 453 is rated over 1Hz to 110kHz range. Typical nonlinearity performance is shown for all models in Figure 11.

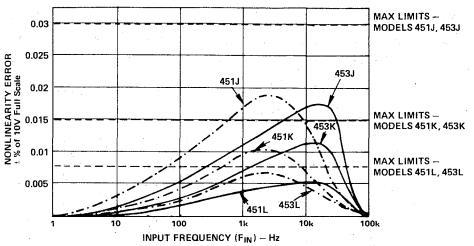


Figure 11. Nonlinearity Error Versus Input Frequency

Gain Temperature Stability: Gain Drift is specified in ppm of output signal and is guaranteed for each model over the 0 to +70°C temperature range. Models 451K, 451L, 453K and 453L offer ±50ppm/°C maximum gain drift. Models 451J and 453J offer ±100ppm/°C maximum gain drift. Gain drift is typically half the guaranteed limits.

OUTPUT RIPPLE

The output contains an ac ripple signal which increases in amplitude with input frequency. Adding external capacitance in parallel with the internal filter capacitor will reduce output ripple as shown in Figures 12 and 13.

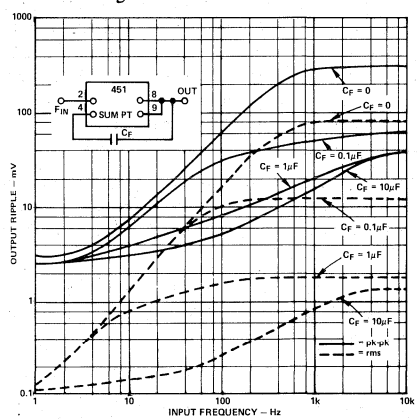


Figure 12. Output Ripple Versus External Filter Capacitor (C_F) – Model 451

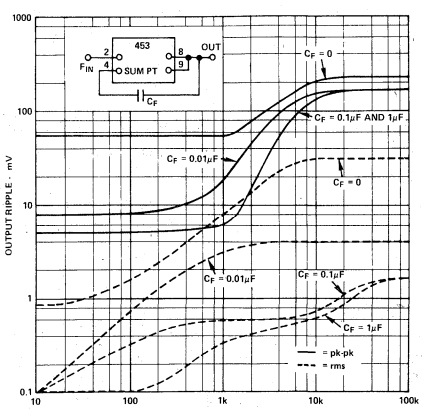


Figure 13. Output Ripple Versus External Filter Capacitor (C_F) – Model 453

12

SETTLING TIME

Increasing the external filter capacitor to reduce output ripple will increase the settling time to step changes in frequency occurring at the input. Figure 14 shows curves of settling time to ±0.5% of final value for both increasing and decreasing full scale step changes. As C_F increases in value, the total filter time constants for models 451 and 453 approach equal values, resulting in identical settling time.

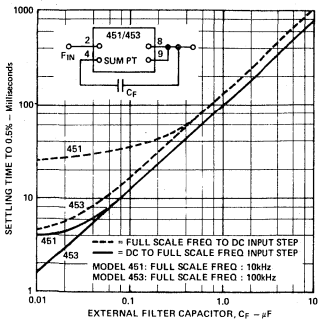


Figure 14. Settling Time Versus External Filter Capacitor

APPLICATIONS IN PROCESS CONTROL SYSTEMS

MOTOR CONTROLLER

In making rpm measurements, transducers are often encountered that have pulse-train outputs from variable-reluctance magnetic pickups (in which the output frequency is a function of rpm). These low level signals are generally in the range of 0 to 200mV peak. The adjustable input threshold feature of models 451 and 453 enables direct connection to low level transducers, offering simple, reliable interfacing.

The motor speed control and monitoring application shown in Figure 15 illustrates the F/V converter applied in a closed loop control system. R1 sets the threshold to +60mV with ±50mV hysteresis for model 451.

The +20mA output current capability of both models 451 and 453, enables direct interface to low impedance loads, up to 500Ω, such as analog meters or relays.

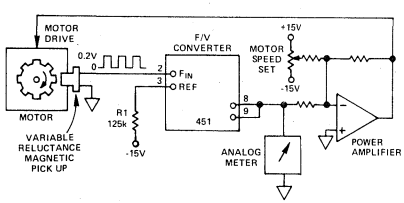


Figure 15. Application of F/V Converter to Control and Monitor Motor Speed in Closed Loop System

SPEED SWITCH

With the addition of a low cost comparator and relay, the F/V converter provides a reliable approach to controlling heavy generator loads after the generator has reached a specified speed. As shown in Figure 16, the relay will remain open until the output from the F/V converter reaches a preset POWER ON trip level. The F/V output signal is linearly related to the speed of the motor, permitting precise control of the POWER ON set point.

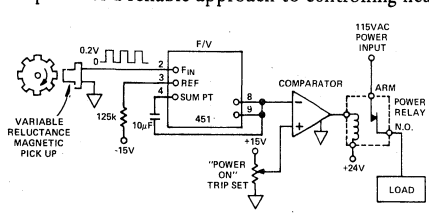


Figure 16. Application of F/V Converter to Control Load Power

APPLICATION IN INSTRUMENTATION SYSTEMS

FREQUENCY MONITORING

Small input frequency changes can be monitored more readily by using the programmable gain feature of models 451 and 453 to achieve greater signal sensitivity. In the application of model 451 illustrated in Figure 17, gain has been set to 0.1V/Hz, resulting in a 100Hz full scale frequency range. The output resolution for small changes occurring in the 60Hz line frequency has been improved. An additional advantage of this approach is the reduced accuracy and stability requirements placed on the relay trip levels, set by the voltage levels at the comparators. A precision voltage reference supply is not required.

Since both models 451 and 453 tolerate input signals up to the supply levels, $\pm V_S$, costly input protection is eliminated in most applications.

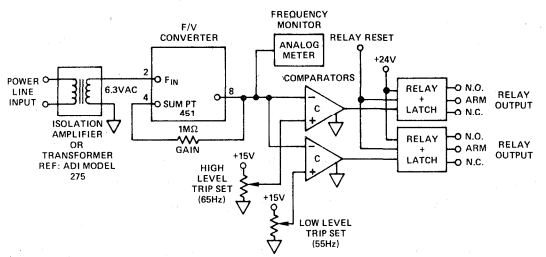


Figure 17. Application of F/V Converter to Monitor 60Hz Line Frequency

APPLICATION IN DATA ACQUISITION SYSTEMS

HIGH NOISE IMMUNITY TRANSMISSION

F/V converters are excellent companion products to V/F converters for use in low cost, two wire data transmission systems. As shown in Figure 18, this V/F/V approach utilizes the continuous self-clocking feature of the V/F converter thereby eliminating the need for costly additional twisted pair cable for external synchronization. Model 610 instrumentation amplifier amplifies the low level differential transducer signal to the 10V full scale of models 450 and 456 10kHz V/F converters. A differential line driver is used to drive a twisted pair cable through a noisy environment. A differential line receiver is used to drive model 451 10kHz F/V converter. The low cost of the V/F and F/V converters in addition to the simple twisted pair cabling approach make it economical to use a V/F/V converter pair for each channel in a data acquisition system.

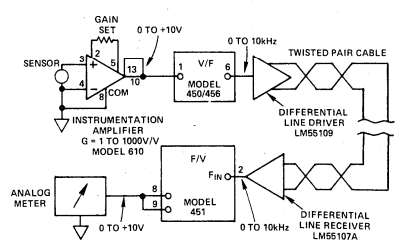


Figure 18. Application of F/V Converter in a Low Cost, High Noise Rejection Two-Wire Data Transmission System

High Accuracy, 100kHz and 1MHz Voltage to Frequency Converters

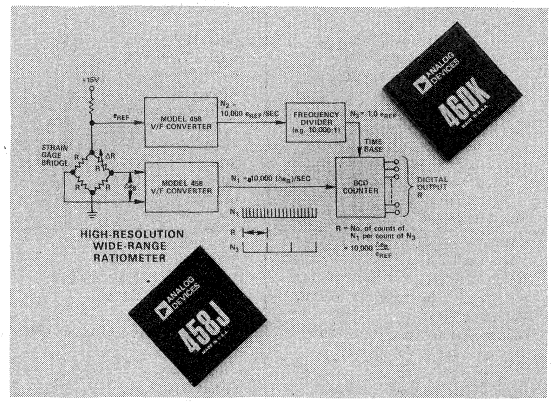
MODELS 458 and 460

FEATURES

High Stability: 5ppm/°C max, Model 458L
15ppm/°C max, Model 460L
Low Nonlinearity: 100ppm max, Model 458
150ppm max, Model 460
Versatility: Differential Input Stage
Voltage and Current Inputs
Floating Inputs: ±10V CMV
Wide Dynamic Range: 6 Decades, Model 460
TTL/DTL Compatible Output

APPLICATIONS

Fast Analog-to-Digital Converter
High Resolution Optical Data Link
Ratiometric Measurements
2-Wire High Noise Immunity Digital Transmission
Long Term Precision Integrator



GENERAL DESCRIPTION

Models 458 and 460 are high performance, differential input, voltage to frequency modular converters designed for analog to digital applications requiring accuracy and fast data conversion. Model 458 offers a 100kHz full scale frequency, guaranteed nonlinearity of ±0.01% maximum over five decades (1Hz to 100kHz) of operation and guaranteed low maximum gain drift in three model selections; model 458L: 5ppm/°C max; model 458K: 10ppm/°C max; and model 458J: 20ppm/°C max. Model 460 offers a 1MHz full scale frequency, guaranteed maximum nonlinearity of ±0.015% over six decades (1Hz to 1MHz) of operation and guaranteed low maximum gain drift in three selections; model 460L: 15ppm/°C max; model 460K: 25ppm/°C max; and model 460J: 50ppm/°C max. Model 460L is the industry's first 1MHz V/F converter to offer 15ppm/°C maximum gain drift.

The differential input stage of models 458 and 460 provide the versatility of either direct interface to off-ground 0 to +11V input signals with common mode voltages (CMV) to ±10V, as well as ground referenced positive, 0 to +11V or negative, 0 to -11V signals. Both models also accept positive current signals: 0 to +0.5mA, model 458; 0 to +1mA, model 460 for current to frequency (I/F) applications.

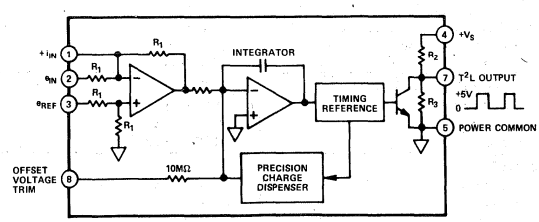
The rated performance of both models 458 and 460 is achieved without the need for external components or adjustments. Optional adjustments are available for trimming full scale frequency and the input offset voltage.

WHERE TO USE MODELS 458 AND 460

The combination of low gain drift, low nonlinearity and the versatility of a differential input with both high speed (100kHz/1MHz) models, offer excellent solutions to a wide variety of demanding applications; in high speed remote data acquisition systems – two wire data transmission over long wires; in 5½ digit DVM's – featuring high resolution A/D conversion, monotonic performance, no missing codes and high noise rejection; in strain gage bridge weighing applications – accurate ratiometric measurements over wide dynamic range.

DESIGN APPROACH - PRECISION CHARGE BALANCE

Models 458 and 460 incorporate a superior charge balance design that result in high linearity and temperature stability - see Figure 1. Both models accept unipolar, single-ended voltage or current input signals directly. By offsetting the input using the current terminal, models 458 and 460 will accept bipolar input voltages up to ±5V.



MODEL	FULL SCALE OUTPUT	R_1	R_2	R_3
458	100kHz	20kΩ	10kΩ	4.7kΩ
460	1MHz	10kΩ	2kΩ	910Ω

Figure 1. Block Diagram - Models 458, 460

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise noted)

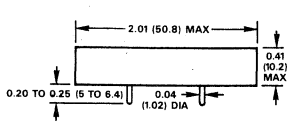
MODEL	100kHz Full Scale 458 J | K | L	1MHz Full Scale 460 J | K | L
TRANSFER FUNCTION		
Voltage Input	$f_{OUT} = (10^4 Hz/V)\ e_{IN}$	$f_{OUT} = (10^5 Hz/V)\ e_{IN}$
Current Input	$f_{OUT} = (2 \times 10^5 Hz/mA)\ i_{IN}$	$f_{OUT} = (10^6 Hz/mA)\ i_{IN}$
ANALOG INPUT		
Configuration	Differential	Differential
Voltage Signal Range		
e_{IN} Terminal (e_{REF} = 0)	0 to +10V dc min	0 to +10V dc min
e_{REF} Terminal (e_{IN} = 0)	0 to -10V dc min	0 to -10V dc min
Differential ($e_{IN} - e_{REF}$)	0 to +10V dc min	0 to +10V dc min
Overrange	+10% min	+10% min
Current Signal Range (i_{IN})	0 to +0.5mA min	0 to +1mA min
Common Mode Voltage	±10V	±10V
Common Mode Rejection	40dB	40dB
Impedance, e_{IN} Terminal	20kΩ	10kΩ
e_{REF} Terminal	40kΩ	20kΩ
i_{IN} Terminal	0Ω	0Ω
Max Safe Input	$\pm V_S$	$\pm V_S$
ACCURACY		
Warm Up Time	5 Seconds to 0.01%	2 Minutes to 0.02%
Nonlinearity, e_{IN} = +0.1mV to +11V	±0.01% of Full Scale, max	±0.015% of Full Scale, max
e_{IN} = -0.1mV to -11V	±0.01% of Full Scale	±0.015% of Full Scale
Full Scale Error[1]	+0.1% to +2%, max	+0.1% to +2%, max
Gain vs. Temperature (0 to +70°C)	±20ppm/°C max | ±10ppm/°C max | ±5ppm/°C max	±50ppm/°C max | ±25ppm/°C max | ±15ppm/°C max
vs. Supply Voltage	±15ppm/%	±25ppm/%
vs. Time	±10ppm/day	±10ppm/day
Input Offset Voltage[2]	±10mV max	±10mV max
vs. Temperature (0 to +70°C)	±30μV/°C max	±30μV/°C max
vs. Supply Voltage	±10μV/%	±10μV/%
vs. Time	±20ppm/day	±10ppm/day
RESPONSE		
Settling Time, ±0.01% +10V Step	3 Output Pulses Plus 2μs	2 Output Pulses Plus 2μs
Overload Recovery Time	10ms	1ms
FREQUENCY OUTPUT[3]		
Waveform	TTL/DTL Compatible Pulses	TTL/DTL Compatible Pulses
Pulse Width	5μs	500ns
Rise and Fall Time	300ns/50ns	60ns/50ns
Pulse Polarity	Positive	Positive
Logic "1" (High) Level	+2.4V min	+2.4V min
Logic "0" (Low) Level	+0.4V max	+0.4V max
Capacitive Loading	500pF max	200pF max
Fan Out Loading	10 TTL Loads min	10 TTL Loads min
Impedance	3kΩ (High State)	670Ω (High State)
POWER SUPPLY[4]		
Voltage, Rated Performance	±15V dc	±15V dc
Voltage, Operating	±(13 to 18)V dc	±(13 to 18)V dc
Current, Quiescent	(+25, -8)mA	(+25, -8)mA
TEMPERATURE RANGE		
Rated Performance	0 to +70°C	0 to +70°C
Operating	-25°C to +85°C	-25°C to +85°C
Storage	-55°C to +125°C	-55°C to +125°C
MECHANICAL		
Case Size	2" x 2" x 0.4"	2" x 2" x 0.4"
Weight	45 Grams	45 Grams
Mating Socket	AC1016	AC1016

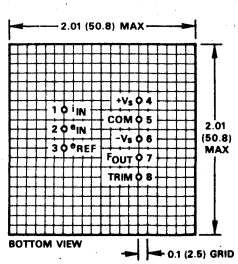
[1] Adjustable to zero using 500Ω potentiometer.
[2] Adjustable to zero using 50kΩ potentiometer.
[3] Protected for continuous short-circuits to ground and momentary (less than 1 sec) shorts to the $+V_S$ supply. Output is not protected for shorts to the $-V_S$ supply.
[4] Recommended power supply, ADI model 904, ±15V @ 50mA output.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).





MATING SOCKET: AC1016

VOLTAGE TO FREQUENCY OPERATION

Models 458 and 460 provide accurate conversion of analog signals into a train of constant width and constant amplitude pulses at a rate directly proportional to the analog signal amplitude. The output continuously tracks the input signal, responding directly to changes in the input signal; external clock synchronization is not required. The output pulse train is TTL/DTL compatible, permitting direct interface to digital processing circuits.

BASIC V/F HOOK-UP AND OPTIONAL TRIMS

Models 458 and 460 can be applied directly to achieve rated performance without external trim potentiometers or other components. Figures 2, 3 and 4 below illustrate the basic wiring connections for either V/F converter model. Using the basic hookup without trims, full scale (e_{IN} = 10V) accuracy is +0.1% to +2% and the input offset voltage is ±10mV max. The full scale and input offset voltage errors can be eliminated by using the FINE TRIM PROCEDURE.

FINE TRIM PROCEDURE

Connect the optional trims as shown in Figure 2, 3 or 4 and allow a five minute warm-up after initial power turn-on. Using a precision, stable voltage source, set the input voltage, e_S, to 10mV. Adjust the OFFSET trim, R_O, for an output pulse interval of 0.1 sec (model 458) or 0.01 sec (model 460).

V/F INTERCONNECTIONS

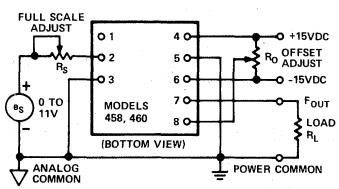


Figure 2. Positive Input Signal

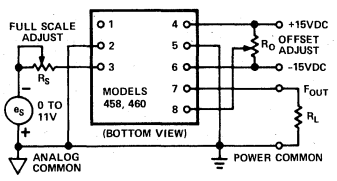


Figure 3. Negative Input Signal

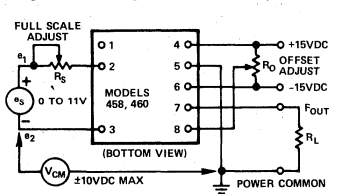


Figure 4. Floating Input Signal

EXTERNAL CONNECTIONS FOR VOLTAGE TO FREQUENCY OPERATION, WITH OPTIONAL INPUT OFFSET VOLTAGE AND FULL SCALE FREQUENCY ADJUSTMENTS

R_S = FULL SCALE ADJUSTMENT; 500Ω (Use low T.C. Cermet, <50ppm/°C or equivalent)
R_O = INPUT OFFSET ADJUSTMENT; 50kΩ (Use low T.C. Cermet, <50ppm/°C or equivalent)

CAUTION: DO NOT SHORT OUTPUT TERMINAL TO -15V

Set the input voltage to +10.000V and adjust the FULL SCALE trim for an output pulse frequency of 100kHz (model 458), or 1MHz (model 460). The V/F converter may now be used without further adjustment.

DIFFERENTIAL INPUT

The e_{IN} and e_{REF} input terminals represent a true differential input capable of accepting a signal from a strain gage bridge, a balanced line, or a signal source sitting at a common mode voltage. The differential input eliminates the need for a differential amplifier to handle these signals.

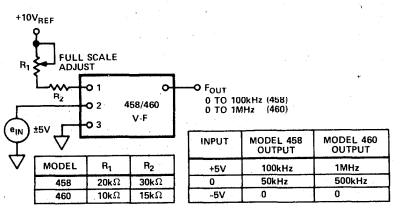
To apply the 458 or 460 voltage inputs differentially, the e_{IN} pin must always be positive with respect to the e_{REF} pin as shown in Figure 4. The differential signal source may be completely floating with common mode voltages up to ±10V max. For differential inputs the output frequency is:

$$F_{OUT} = \left[\underbrace{(e_1 - e_2)}_{\text{INPUT SIGNAL}} + \underbrace{\left(\frac{e_1 + e_2}{2}\right) \times \left(\frac{1}{CMR}\right)}_{\text{CMR ERROR}} \right] K_g$$

K_g = 10^4 Hz/V; model 458
10^5 Hz/V; model 460

OFFSETTING INPUT FOR BIPOLAR INPUTS

The input summing terminal, $+i_{IN}$, may be used to improve dynamic response as well as scale the output frequency to directly convert bipolar input voltages. An offset current is fed through an external resistor from a stable voltage reference. As shown in Figure 5, input voltages of ±5V min can be converted directly.

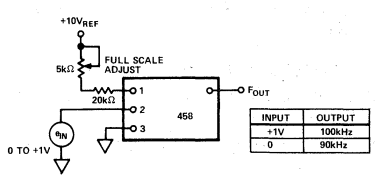


MODEL	R_1	R_2
458	20kΩ	30kΩ
460	10kΩ	15kΩ

INPUT	MODEL 458 OUTPUT	MODEL 460 OUTPUT
+5V	100kHz	1MHz
0	50kHz	500kHz
-5V	0	0

Figure 5. Offsetting Input to Accept ±5V Bipolar Inputs

The output may also be scaled up so that low amplitude signals, such as 1V will give full scale output frequency; 100kHz model 458 or 1MHz model 460. By scaling the output frequency for low level signals, the step response will significantly improve. As shown in Figure 6 for model 458, the step response for a 1 volt input decreases from 200μs before input scaling, to 20μs with scaling.



INPUT	OUTPUT
+1V	100kHz
0	90kHz

Figure 6. Offsetting Input to Achieve Improved Dynamic Response for Small Signal Inputs

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PERFORMANCE SPECIFICATIONS

Nonlinearity: Nonlinearity error is specified as a % of 10V full scale input and is guaranteed over the 0.1mV to 11V operating signal range; ±0.01% max, models 458J/K/L, ±0.015% max, models 460J/K/L. Typical nonlinearity performance is illustrated in Figure 7.

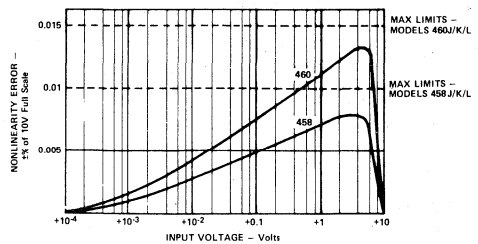


Figure 7. Nonlinearity Error Versus Input Voltage

Gain Temperature Stability: Gain drift is specified in ppm of output signal and is guaranteed for each model over the 0 to +70°C temperature range; 5ppm/°C (458L), 10ppm/°C (458K), 20ppm/°C (458J), 15ppm/°C (460L), 25ppm/°C (460K) and 50ppm/°C (460J) max.

LONG TERM PRECISION INTEGRATOR

In critical measurement applications, such as pollution monitoring where it is required to integrate for periods greater than 1 hour with overall accuracy of 0.05%, the V/F converter offers a superior low cost approach when compared to the traditional operational integrator circuit. As shown in Figure 8, the analog signal is applied to a precision input amplifier, model 52K and then to the V/F input. The V/F output is connected to a large capacity counter and display, operating as a totalizer. The total pulse count is equal to the time integral of the analog input signal. Since the output displayed is an accumulated pulse count, there is no integrator drift error. A feature of this approach is the infinite hold capability without errors due to time drift, since the counter may be held at any time without affecting the output reading.

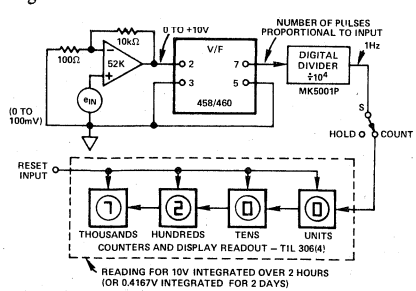


Figure 8. Models 458/460 as Long Term Integrator with Arbitrary Display Calibration. Frequency Division Ratio can Otherwise be Chosen to Provide Direct Readout in any Desired Units.

CMOS/HNIL COMPATIBLE OUTPUT

The circuit shown in Figure 9 may be used to shift the output of the 458/460 from 0 to +5V to 0 to +12V, to provide a 4V noise immunity for driving high noise immunity logic (HNIL) and CMOS logic.

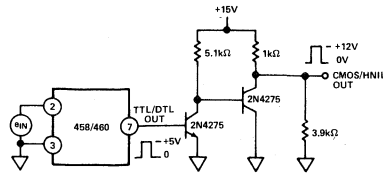


Figure 9. Circuit for Shifting the Output of the 458/460 to Drive CMOS/HNIL Logic

PRECISION HIGH CMV ANALOG ISOLATOR

By combining the V/F converter with a floating power supply and optical isolator as shown in Figure 10, accurate low level measurements in the presence of high common mode voltages may be achieved. Only the CMV rating of the optical isolator and the breakdown rating of the power supply limit the CMV rating. Using this approach for isolating transducers, ground loop problems are eliminated. Cost and complexity are minimized since only a single optical isolator is required to couple the serial pulse output from the V/F to the digital readout.

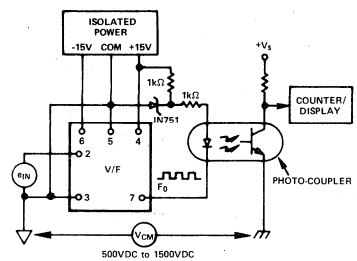


Figure 10. Optical Isolation Using LED Photo Isolator to Provide Up to 1500V dc CMV Isolation

APPLICATION IN DATA ACQUISITION SYSTEMS

High Noise Immunity Data Transmission: A method of accurately transmitting analog data through high noise environments is illustrated in Figure 11. This approach utilizes the self clocking output of models 458 and 460 and eliminates the need for costly additional twisted pair for external synchronization. Model 610 amplifies the low level differential transducer signal up to the 10V full scale V/F input level. A differential line driver is used to drive a twisted pair cable. The differential line driver and receiver offer high noise immunity to common mode noise signals.

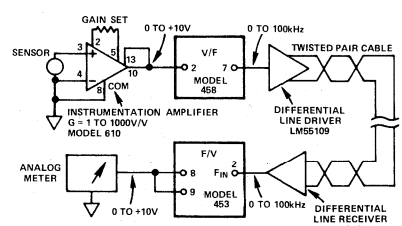


Figure 11. Application of Model 458 V/F Converter in a High Performance, High Noise Rejection Two-Wire Data Transmission System

Synchro & Resolver Converters

Contents

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TSL1612 Processors for 2-Speed Synchro-to-Digital Conversion	13-59

•New product since *1980 Data-Acquisition Components and Subsystems Catalog*

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Selection Guide
Synchro & Resolver Converters

The products in this section are generally concerned with angular measurements. They include the following classes of device:

Digital Angle to Trigonometric (sine-cosine) Analog Voltage
Digital-to-Resolver Converters
Digital-to-Synchro Converters
Inductosyn™-to-Digital Converters
Resolver-to-Analog Voltage Converters
Resolver-to-Digital Converters
Resolver-to-Digital Display (Angular-Position Indicators)
Synchro-to-Analog Voltage Converters
Synchro-to-Digital Converters
Synchro-to-Digital Display (Angular-Position Indicators)

Complete descriptions, specifications, and applications information on the products in this section can be found in the data sheets. Brief general information can be found overleaf.

The Selection Guide is provided to ease the job of finding the right unit to do your job. Devices are listed in the Selection Guide vertically, by model number, in alphabetic, then numeric order, as well as by function and type of input. Salient characteristics are listed horizontally. A bullet is placed at each intersection that is appropriate for each device.

			ANALOG I/O					DIGITAL I/O							
								BCD			RESOLUTION (BITS)				
			SYNCHRO	RESOLVER	INDUCTOSYN™	LINEAR	BINARY	0 to ±180°	0 to 360°	PULSE TRAIN	18	16	14	12	10
SYNCHRO RESOLVER INPUT	Angle Position Indicator	API1620	•	•			•	•				•			
		API1718	•	•			•	•				•			
DIGITAL INPUT	Digital to Synchro Resolver	DSC1705	•	•			•						•		
		DSC1706	•	•			•							•	
	Digital to Trig. (Analog)	DTM1716				•							•		
		DTM1717				•								•	
INDUCTOSYN	Inductosyn/ Resolver to Digital	IRDC1730		•	•		•							•	
		IRDC1731		•	•		•		•					•	
RESOLVER INPUT	Resolver to Digital Converters	RDC1727		•			•				•				
		RDC1740		•			•						•		
		RDC1741		•			•							•	
		RDC1742		•			•							•	
SYNCHRO INPUT	Sync/Resolver Analog	SAC1763	•	•		•									
	Synchro or Resolver to BCD Converters	SBCD1752	•	•				•					•[1]		
		SBCD1753	•	•				•					•[2]		
		SBCD1756	•	•					•				•[1]		
		SBCD1757	•	•					•				•[2]		
	Synchro or Resolver to Binary	SDC1700	•	•			•							•	
		SDC1702	•	•			•								•
		SDC1704	•	•			•						•		
		SDC1725	•	•			•							•	
		SDC1726	•	•			•								•
	Synchro to Digital	SDC1727	•				•				•				
		SDC1740	•				•						•		
		SDC1741	•				•							•	
		SDC1742	•				•							•	

[1] 13 Bit BCD plus sign.
[2] 14 Bits BCD.
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Here's an example of its use: if you were looking for a 14-bit resolver-to-digital converter with the highest accuracy in the smallest package, you night start at the 14-bit column; you would see that there are two resolver families that have 14-bit resolution and error less than 5 arc-minutes: RDC1740 and SDC1704; the RDC1740 is a hybrid, and the SDC1704 is in a 0.4″H module. Thus, you would be quickly led to look at the SDC/RDC1740 data sheet and be guided to its location by the page number at the right.

In addition to the devices listed in the chart, data sheets for the following accessory products are also to be found in this section:

Resolver and Synchro 5VA Output Transformers, models RTM/STM1686/1696/1736/1687/1697/1737 — Volume II, Page 13-27

Synchro/Resolver 5VA-Output Power Amplifier, model SPA1695 — Volume II, Page 13-57

Two-Speed Processor for Coarse/Fine Synchro/Resolver Systems, model TSL1612 — Volume II, Page 13-59

ACCURACY (arc-min)						ASSEMBLY/PACKAGE TECHNOLOGY				PAGE		
						MODULE						
<1	<5	<10	<20	>20	HYBRID	<0.4″H	0.4″H	>0.4″H	INSTRUMENT	VOLUME I	VOLUME II	
	•								•	–	13-5	API1620
	•								•	–	13-5	API1718
	•							•		–	13-9	DSC1705
		•						•		–	13-9	DSC1706
	•						•			–	13-13	DTM1716
	•						•			–	13-13	DTM1717
			•				•			–	13-17	IRDC1730
			•				•			–	13-23	IRDC1731
•								•		–	13-49	RDC1727
	•				•					13-5	13-53	RDC1740
			•		•					13-5	13-53	RDC1741
		•			•					13-5	13-53	RDC1742
			•					•		–	13-31	SAC1763
			•					•		–	13-35	SBCD1752
			•					•		–	13-35	SBCD1753
			•					•		–	13-35	SBCD1756
			•					•		–	13-35	SBCD1757
		•					•			–	13-39	SDC1700
				•			•			–	13-39	SDC1702
	•						•			–	13-39	SDC1704
	•					•				–	13-45	SDC1725
			•			•				–	13-45	SDC1726
•								•		–	13-49	SDC1727
	•				•					13-5	13-53	SDC1740
			•		•					13-5	13-53	SDC1741
		•			•					13-5	13-53	SDC1742

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Orientation
Synchro & Resolver Converters

These products constitute a complete line of devices for the digital measurement and control of angular and linear displacements by means of synchros, resolvers, and Inductosyns. In addition to modules and hybrid circuits that perform the appropriate conversions, the line also includes modules that perform purely algebraic or logical functions; in some cases, solid-state circuitry emulates the functions of electromechanical devices.

The range of synchro processing modules now available covers a wide area of application. They are widely used in military and radar applications, but there are additional fields in which they could be used to advantage because of the proven ruggedness and high precision of the electromechanical hardware, their standardized specifications, and their low cost. They have a number of advantages over potentiometers and optical systems.

In this introductory section, there will be provided a brief set of device definitions. Detailed data and applications information is given in the data sheets. For a complete introduction to synchro/digital conversion, Analog Devices has available a 208-page book, *Synchro and Resolver Conversion*, edited by G. Boyes (1980), $11.50.

In this section, and in much of the text, the word "Synchro" appears frequently. In many cases, the word "Resolver" could be used in its place. The modules make use of angular data in resolver form; if the input data is in three-wire synchro form, transformers in "Scott T" configuration convert it to resolver form; analog outputs are available in both forms. There are a number of voltage and frequency options.

REPRESENTATION OF ANGLES IN DIGITAL FORM

Binary

The most commonly used method of representing angles in digital form is simple natural binary weighting, where the most-significant bit (MSB) represents 180°, the next represents 90°, etc. The table shows the bit weights in degrees, degrees-and-minutes, and radians for this coding method.

BCD

When angular measures have to be displayed in visual form, BCD coding is used, through the use of binary-to-BCD converters, such as the BDM1615, which provides the necessary scaling and conversion, e.g., from 10100000000000 (180° + 45°) to 10 0010 0101.0000 000 (or 225.00°).

TYPICAL S/D/S DEVICES

Binary-to-Binary-Coded-Digital Converter (BDM1615/16/17)

A device that accepts angular data in binary form and converts it to BCD form, with fractional degrees in decimal fractions of 1° (1615, 1617) or minutes and seconds (1616). The BCD output is modulo 360°.

Bit No.	Degrees	Degrees, minutes		Radians
1	180	180	0	3.141593
2	90	90	0	1.570796
3	45	45	0	0.785398
4	22.5	22	30	0.392699
5	11.25	11	15	0.196349
6	5.625	5	37.5	0.098175
7	2.8125	2	48.75	0.049087
8	1.40625	1	24.38	0.024544
9	0.70312	0	42.19	0.012272
10	0.35156	0	21.09	0.006136
11	0.17578	0	10.55	0.003068
12	0.08789	0	5.27	0.001534
13	0.04395	0	2.64	0.000767
14	0.02197	0	1.32	0.000383
15	0.01099	0	0.66	0.000192
16	0.00549	0	0.33	0.000096

Digital-to-Synchro Converters (DSC1705/06)

Devices that accept parallel binary digital inputs (14 or 12 bits) and an ac reference signal, and provide outputs in 3-wire synchro form.

Inductosyn/Resolver-to-Digital Converter (IRDC1730)

A device that produces a digital output capable of resolving (to 12 bits) intermediate distances within a single track-pitch of a Farrand linear-Inductosyn stator in displacement- and angle-measuring Inductosyn systems. The moving element is used as though it were a resolver input; hence the device will also convert resolver information to digital.

Synchro-to-Digital Converter

A device that accepts either 3-wire synchro- or 4-wire resolver inputs, together with a 2-wire ac reference, and outputs angular binary data in a continuously tracking mode, employing a Type 2 servo loop. The inputs may be from either remote synchros or from electrically simulated synchros (e.g., DSC's).

Digital Converter and Processor for Two-Speed Synchros (TSL1612)

A two-speed processor takes as inputs two sets of digital information, representing the angles from coarse and fine synchros, and combines them to produce a single 19-bit word representing the actual angle of the "coarse" shaft. The TSL consists of the processing logic alone—it can be used with a pair of SDC's, which provide the two sets of digital information.

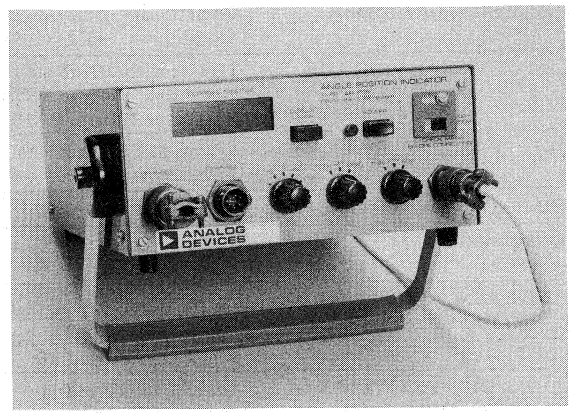
Synchro/Resolver Angle Position Indicators and Digital Converter

API1620 and API1718

FEATURES
Five Digit Display
Accuracy 0.02° (API1620) or 2 arc-minutes (API1718)
Two Channel Input
Accepts High or Low Level Synchros, Resolvers or Magslips
47Hz to 600Hz Carrier Frequency
16-Bit BCD or Natural Binary Output
Storage Compartment for Leads/Connectors

API1620 FEATURES
Degrees and Decimal Parts of a Degree Display
Display Test Facility
Full Scale 359.99°

API1718 FEATURES
Nato Codified
Degrees and Minutes Display
Display Latch Facility
Full Scale 359° 59′



DESCRIPTION
The Angle Position Indicators API1620 and API1718 are instruments for displaying in visual digital form the angle represented by synchro, magslip or resolver signals. In addition to displaying the angle in visual form the APIs also convert the input angular signals into natural binary or BCD angular data at TTL levels for use externally. Facility is provided for the connection of two sets of input signals which may be alternately switched into the converter. The APIs have been designed to accommodate input signals from all the usually encountered angular data transmission systems i.e., Synchros, Magslips and Resolvers at both high and low voltage levels and at frequencies from 47Hz to 600Hz. The two sets of inputs to the APIs can be different e.g., a 60Hz synchro on one input together with a 400Hz resolver on the other. The facility of switching from one set of inputs to the other enables the angular position of separate devices to be directly compared. The meters have been designed to work with any reference voltage from 6V rms to 115V rms.

STORAGE COMPARTMENT
A storage compartment for storing the input leads and connectors is provided on the underside of the instrument, access to this is by an easily operated slotted screw fastener. The API is delivered with part of the Application Kit stored in this compartment.

SELF TESTING
Both Angle Position Indicators have a self checking facility. This is provided by internally simulated input angles of 45° and 225° selected by the front panel mode switch. The simulated angles have an accuracy an order of magnitude greater than the Instrument.

NATO CODE NUMBER
The API1718 BCD option has been issued with a Nato Stock Number, 6625-99-539-8389, which eases acceptance of the Angle Position Indicator in military applications.

MODELS AVAILABLE
The two Angle Position Indicators described in this data sheet differ primarily in the format of the display and the presence of a Display Check or Display Latch facility.

Model API1620 has a display format of degrees and decimal parts of a degree with a full scale range of 359.99° and an accuracy of 0.02°. It has a display check facility on the front panel and is available in two options, viz.

BINARY option has 16-bit representation at TTL levels of the input angular signal in natural binary form on the rear connector.

BCD option has a 5 decade BCD representation at TTL levels of the input angular signal on the rear connector.

Model API1718 has a display format of degrees and minutes with a full scale range of 359° 59 minutes and an accuracy of 2 arc minutes. It has a display latch facility on the front panel and is available in two options, viz.

BINARY option has a 16-bit representation at TTL levels of the input angular signal in natural binary form on the rear connector.

BCD option has a 5 decade BCD representation at TTL levels of the input angular signal on the rear connector.

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SPECIFICATIONS (typical @ +25°C unless otherwise noted)

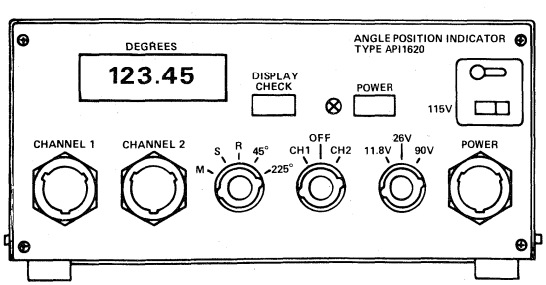
Models	API1620	API1718
ACCURACY[1]	±0.02° at 400Hz ±0.03° at 60Hz	2 arc minutes at 400Hz 3 arc minutes at 60Hz
ANGULAR RANGE	000.00° to 359.99° continuous rotation	000.00° to 359° 59 minutes continuous rotation
TEMPERATURE RANGE	Operational 0 to +50°C Storage -5°C to +55°C	*
INPUT SIGNAL VOLTAGE	11.8V rms 200Hz to 600Hz 26.0V rms 200Hz to 600Hz 90.0V rms 47Hz to 600Hz	*
REFERENCE VOLTAGE	6V rms to 115V rms with no adjustments required	*
REFERENCE FREQUENCY	47Hz to 600Hz	*
INPUT IMPEDANCE	Signal 2MΩ Reference 200kΩ	*
TOLERANCE ON SIGNAL TO REFERENCE PHASE	±20°	*
DISPLAY	5 digit, dot matrix LED	*
DATA OUTPUT (TTL) ON REAR CONNECTOR (BCD 2TTL Loads, Binary 3TTL Loads)	Either 5 decade BCD or 16-bit natural binary. Degrees and decimal parts of a degree format.	*
INHIBIT INPUT (TTL) (1TTL LOAD)	Logic "0" = Hold Logic "1" = Track	*
BUSY OUTPUT (TTL) (10TTL LOADS)	Logic "0" = Data Stable Logic "1" = Busy	*
POWER SUPPLY	23VA (typ), 28VA (max) at either 115V rms or 220V rms ±15% 47Hz to 400Hz	*
WEIGHT	10 lbs 4.53Kgm	*
SIZE (EXCLUDING HANDLE)	11.75" X 8" X 4" (300mm X 204mm X 102mm)	*
NATO STOCK NO.	–	6625–99–539–8389 (BCD version only)

NOTES

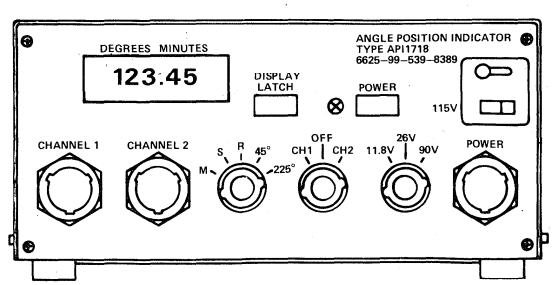
*Specifications same as API1620.

[1] Full accuracy is maintained if signal voltages within ±10% of the nominal values are applied (all lines varying together). The input amplifier limits are set at +15% of the nominal voltage levels, no damage will occur if 90 volts is applied on the 11.8 volts or 26.0 volt settings and up to 150 volts can be applied on the 90 volts setting without damage. For voltages considerably lower than the normal voltages the API will continue to function at a reduced accuracy; the inaccuracy will manifest itself mainly as an hysteresis error.

Specifications subject to change without notice.



Front Panel of the API1620



Front Panel of the API1718

DATA READOUT

The digital angle readout is displayed on a five digit display by Light Emitting Diode (LED) dot matrix indicators on the front panel.

The API1620 model displays this angle as degrees and hundredths of a degree.

The API1718 model displays this angle as degrees and minutes.

The displayed angle is also available at TTL levels in either Binary or BCD format on the rear connector. *In both APIs this angle is produced in degrees and hundredths of a degree.*

DISPLAY CHECK (API1620)

The API1620 has a display check press button on the front panel which when pressed causes all the dots in all LED matrices to be illuminated.

POWER CONNECTIONS

The Angle Position Indicators can be powered from 115V ac or 220V ac ±15%, the changeover switch being on the front panel. The supply frequency can be 47Hz to 400Hz.

DISPLAY LATCH (API1718)

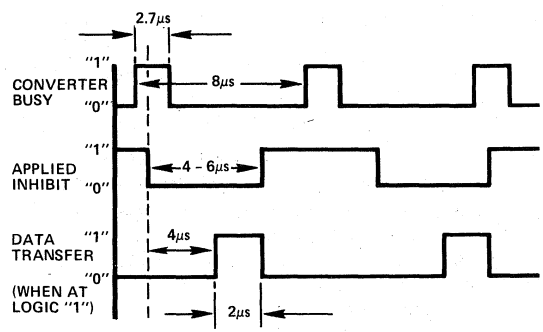
The API1718 has a Display Latch button on the front panel which when pressed will hold the display at its existing reading —but does not effect the digital output data.

Both APIs have a latch facility available on Pin 36 on the rear connector. This "$\overline{\text{INHIBIT}}$" input will "Freeze" both the display and the digital output data if a Logic "0" is applied.

OUTPUTTING VALID DATA

A "Converter Busy" pulse is available on Pin 37 of the rear connector, which indicates the state of the converter. When this line is at Logic 1 the converter is busy and the data is changing. A Logic 0 indicates that the data is valid.

Data can be transmitted without error under the following timing sequence.



Data Transfer Waveforms

DATA OUTPUT CONNECTIONS AND BIT WEIGHTS

The APIs are available in two forms one giving the output in BCD form and the other giving the output in natural binary form. In both cases the resolution corresponds to 16-bits binary. The pin connections for the 37 way DCM 37S Souriau rear connector are given in the following table.

OPERATING NOTES

The line voltage selector switch must be set in the correct position before the power is applied. To the left of the voltage selector switch is the instrument "on/off" press button and to the left of that is the power indicator neon.

PIN NUMBER	NATURAL BINARY VERSION BIT NO.	BIT WEIGHT	BCD VERSION CODING
1	GROUND		GROUND
2	16	0·0055	0·01°
3	15	0·0110	0·02°
4	14	0·0220	0·04°
5	13	0·0439	0·08°
6	12	0·0879	0·10°
7	11	0·1758	0·20°
8	10	0·3516	0·40°
9	9	0·7031	0·80°
10	N/C		1·0°
11	N/C		2·0°
12	8	1·4063	4·0°
13	7	2·8125	8·0°
14	6	5·6250	10·0°
15	5	11·2500	20·0°
16	4	22·5000	40·0°
17	3	45·0000	80·0°
18	2	90·0000	100·0°
19	1	180·0000	200·0°
20	N/C		N/C
TO↓	••		TO↓
35	N/C		N/C
36	$\overline{\text{INHIBIT}}$		$\overline{\text{INHIBIT}}$
37	BUSY		BUSY

Connections on Output Connector at rear of API

SIGNAL VOLTAGE SELECTOR SWITCH

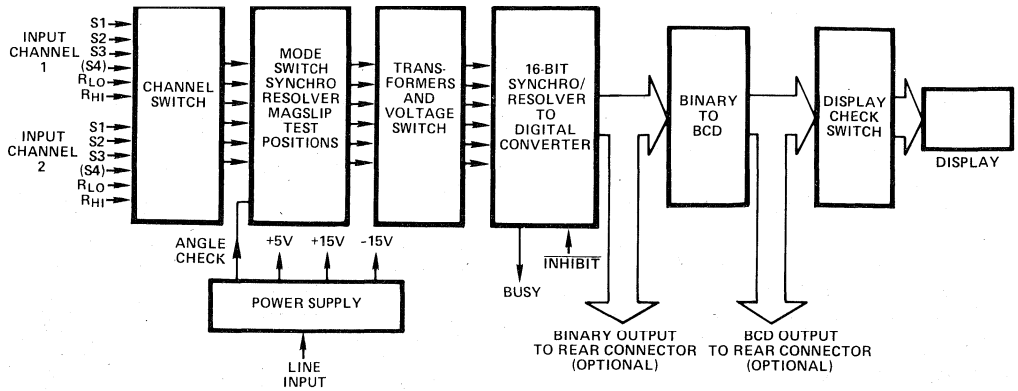
The three position selector switch alters the transformers to suit the synchro or resolver voltages being applied to the API. THIS SWITCH SHOULD BE SET IN THE 90 VOLT POSITION DURING 45° OR 225° CHECKING, no damage will be done if this or any of the switches are in wrong positions but errors in checking could occur.

MODE SELECTOR SWITCH

This mode selector switch marked M, S, R, 45°, 225° meaning Magslip, Synchro, Resolver, 45° check and 225° check is for making appropriate changes according to whether a magslip synchro or resolver is being used. If two differing systems are being applied to the inputs e.g. Channel 1 resolver at 26V and Channel 2 synchro 90V, then the mode switch will have to be changed from R to S and the voltage switch from 26V to 90V when changing from Channel 1 to Channel 2. No damage will be done to the API by any order of switching but some change of loading on the inputs may occur. To avoid this problem the channel switch marked CH1, OFF, CH2 should be set in the OFF position when changing the mode and voltage switches.

DIRECTION OF DATA ROTATION

The convention of zero angle on Magslips differs from Synchros by 150°. Correction for this has been made inside the APIs, so that zero degrees will be indicated on the API for both Synchro and Magslips set to zero. The direction of rotation convention is different for Synchros and Magslips this has not been changed so that a clockwise rotation (from zero) of the synchro will give the same reading as an anticlockwise rotation (from zero) of a Magslip.



Schematic Arrangement of the API1620 and API1718

REFERENCE INPUT

Both the Angle Position Indicators require a reference voltage to be supplied via the input connectors. This must be the same reference as supplied to the devices under test and can be any voltage from 6V rms 115V rms.

POWER AND SIGNAL INPUT CONNECTIONS

The power and input connectors have lettered pins (see table on previous page). Connections are:

Power

Fixed Connector: Amphenol 62GB-57A-8-3.3P
Free Connector: Amphenol 62GB-16F-8-3.3S

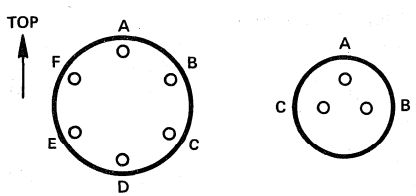
3 Way:	Pin A	Ground
	Pin B	Live
	Pin C	Neutral

Inputs

Fixed Connector: Amphenol 62GB-57A-10-6P
Free Connector: Amphenol 62GB-16F-10-6S

6 Way:	Pin A to S1	Pin D to S4
	Pin B to S3	Pin E to Ref High
	Pin C to S2	Pin F to Ref Low

For resolver inputs the sine voltage is applied to S1 and S3 and the cosine to S2 and S4. The phase of the resolver connections should be such that if S3 and S4 and Ref Low are regarded as common then in the first angular quadrant 0 to 90° the voltages on S2 and Ref High will be in time phase, i.e., positive together and negative together and the voltages on S1 and Ref High will be 180° out of time phase. For synchro or magslip operation the connections should be made to S1, S2 and S3 in rotation.



Pin Connections as Viewed Looking at the Front of the API1620 and API1718

APPLICATIONS OF THE ANGLE POSITION INDICATOR

The API finds many applications in both civil and military systems where it is common place to use synchro or resolver angular data transmission.

In many areas of mechanical engineering where angular settings have to be made to high accuracies, the APIs can be used with a precision synchro to display the shaft angle—or by using both inputs to compare shaft angle settings.

Other examples of the API's applications are checking constant velocity, coupling (universal joints) and measuring nonuniformity in the gearing velocity of gear boxes. By converting the digital output data to printers, permanent records can be obtained.

FUSES

The API1620 is protected by a 300mA anti-surge fuse in the fuse holder in the rear panel. The API1718 has two 160mA anti-surge fuses located on the rear panel for 240V operation. When used at 115V the 300mA fuses supplied should be fitted.

ORDERING INFORMATION

The APIs should be ordered according to the following:

API1620/BCD	degrees and hundredths display. BCD digital data output on rear connector.
API1620/BIN	degrees and hundredths display. Binary digital data output on rear connector.
API1718/BCD	degrees and minutes display. BCD digital data output on rear connector. Nato Code: 6625—99—539—8389.
API1718/BIN	degrees and minutes display. Binary digital data output on rear connector.

The API1620 is supplied with the following applications kit: 2 input connectors Amphenol sockets type 62GB—16F10—6S, 1 mains lead with Amphenol socket type 62GB—16F8—3.3S attached, one 37 way DCM37S Souriau connector with cover and spring clip. 1 Users Handbook. Calibration Result Sheet.

The API1718 is supplied with the following applications kit: 2 input leads with Amphenol socket type 62GB—16F10—6S attached. (Nato stock number 6625—99—541—3454). 1 mains lead with Amphenol socket type 62GB—16F8—3.3S attached. (Nato stock number 6625—99—541—3453). One 37 way connector DCM37S/Souriau connector with cover and spring clip. 1 Users Handbook. 3 Spare fuses (one 160mA anti-surge, two 300mA anti-surge). Calibration result sheet.

ANALOG DEVICES

Digital to Synchro Converters

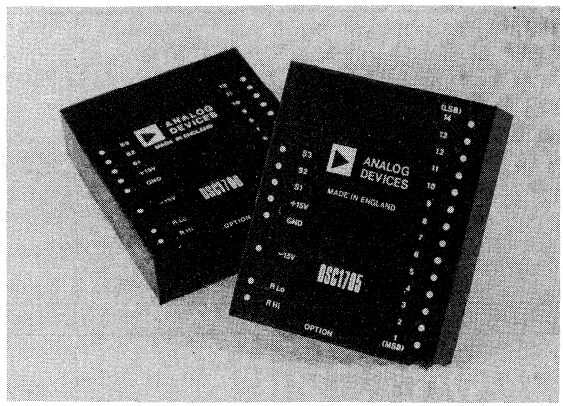
DSC1705/1706

FEATURES

- Very Low Radius Vector Variation (Transformation Ratio) (±0.1%)
- High Accuracy (±2 arc-mins at +25°C)
- 12- or 14-Bit Resolution
- No 5 Volt Power Supply Required
- MIL Spec/Hi Rel Versions Available
- Internal 1.3VA Amplifiers
- Internal Transformers (400Hz Option)
- No Trims or Adjustments Necessary

APPLICATIONS

- Driving Control Transformers
- Driving Torque Receivers (with External Amplifiers)
- Servo Mechanisms
- Retransmission Systems
- Positional Control



GENERAL DESCRIPTION

The DSC1705 and DSC1706 are Digital to Synchro and Digital to Resolver converters capable of driving electromechanical loads of up to 1.3VA.

They accept a 14- or 12-bit digital input representing angle and a reference voltage of either 60Hz or 400Hz, and produce a 3 wire or 4 wire output suitable for driving Synchros or Resolvers.

The 400Hz converters contain internal 1.3VA amplifiers as well as output and reference transformers.

The 60Hz versions contain internal 1.3VA amplifiers but require external output and reference transformers.

If it is necessary to drive a load requiring more than 1.3VA, options for both the 400Hz and 60Hz converters are available allowing the use of external amplifiers and transformers.

RADIUS VECTOR

One of the outstanding features of these converters is the almost negligible Radius Vector variation (Transformation Ratio).

On many Digital to Synchro Converters presently available, the individual sine and cosine outputs produced do not follow the exact sine and cosine laws, and depending upon angle can vary up to ±7%. This is not always important as the ratio of the sine to the cosine, i.e., the tangent, is always correct to the specified accuracy of the converter. There are cases however, when driving torque receivers and certain servo control loops when this variation is unacceptable.

The design of the DSC1705 and DSC1706 has reduced this variation to less than ±0.1%. This means that when the converters are used in closed loop servo systems, the gain of the closed loop is independent of the digital input angle, thus making reference correction unnecessary.

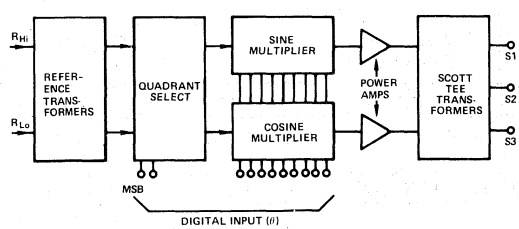
MODELS AVAILABLE

The two Digital to Synchro/Resolver converters described in this data sheet differ primarily in the areas of resolution and accuracy as follows:

Model DSC1705XYZ is a 14-bit converter with an overall accuracy of ±4 arc-minutes.

Model DSC1706XYZ is a 12-bit converter with an overall accuracy of ±8 arc-minutes.

The XYZ option code defines the option thus: (X) signifies the operating temperature range, (Y) signifies the reference frequency, (Z) signifies the output and the reference voltages, whether the output is in Synchro or Resolver format and whether external transformers are required.



Principle of Operation

FUNCTIONAL DIAGRAM, DSC1705 and DSC1706

The principle of operation of the converters described in this data sheet is shown in the diagram above.

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SPECIFICATIONS (typical @ +25°C unless otherwise noted)

Model	DSC1705	DSC1706
ACCURACY[1]	±4 arc-minutes	±8 arc-minutes
RESOLUTION	14 Bits (1LSB = 1.3 arc-minutes)	12 Bits (1LSB = 5.3 arc-minutes)
INPUT CODE	14-Bits Natural Parallel Binary with MSB = 180°	12-Bits Natural Parallel Binary with MSB = 180°
REFERENCE VOLTAGE INPUT		
With Internal Transformers		
Low Level	26V rms	*
High Level	115V rms	*
External Transformer Options[2]	4V rms	*
REFERENCE FREQUENCY	60Hz or 400Hz	*
REFERENCE INPUT IMPEDANCE		
With Internal Transformers		
Low Level	20kΩ	*
High Level	200kΩ	*
External Transformer Options[2]	10kΩ	*
DIGITAL INPUT (TTL COMPATIBLE)	1TTL Load	*
OUTPUT VOLTAGE AND FORMAT		
With Internal Transformers		
Low Level	11.8V rms Line-to-Line Synchro or Resolver	*
High Level	90V rms Line-to-Line Synchro or Resolver	*
External Transformer Options[3]	7V rms Sine and Cosine	*
LOAD CAPABILITY	1.3VA	*
SHORT CIRCUIT PROTECTION	Continuous for 5 minutes	*
OUTPUT SETTLING TIME[4]	50μs for 180° Step	*
RADIUS VECTOR VARIATION (Transformation Ratio)	±0.1% max Sine and Cosine	*
INTERNAL TRANSFORMER ISOLATION	500V dc	*
POWER SUPPLIES		
Voltage	±15V dc ±5%	*
Current		
(a) No Load	95mA per Line	*
(b) Full Load Mean	225mA per Line	*
WARM-UP TIME	1sec to Full Accuracy	*
OPERATING TEMPERATURE RANGE	0 to +70°C Standard	*
	-55°C to +105°C Extended	*
STORAGE TEMPERATURE RANGE	-55°C to +125°C	*
SIZE	3.125" x 2.625" x 0.8"	*
	(79.4mm x 66.7mm x 20.3mm)	*
WEIGHT	8 ounces (224 grams) max	*
MEAN TIME BETWEEN FAILURES (MTBF) CALCULATED[5]	150,000 Hours	*

NOTES

*Specifications same as DSC1705.

[1] Accuracy applies over the full operating temperature range of the option and for:
- (a) ±10% reference frequency and amplitude variation.
- (b) 10% harmonic distortion on the reference.
- (c) ±5% power supply variation.
- (d) Any balanced load from no load to full load.

[2] Refers to input to converter and not to external transformers.

[3] Refers to output from internal converter amplifiers and not from external transformers.

[4] Dependent upon option and load conditions.

[5] With MIL-STD-883B components.

Specifications subject to change without notice.

CONNECTING THE CONVERTER

400Hz options. All these converters contain internal output and reference transformers.

The digital input should be connected to pins "1" through "12" on the DSC1706 and pins "1" through "14" on the DSC1705, noting that pin "1" is the Most Significant Bit (MSB).

"S1", "S2" and "S3" should be connected to the appropriate inputs on the synchro being driven. ("S4" is used also when connection is made to a resolver).

The reference should be connected to "R_{Hi}" and "R_{Lo}" ensuring that the phase is correct.

"GND" is the common for both power supplies and digital inputs.

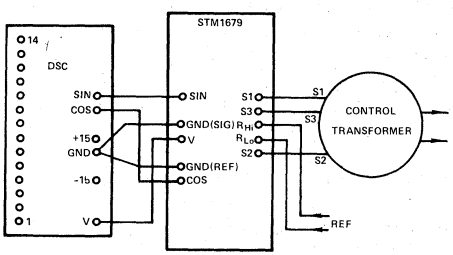
60Hz Options. For 60Hz operation, an external transformer, STM1679 is required.

The power supplies and digital input should be connected as for the 400Hz version.

The STM1679 transformer should have its pins "SIN", "COS" and "V" connected to the equivalent pins on the converter. The "GND(SIG)" and "GND(REF)" should both be connected to "GND" on the converter.

The outputs to the load should be taken from "S1", "S2" and "S3" on the STM1679 transformer ("S4" also in the case of a resolver).

The reference input should be made to "R_{Hi}" and "R_{Lo}" on the STM1679.



60Hz Connection to a Control Transformer (Diagram Shows Bottom View of Modules)

OPERATION WITH EXTERNAL AMPLIFIERS OR TRANSFORMER OTHER THAN STM1679

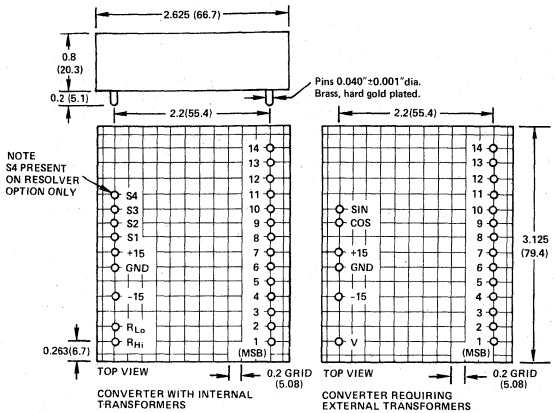
For certain applications, the power output required by the load will be greater than the 1.3VA supplied by the internal amplifiers. Thus external amplifiers and transformers will be needed. Products offered to fulfull this requirement are:

SPA1695 – Dual 5VA Amplifier
STM1696 – 5VA output and reference transformers (400Hz)
STM1697 – 5VA output and reference transformers (60Hz)

If you have a requirement for such products please request the data sheet.

CONVERTER OUTLINE DIMENSIONS AND PIN CONNECTION DIAGRAM

Dimensions shown in inches and (mm).

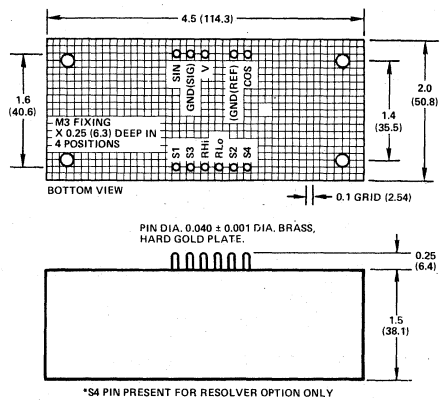


NOTE
DIAGRAMS ABOVE SHOW DSC1705.
DSC1706 DOES NOT HAVE PINS "13" AND "14".

MATING SOCKET: CAMBION 450-3388-01-03

TRANSFORMER (STM1679) OUTLINE DIMENSIONS AND PIN CONNECTION DIAGRAM

Dimensions shown in inches and (mm).



BIT WEIGHT TABLE

Bit Number	Weight in Degrees
1 (MSB)	180.0000
2	90.0000
3	45.0000
4	22.5000
5	11.2500
6	5.6250
7	2.8125
8	1.4063
9	0.7031
10	0.3516
11	0.1758
12 (LSB for DSC1706)	0.0879
13	0.0439
14 (LSB for DSC1705)	0.0220

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LOADING THE DSC's WITH CONTROL TRANSFORMERS (CT's)

The most common device to be driven by Digital to Synchro converters is the control transformer (CT)

The minimum power required to drive a CT can be expressed as:

$$(VA) = \frac{V^2}{|Z_{so}|} \cdot \frac{3}{4}$$

where V is the line to line voltage and Z_{so} is the impedance between one input terminal and the other two shorted together with the rotor open circuit. ($Z_{so} = R_{so} + j\,X_{so}$)

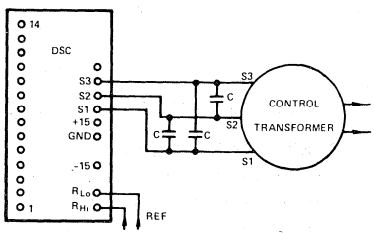
For example, if a CT has a Z_{so} of 700 + j 4900 and a line to line voltage of 90 volts, then:

$$|Z_{so}| = \sqrt{700^2 + 4900^2} = 4950 \text{ Ohms}$$

$$\text{and } (VA) = \frac{90^2}{4950} \cdot \frac{3}{4} = 1.23VA$$

TUNING CT LOADS

The load can be reduced by tuning the output with 3 capacitors as shown below.



Capacitor Connection for Tuning CT's

C should be equal to:

$$\frac{X_{so}}{2\omega\,(R_{so}^2 + X_{so}^2)}$$

The power required after tuning will be:

$$(VA) \text{ untuned} \times \frac{R_{so}}{Z_{so}}$$

Therefore in the above example the capacitor value should be:

$$\frac{4900}{2 \times 2\pi \times 400\,(245 \times 10^5)} = 40nF$$

and the power required after tuning will be:

$$1.23 \times \frac{700}{4950} = 0.17VA$$

Note allowance should always be made for tolerances in the CT windings, capacitors and frequency.

PRACTICAL CONSIDERATIONS OF TUNING CT LOADS

1. The capacitors used need not be of high tolerance, 20% is sufficient.
2. Three capacitors must be used, one across S1 and S2, one across S1 and S3 and one across S2 and S3.
3. Voltage working and type of capacitors should be as follows:

   11.8V Line-to-Line options:
   15 Volt ac working or greater, non-polarized tantalum type.

   90V Line-to-Line options:
   100 Volt ac working or greater, for example, low K ceramic types.
4. For tuning Resolver loads, two capacitors only are required, one connected between S1 and S3 and the other connected between S2 and S4.

CONTROL DIFFERENTIAL TRANSMITTERS (CDX's)

The loading on a DSC of these devices can be considered in a similar way to that of CT's. However becasue a CT normally follows a CDX, the effective Z will need to be calculated. This value will normally be between 66% and 80% of the Z_{so} quoted for the CDX.

TORQUE RECEIVERS (TR's)

Torque receivers are more difficult devices to drive than CT's and CDX's, and in general external amplifiers and transformers will be necessary. However, because of the lack of radius vector variation, the DSC1705 and DSC1706 are far more suited to driving TR's than converters with a variation of ±7%.

For a deviation of an angle θ, the drive current required will be:

$$\frac{2 \cdot V \cdot \sin\frac{\theta}{2}}{|Z_{ss}|}$$

Points to be observed are:

(a) The TR should not be allowed to lock up.
(b) A phase lead equal to that specified for the TR should be introduced into the reference input to the DSC.
(c) The reference should always be present on the TR and the converter.
(d) The DSC output voltage should be matched exactly to the voltage requirements of the TR.

CAUTIONS

(a) Do not connect a 115V reference to a 26V converter.
(b) Do not reverse the power supplies.
(c) Do not connect the reference to any other pins except "R_{Hi}" and "R_{Lo}".

ORDERING INFORMATION

When ordering, the converter part numbers should be suffixed by an option code in order to fully define the item. All standard options and their appropriate option codes are listed below.

Part Number[1]	Resolution	Operating Temp. Range	Line-to-Line Output Voltage and Format	Reference Voltage	Reference Frequency
DSC1705511	14 Bits	0 to +70°C	11.8V Synchro	26V	400Hz
DSC1705512	14 Bits	0 to +70°C	90.0V Synchro	115V	400Hz
DSC1705611	14 Bits	-55°C to +105°C	11.8V Synchro	26V	400Hz
DSC1705612	14 Bits	-55°C to +105°C	90.0V Synchro	115V	400Hz
DRC1705518	14 Bits	0 to +70°C	11.8V Resolver	26V	400Hz
DRC1705618	14 Bits	-55°C to +105°C	11.8V Resolver	26V	400Hz
DSC1705507 and STM1679522	14 Bits	0 to +70°C	90.0V Synchro	115V	60Hz
DSC1705607 and STM1679622	14 Bits	-55°C to +105°C	90.0V Synchro	115V	60Hz

Note: 1. For 12-bit resolution, substitute DSC1706 in place of DSC1705 in the above.
2. For options not shown above, consult the factory.

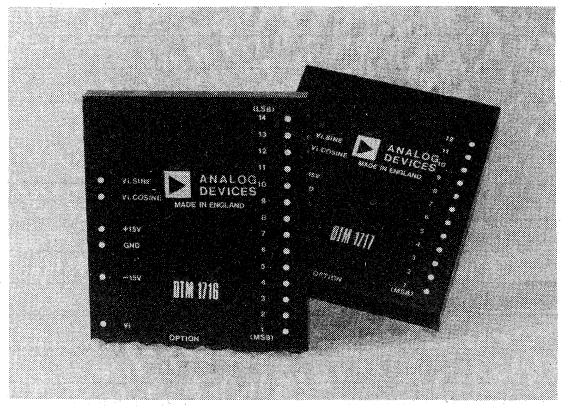
ANALOG DEVICES

Digital Vector Generator

DTM 1716/1717 SERIES

FEATURES
- **Accurate Sine, Cosine Multiplication**
- **14-Bit Resolution**
- **3 Arc-Minutes Accuracy**
- **0.1% Radius Accuracy**
- **Low Profile (0.4")**
- **Maximum Frequency to Full Accuracy 2.5kHz**
- **Low Feedthrough**

APPLICATIONS
- **Digital to Synchro Conversion**
- **Displays**
- **Axis Rotation**
- **Simulators**
- **Numerical Control**
- **Prediction**
- **Vector Resolution**
- **Spectrum Analysis**
- **Ultra Low Frequency Oscillators**



GENERAL DESCRIPTION

The DTM1716 and DTM1717 are computing converters which have a digital angle input in natural binary form and a bipolar analog input $V_i(t)$. There are two analog outputs $V_{01}(t)$ and $V_{02}(t)$, the outputs are related to the inputs by;

$$V_{01}(t) = V_i(t) \sin \phi(t) \qquad V_{02}(t) = V_i(t) \cos \phi(t)$$

where ϕ is the digital angular input. ϕ ranges from 0 to 360°. The analog input has a range of ±10V; the analog output has a range of ±10V.

The digital input has a resolution of 14 bits for the DTM1716 and 12 bits for the DTM1717. The modules are powered from ±15V supply lines.

If the output voltages are regarded as the components of a vector, the radius accuracy is better than 0.1% and the angular inaccuracy is less than 3 arc minutes for the DTM1716.

A block diagram of the DTM1716 is shown in Figure 1.

Particular attention has been paid in the design to achieve high accuracy in the sine and cosine generation so that they may be used separately as accurate functions.

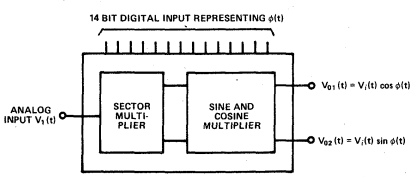


Figure 1. Diagram of DTM 1716

Two models are available each with two options as shown below.

DTM1716500 has 14-bit digital input resolution and a 0 to +70°C operating temperature range.

DTM1716600 has 14-bit digital input resolution and a -55°C to +105°C operating temperature range.

DTM1717500 has a 12-bit digital input resolution and a 0 to +70°C operating temperature range.

DTM1717600 has a 12-bit digital input resolution and -55°C to +105°C operating temperature range.

OPERATION

The operation of the DTM1716 is straightforward, being powered from ±15V lines relative to the common pin. No damage is caused by either the +15V or -15V being disconnected but they must not be reversed. The analog input is protected against a short circuit to either power line. The output is short circuit proof and can be connected to either power line without damage. The digital inputs are standard TTL levels. The module dimensions and pin out are shown in Figure 2.

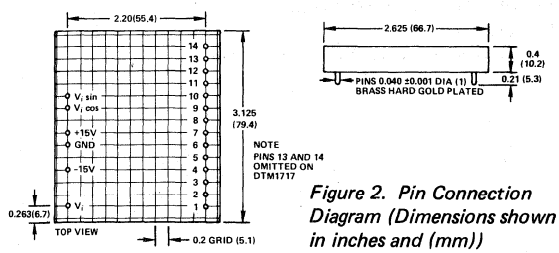


Figure 2. Pin Connection Diagram (Dimensions shown in inches and (mm))

MATING SOCKET: CAMBION 450-3388-01-03

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SPECIFICATIONS (typical @ +25°C unless otherwise noted)

MODELS	DTM1716	DTM1717
DIGITAL ANGULAR RESOLUTION	14 bits (1 LSB = 1.3 arc-mins)	12 bits (1 LSB = 5.3 arc-mins)
FULL SCALE OUTPUT	±10V	*
SCALING ACCURACY	0.1% FSR	*
FULL SCALE INPUT	±10V	*
SCALE TEMPCO	25ppm/°C of FSR	*
ZERO OFFSET	2.5mV	*
OFFSET DRIFT	50μV/°C	*
AC ACCURACY Analog Step Response (10V Step)	 40μs (to 0.1%)	 *
MAX SLEW RATE	0.5V/μs	*
FULL POWER OUTPUT	8kHz	*
FEEDTHROUGH	<1mV at 400Hz	*
ANALOG INPUT IMPEDANCE	10kΩ	*
ANALOG OUTPUT IMPEDANCE	100mΩ	*
OUTPUT LOAD	2kΩ	*
OUTPUT PROTECTION	Short circuit proof	*
DIGITAL INPUT	14-bit natural parallel binary, 1TTL Load	12-bit natural parallel binary, 1TTL Load
RESPONSE TO DIGITAL STEP (90°) (FS Analog Input)	40μs to 0.1% of final value	*
VECTOR ACCURACY[1] Radius Error Angular Error	 0.1% FSR ±3 arc-mins	 * *
POWER SUPPLY REJECTION	80dB	*
POWER SUPPLIES	+15V @ 50mA max -15V @ 40mA max	* *
TEMPERATURE RANGE Operating Storage	0 to +70°C Standard or -55°C to +105°C extended -55°C to +125°C	* * *
DIMENSIONS	3.125 x 2.625 x 0.4" 79.4 x 66.7 x 10.2mm	*
WEIGHT	3 oz (85 grams)	*

NOTES

*Specification same as DTM1716.

[1] See Figure 4.

Specifications subject to change without notice.

APPLICATIONS OF THE DTM1716

Figure 3 shows how the DTM1716 can be used in radars and radar simulators for modulating display sawtooth generators using signals derived from a synchro transmitter on the antenna and a Synchro to Digital converter. The synchro signal representing the antenna angle is converted to a 14-bit natural binary representation by the Synchro to Digital converter SDC1704. The digital angle is applied to the digital input of the DTM1716. A dc voltage is applied to the DTM1716 analog input which controls the radius of the displayed raster. The output voltages are used to provide the X and Y time base currents. The switches across the capacitors are opened on the leading edge of the transmission pulse and closed after a time interval determined by the range.

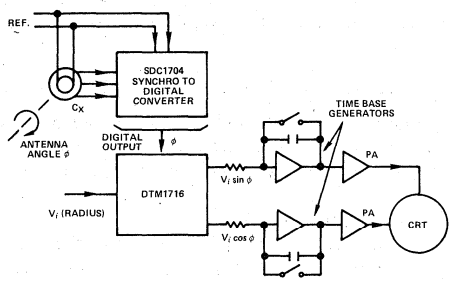


Figure 3. PPI Waveform Generation Using the DTM1716

AXIS ROTATION

Figure 4 shows how two DTM1716's may be used to compute the new two dimensional coordinates of a point relative to a rotated set of axes. The input voltage X_1 and Y_1 are proportional to the coordinates of a point in the XY plane. If a digital angle ϕ is applied to the DTM1716's, the output voltages X_2 and Y_2 correspond to the X and Y coordinates of the point relative to a set of axes rotated through the angle ϕ. The systems can be extended to three dimensions.

The arrangement as shown in Figure 4 may also be used to obtain the new coordinates of a point which is rotated through the angle in the same coordinate set. This scheme provides a low cost, accurate and compact solution to transformation problems.

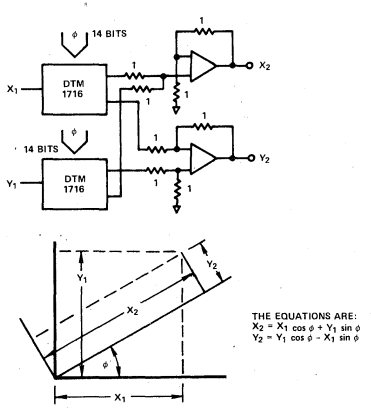


Figure 4. Axis Rotation in Two Dimensions Using the DTM1716

SYNCHRO TO INVARIANT SINE/COSINE

In many engineering applications it is required to obtain voltages proportional to the sine and cosine of an angular movement and to be able to scale the voltages electrically. Figure 5 shows how a Synchro to Digital converter and the DTM1716 may be used for this purpose. The advantage of this scheme is that the coefficients of sine and cosine are electrically scalable by means of the bipolar voltage V_i, saving memory space, multipliers, power and space.

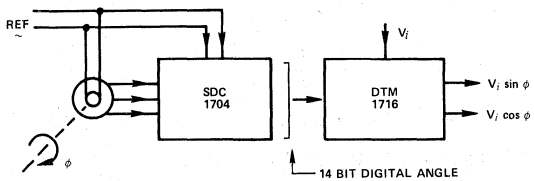


Figure 5. Synchro to Invariant Sine/Cosine Using the SDC1704 and DTM1716

POWER SPECTRUM ANALYSIS

Figure 6 shows a less usual application of the DTM1716 in the spectrum analysis of low frequency signals. This has the advantage of providing almost infinite resolution at extremely low relative cost.

A simple method of obtaining the power in the frequency interval $f \pm \Delta f$ is shown in Figure 6.

The input waveform from which the power spectrum is required is g(t). Multiplication of this waveform by Sin $2\pi ft$ causes the energy in the waveform between $f - \Delta f$ and $f + \Delta f$ to be shifted to lie between $-\Delta f$ and $f + \Delta f$. The low pass filter passes this voltage waveform to the square law devices to produce an output proportional to the power. Two channels, sine and cosine, are used for the case where g(t) may contain a periodic component. If for example there is a line in the power spectrum, without the use of the two channels the output at that frequency would depend upon its phase. The use of both sine and cosine multiplication avoids this problem.

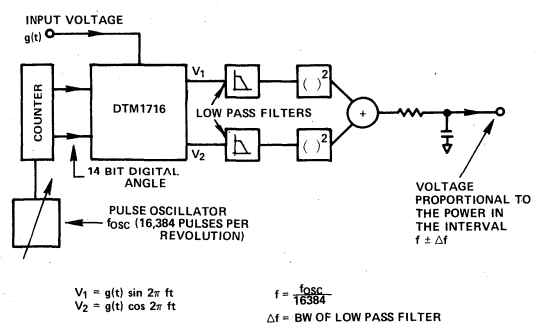


Figure 6. The Use of the DTM1716 to Obtain the Power Frequency Spectrum of g(t)

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PHASE MODULATION

The DTM1717 can be used for low frequency phase modulation of subcarriers. Figure 7 shows the method which uses two DTM1717's and an ADC. Frequency modulation can be obtained if the amplitude of the signal is made to be inversely proportional to its frequency. This can be accomplished by inserting an integrator in series with the modulation input. Similar techniques can be used for very low frequency synthesis.

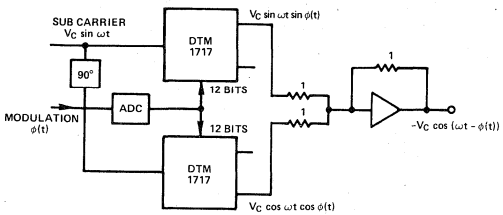


Figure 7. Phase Modulation Using 2 DTM1717's

ORDERING INFORMATION

There are only two options for each of the DTM1716 and DTM1717. They are the commercial or extended temperature ranges. The appropriate designations are as follows:

DTM1716500 (14 bits) 0 to +70°C
DTM1716600 (14 bits) -55°C to +105°C
DTM1717500 (12 bits) 0 to +70°C
DTM1717600 (12 bits) -55°C to +105°C

OTHER PRODUCTS

Many modules concerned with the conversion of synchro data are manufactured by us, some of which are listed below. If you have any questions about our products or require advice about their use for a particular application, please contact our Applications Engineering Department.

SYNCHRO TO DIGITAL CONVERTERS

The SDC1700 is a low profile (0.4″) converter with a 12-bit natural binary output. Its overall accuracy is ±8.5 arc-minutes, and the module contains internal transformers for all reference frequency options including 60Hz.

The SDC1702 is similar to the new SDC1700 but has a 10-bit natural binary output and an overall accuracy of +22 arc-minutes.

The SDC1704 is similar to the above two converters, but has a 14-bit natural binary output and an overall accuracy of ±2.0 arc-minutes ±1LSB.

The SBCD1752/1753/1756 and 1757 are Synchro to Digital converters based on the SDC1700 which give an output in BCD format.

DIGITAL TO SYNCHRO CONVERTERS

Resolutions of between 10 and 14 bits are available as well as the DSC1710 which is a one card, 1 channel, two speed DSC system containing its own 20VA power amplifiers.

TWO SPEED PROCESSORS

The TSL1612 combines the digital outputs of the two Synchro to Digital converters in a two speed system in order to produce a single digital word representing the input angle. It is available for any ratio between 2:1 and 36:1.

12-Bit, Tracking Inductosyn™/ Resolver to Digital Converter

IRDC 1730

FEATURES
- Uses Ratiometric Amplitude Measurement Principle
- Can Be Used with Inductosyns or Resolvers
- 12-Bit Parallel Word Representing Resolver Shaft Angle or Distance Moved Through Inductosyn Pitch
- Tracking Rates at Up to 170 revs/sec (10,200 rpm) or 170 Pitches Per Second
- Transformer Isolated Inputs
- Resistive Scaling Facility Accommodates Most Resolver Signal Levels
- Direction Output
- Ripple Clock Output (Revolution or Pitch Count)
- DC Velocity Output Representing Input Rate
- No External Trims or Adjustments
- Four Frequency Options (400Hz, 2.6kHz, 5kHz or 10kHz)
- Low Profile Module (0.4", 10.2mm)
- Designed to Meet Intrinsic Safety Requirements

APPLICATIONS
- Industrial Control
- Machine Tool and Robot Control

GENERAL DESCRIPTION

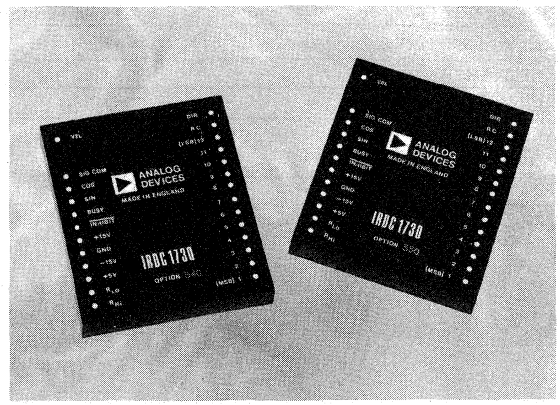
The IRDC1730 converts resolver format (sine and cosine) signals into a 12-bit parallel word. The unit accepts inputs from either a resolver, in which case the 12-bit word represents the angle of the resolver shaft or from an Inductosyn slider via external pre-amps in which case the 12-bit word represents the distance moved through an Inductosyn pitch.

The converter is of the continuous tracking type working on a type 2 servo loop principle and operates for input rates of up to 170 revs per second (in the case of the 5kHz and 10kHz versions). In the case of an Inductosyn input used at these frequencies, it will track at a maximum rate of 170 pitches per second.

The converters are available in 4 different frequency options, 400Hz, 2.6kHz, 5kHz and 10kHz; and the signal and reference inputs, which are transformer isolated, are accepted as 2.5 volts rms max. *An outstanding feature of the converter is that even though the signal and reference inputs are transformer isolated, they can still be externally resistively scaled to accommodate the user's particular voltage levels.*

A further advantage of the IRDC1730 is that it works on a ratiometric, amplitude comparison principle and therefore any voltage drop between the resolver or the Inductosyn and the converter does not substantially affect the accuracy. The amplitude measurement technique also ensures a high degree of noise immunity which might exist on the signal input lines.

Inductosyn is a trademark of Farrand Industries Inc.



In addition to the digital output, the IRDC1730 also provides a dc velocity signal which is proportional to the rate at which the input is changing.

A direction signal is also provided as well as a ripple clock output which gives a pulse every time the resolver input passes through the zero position or the Inductosyn slider moves to an adjacent pitch (see timing diagram).

The IRDC1730 is housed in a 0.4" (10.2mm) low profile module and weighs only 3.5 ozs (100G).

MODELS AVAILABLE

The IRDC1730 is available in two operating temperature versions each one of which is available in four frequency options. For details of how to specify an exact part number see "Ordering Information".

OPERATION OF THE CONVERTER

The IRDC1730 is a tracking converter. This means that the output always automatically follows the input for speeds up to the maximum specified tracking rate of the particular option. There is no requirement for "Convert Command" signals. One full revolution of the resolver or the movement of the slider through a distance equivalent to one pitch of the Inductosyn will cause the output of the converter to change from an output of all "zeroes" through to an output of all "ones" or vice versa. As the output of the converter passes through electrical zero of the resolver or the Inductosyn, a pulse will be output on the Ripple Clock (RC) pin. The direction of rotation is indicated by the DIR signal.

SPECIFICATIONS (typical @ +25°C unless otherwise stated)

Model	IRDC1730
ACCURACY[1]	±8 arc-minutes Static Input (see tracking rate specification)
RESOLUTION	12 Bits (LSB = 5.27 arc-minutes or 1/4096 of a pitch)
DIGITAL OUTPUT	Parallel, 2TTL Loads, MSB = 180° or half pitch posn.
SIGNAL AND REFERENCE FREQUENCY[1]	400Hz, 2.6kHz, 5kHz or 10kHz
SIGNAL VOLTAGE[1]	2.5 volts max (Sine and Cosine) rms
SIGNAL IMPEDANCE	5.6kΩ
REFERENCE VOLTAGE[1]	2.5 volts rms
REFERENCE IMPEDANCE	5.6kΩ
ALLOWABLE PHASE SHIFT[2] (Signal to reference)	±20° will give no additional error with a static input
TRANSFORMER ISOLATION	500 volts dc
TRACKING RATE (min, i.e., at least)	For ±14 arc-minutes Accuracy: 68 rps (400Hz) 87 rps (2.6kHz) 170 rps (5kHz, 10kHz) For ±10.5 arc-minutes Accuracy: 34 rps (400Hz) 43 rps (2.6kHz) 85 rps (5kHz, 10kHz)
SETTLING TIME (For 179° Step)	
400Hz Options	38ms
2.6kHz Options	33ms
5/10kHz Options	12ms
ACCELERATION CONSTANT (K_A)	
400Hz Options	88,435/sec^2
2.6kHz Options	469,000/sec^2
5/10kHz Options	1,015,000/sec^2
"BUSY" OUTPUT	Logic "HI" when busy. 350ns max width. 1TTL load.
DIRECTION OUTPUT (DIR)	Logic "LO" when counting up. Logic "HI" when counting down. 2 STTL load (Mil) 4STTL loads (comm). Valid for min of 300ns before and min of 75ns after positive going edge of BUSY.
RIPPLE CLOCK OUTPUT (RC)	Low going pulse indicating when internal counters will change from all "1s" to all '0s" or vice versa. Duration equals BUSY period, between contiguous positive going edges.
INHIBIT INPUT	Logic "LO" to inhibit. 1LS TTL Load.
VELOCITY OUTPUT CHARACTERISTICS:	
Scaling	±5V ±5% dc for max stated tracking rate of option
Polarity	Positive going voltage for increasing angle
Zero Offset	5mV max at +25°C max 10mV max at max specified operating temperature
Gain Temperature Coefficient	0.07%/°C typical, 0.2%/°C max
Linearity	2% over one fifth max tracking rate
Output Noise	Less than 5mV in 0 to 20Hz bandwidth
POWER SUPPLIES	±15 volts @ 13.3mA +5 volts @ 185mA
POWER DISSIPATION	1.33 Watts
TEMPERATURE RANGE	0 to +70°C Standard −55°C to +105°C Extended
DIMENSIONS	2.625" X 3.125" X 0.4" (66.6mm X 79.3mm X 10.2mm)
WEIGHT	3.5 ozs.

NOTES

[1] Accuracy applies over the operating temperature range and over: (a) ±10% signal and reference voltage and frequency variation (b) ±10% signal and reference harmonic distortion (c) ±5% power supply variation.

[2] See "Dynamic Accuracy vs. Resolver Phase Shift".

Specifications subject to change without notice.

CONNECTING THE CONVERTER AND RESISTIVELY SCALING THE INPUTS

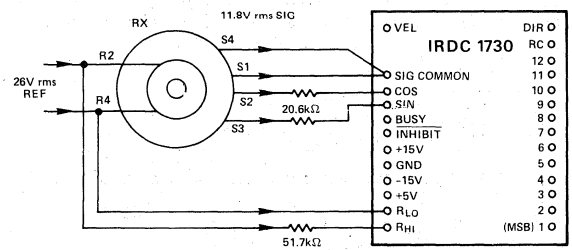
The sine and cosine signal inputs from the resolver or the Inductosyn slider are required to be 2.5V rms at the converter pins (see note 1, Specifications).

The resistive voltage scaling facility enables higher voltages to be interfaced by the simple addition of external scaling series resistors.

In the case of the signal voltages, the resistor value should be 2.22kΩ per extra volt required. The matching of the resistors is more important than the absolute calculated value. A matching of 0.1% between the two resistors will give rise to an additional error of 1.7 arc-minutes or 0.0000787 times the Inductosyn pitch.

The reference input can also be scaled using a resistance of 2.2kΩ per extra volt in the R_{HI} line. The absolute value of this resistor is not critical as long as the voltage appearing on the converter pins is within ±10% of 2.5 volts rms.

An example of resistive scaling is shown below where a resolver with a signal voltage of 11.8 volts rms and a reference voltage of 26 volts rms is being used with the IRDC1730.



Resistive Scaling of a Resolver to the IRDC1730

The electrical connections to the converter are straightforward. The power lines, which must not be reversed, are ±15V and +5V. They must be connected to the "±15V" and "+5V" pins with the common connection to GND. It is suggested that 0.1μF and 6.8μF capacitors be placed in parallel from +15V to GND, from -15V to GND and from +5V to GND.

DYNAMIC ACCURACY VS RESOLVER PHASE SHIFT

Most resolvers, particularly those of the brushless variety, exhibit a phase shift between the signal and the reference. This phase shift will give rise under dynamic conditions to an additional error defined by:

$$\frac{\text{Shaft speed (RPS) X Phase Shift (Degs)}}{\text{Reference Frequency}}$$

For example, for a phase shift of 20°, a shaft rotation of 22 RPS and a reference frequency of 5kHz, the IRDC1730 will exhibit an additional error of:

$$\frac{20 \times 22}{5000} = 0.088^\circ$$

This effect can be eliminated by putting a phase lead in the reference to the converter equivalent to the phase shift in the resolver.

THEORY OF OPERATION

The sine and cosine signals are applied to the signal transformers to produce on the secondary windings the following voltages:

$$V_1 = K\ E_O\ \text{Sin}\ \omega t\ \text{Sin}\ \theta$$
$$V_2 = K\ E_O\ \text{Sin}\ \omega t\ \text{Cos}\ \theta$$

Where θ is the angle of the resolver shaft or the distance moved through a particular pitch of the Inductosyn.

To understand the conversion process, then assume that the current word state of the up-down counter is ϕ.

The V_1 is multiplied by Cos ϕ and V_2 is multiplied by Sin ϕ to give:

$$K\ E_O\ \text{Sin}\ \omega t\ \text{Sin}\ \theta\ \text{Cos}\ \phi$$
and $$K\ E_O\ \text{Sin}\ \omega t\ \text{Cos}\ \theta\ \text{Sin}\ \phi$$

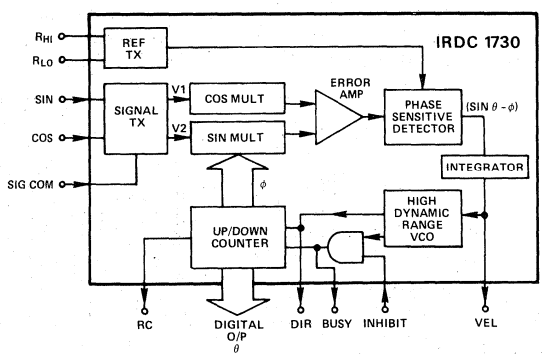
These signals are subtracted by the error amplifier to give:

$$K\ E_O\ \text{Sin}\ \omega t\ (\text{Sin}\ \theta\ \text{Cos}\ \phi - \text{Cos}\ \theta\ \text{Sin}\ \phi)$$
or $$K\ E_O\ \text{Sin}\ \omega t\ \text{Sin}\ (\theta - \phi)$$

A phase sensitive detector, integrator and Voltage Controlled Oscillator (VCO) form a closed loop system which seeks to null Sin $(\theta - \phi)$.

When this is accomplished, the word state of the up-down counter (ϕ), equals within the rated accuracy of the converter, the resolver shaft angle θ.

The Ripple Clock output (RC) is provided from the most significant end of the counter while the direction output (DIR) is taken from the steering logic input to the counter. The BUSY output is derived from the clock used to drive the counter and this can be disabled using the INHIBIT.

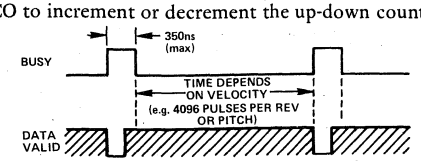


Schematic Diagram of the IRDC1730

DATA TRANSFER

The readiness of the converter for data transfer is indicated by the state of the BUSY pin, (see diagram).

The voltage appearing on the BUSY pin consists of a train of pulses, at TTL levels, when the input to the converter is changing. The converter is busy when the BUSY pin is at a TTL "Hi" level. These pulses correspond to those delivered by the VCO to increment or decrement the up-down counter (see



Data Transfer Diagram (See Also Timing Diagram)

schematic diagram). Thus the pulses will occur for increasing and decreasing counts.

The most suitable time for transferring data is at or following the negative going transition of BUSY.

Taking the INHIBIT to a logic "Lo" state prevents the VCO (BUSY) pulses from updating the up-down counter. However, if applied during a BUSY pulse, the INHIBIT will not become effective until the end of the BUSY pulse.

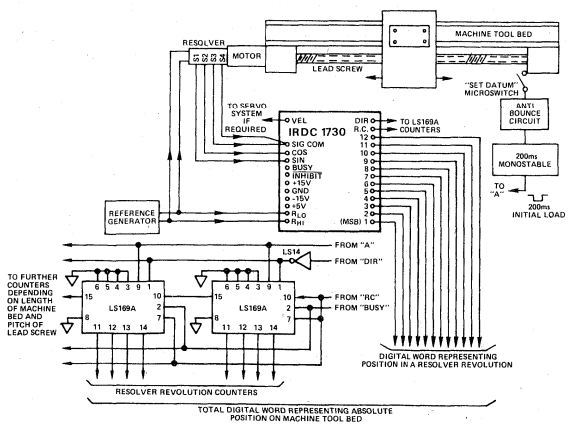
An alternative method of transferring the data is by applying the INHIBIT (taking it to a logic "Lo" state), waiting for at least the width of a BUSY pulse, transferring the data and releasing the INHIBIT.

Note that sustained application of the INHIBIT opens the internal control loop and the converter may take on appreciable time to recover to full accuracy when the loop is restored.

USE OF THE IRDC1730 IN A RESOLVER MACHINE TOOL APPLICATION

In many machine tool applications, a resolver is fitted to the axis lead screw in order to provide a method of measuring linear displacement. The IRDC being a tracking converter with no drift or stale data problems and having a very high maximum tracking rate (over 10,000 rpm in the case of the 5 and 10kHz versions) forms an ideal method of converting the output of the resolver into digital format for use by the controller. The diagram below shows how the resolver may be used in this type of application as well as a method of using external counters to count the number of revolutions of the lead screw and so give an absolute digital representation of the machine axis position.

Note that unlike the phase measuring resolver to digital conversion techniques which require the resolver to be supplied with a very accurate sine and cosine waveform, this method requires that the resolver rotor is energized and the sine and cosine outputs from the stator taken to the converter. *The advantage of this method is that the converter's ratiometric operation does not require a particularly stable voltage or frequency reference to be applied to the resolver rotor.* In addition, any small drops in voltage between the resolver and the converter or any noise induced in the signal lead, will not substantially affect the accuracy.

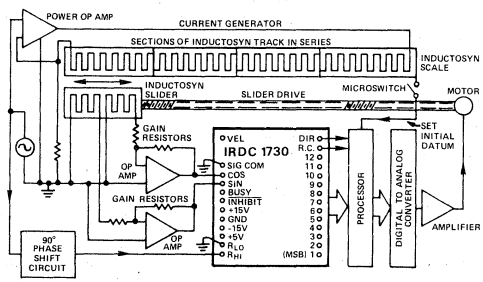


Using the IRDC1730 with a Resolver on a Machine Tool Axis

USE OF THE IRDC1730 WITH AN INDUCTOSYN FOR MEASURING LINEAR OR ROTARY DISPLACEMENT

The IRDC1730 can be used very effectively with an Inductosyn to provide a very accurate linear or rotary measurement system. Inductosyns are normally of 2mm pitch and therefore the resolution obtainable will be in excess 0.5 microns. The use of the IRDC1730 in, for example, a machine axis control system is shown in the diagram below.

The Inductosyn in this case is made to behave like a resolver. The fixed track is driven from an ac current generator at a frequency of 5 or 10kHz, and the resolver format sine and cosine signals are available from the slider. The reason for using a current source is that the track is mainly resistive and it is better to determine the phase by deliberately driving the track from a current source and inserting a 90 degree phase advance into the reference rather than having a less accurately defined phase shift due to the track's X to R ratio.



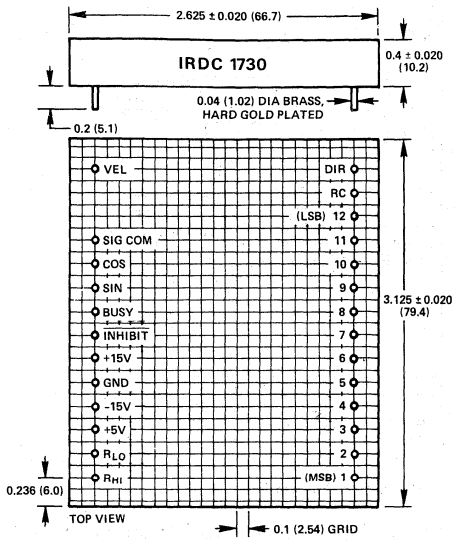
The Use of an Inductosyn/Resolver Converter in an Inductosyn Control Loop

The amplifiers which are necessary between slider and converter need to have equal gains in order to amplify the signals to the 2.5 volts rms required by the converter. (A gain ratio of 1.002 will give rise to an inaccuracy of 1/6000 of a pitch). A typical voltage which might be availabe at the input to the amplifier is 3mV. The amplifiers should be connected as close to the slider as possible with the longer connecting leads being at the high voltage level. The low output impedance of the amplifiers will then drive the cable.

The "Set Datum" circuitry shown in the diagram is identical to that used for the resolver application, the only provision being that the microswitch always operates within the same pitch of the Inductosyn.

CONVERTER OUTLINE DIMENSIONS AND PIN CONNECTION DIAGRAM

Dimensions shown in inches and (mm).



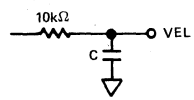
Individual Mating Sockets: Cambion 450-3388-03-01

BIT WEIGHT TABLE

Bit Number	Weight in Degrees
1 (MSB)	180.0000
2	90.0000
3	45.0000
4	22.5000
5	11.2500
6	5.6250
7	2.8125
8	1.4063
9	0.7031
10	0.3516
11	0.1758
12 (LSB)	0.0879

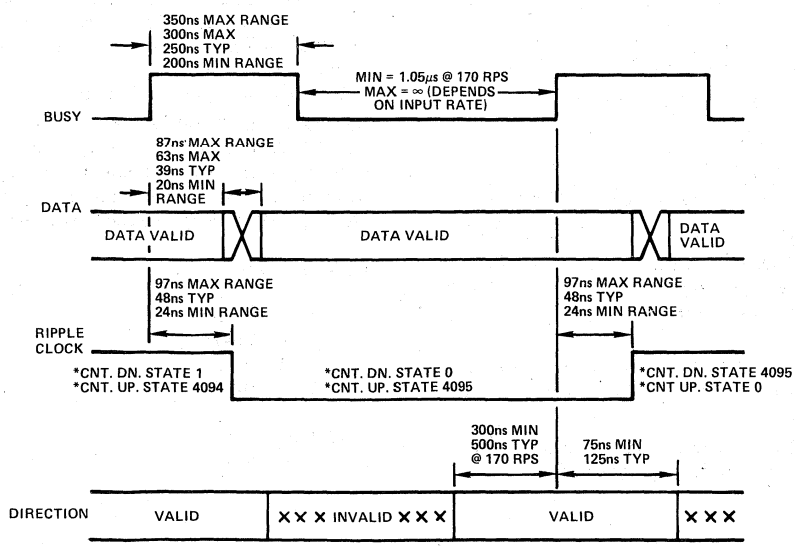
VELOCITY OUTPUT FILTER

The velocity output of the IRDC1730 is internally filtered as shown below.



c = 100nF (400Hz options)
c = 22nF (2.6kHz options)
c = 15nF (5 and 10kHz options)

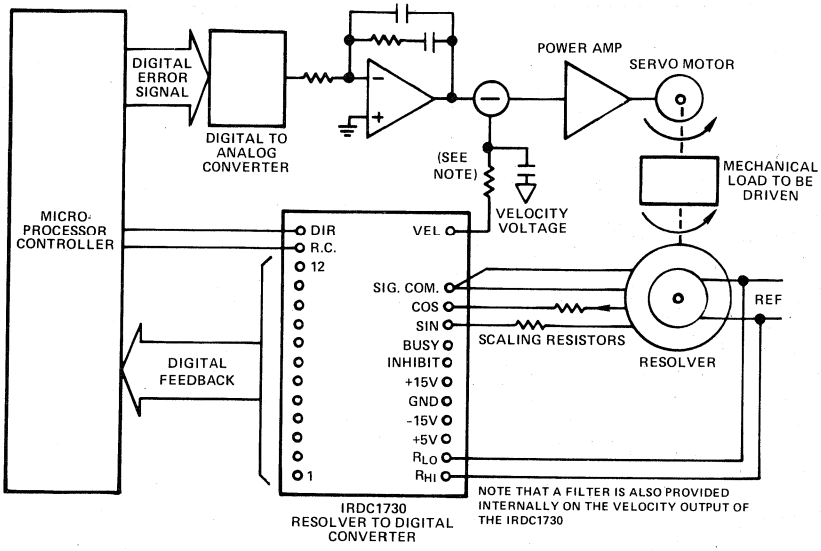
TIMING DIAGRAM



*CNT DN. SHOWS STATE OF DATA OUTPUT WHEN COUNTING DOWN.
*CNT. UP. SHOWS STATE OF DATA OUTPUT WHEN COUNTING UP.

USE OF THE IRDC1730 VELOCITY OUTPUT VOLTAGE

The diagram below shows the use of the velocity output voltage of the IRDC1730 in a servo system.



Practical control using the IRDC1730 as a virtual tachometer

TRANSFER FUNCTIONS

The transfer functions of the various options of the IRDC1730 is as shown below.

400Hz Options

$$\frac{\theta_0}{\theta_1} = \frac{4.815 \times 10^5 s + 9.331 \times 10^7}{s^3 + 1.055 \times 10^3 s^2 + 4.815 \times 10^5 s + 9.331 \times 10^7}$$

2.6kHz Options

$$\frac{\theta_0}{\theta_1} = \frac{2.745 \times 10^6 s + 1.935 \times 10^9}{s^3 + 4.125 \times 10^3 s^2 + 2.745 \times 10^6 s + 1.935 \times 10^9}$$

5kHz and 10kHz Options

$$\frac{\theta_0}{\theta_1} = \frac{5.909 \times 10^6 s + 3.908 \times 10^9}{s^3 + 3.85 \times 10^3 s^2 + 5.909 \times 10^6 s + 3.908 \times 10^9}$$

OTHER PRODUCTS

In addition to the IRDC1730, we also manufacture a very comprehensive range of products which are concerned with the conversion of synchro and resolver information into digital format.

Of particular note is the IRDC1731 which accepts similar inputs to the IRDC1730 but provides a 4000 count serial output. Also we manufacture:

SDC1740/41/42 14- and 12-bit hybrid synchro/resolver to digital converters with *internal transformers.*
SDC1702, 1700 and 1704 10-, 12- and 14-bit synchro/resolver to digital converters.
SDC1725 and 1726 12- and 10-bit synchro/resolver to digital converters with latched three-state outputs.
SDC1721 16-bit synchro/resolver to digital converter.
DTM1716 and 1717 digital vector generators.
DSC1705 and 1706 14- and 12-bit digital to synchro/resolver converters with low radius vector variation.
DDU1714 solid state dummy director with synchro, resolver or digital outputs.
API1620 angle position indicator.

ORDERING INFORMATION

The IRDC1730 part number is suffixed with an X and a Y code to denote operating temperature range and reference frequency as follows. (Note that the Z code used in our other products to denote voltage is left as a zero in this product).

IRDC1730/XY0

Y = 1 400Hz
Y = 4 2.6kHz
Y = 5 5kHz
Y = 6 10kHz

X = 5 0 to +70°C
X = 6 -55°C to +105°C

4000 Count, Tracking Inductosyn™/ Resolver to Digital Converter

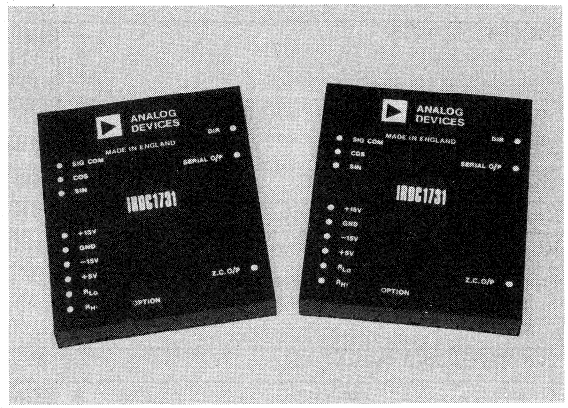
IRDC 1731

FEATURES

- Works on Amplitude Measurement Technique
- Can Be Used with Inductosyns or Resolvers
- 4000 Count Serial Output per Revolution or Pitch
- Transformer Isolated Inputs
- 100 revs/sec (pitches/sec) Tracking Rate
- Resistive Scaling Facility Accommodates Most Signal Levels
- Direction Output
- Zero Crossing Output (Pitch or Revolution Counter)
- No External Trims or Adjustments
- Low Profile 0.4" (10.2mm)

APPLICATIONS

- Digital Display of Inductosyn or Resolver Information in Robotics or Machine Tool Axis Measurement



GENERAL DESCRIPTION

The IRDC1731 converts resolver format (sine and cosine) signals into a 4000 count serial output. The unit accepts inputs from either a resolver, in which case the 4000 counts represent 1 revolution of the shaft or from an Inductosyn slider via external pre-amps in which case the 4000 counts represent a distance corresponding to 1 pitch of the Inductosyn track.

The converter is of the continuous tracking type working on a type 2 servo loop principle and operates for input rates of up to 100 revolutions per second in the case of the resolver and 100 pitches per second in the case of the Inductosyn. *The continuous tracking principle gives the advantages of zero drift and instantly available, nonstale data.*

The converter operates on a 5kHz reference frequency and the inputs, which are transformer isolated, are accepted as 2.5 volts rms max.

An outstanding feature of the converter is that even though the signal and reference inputs are transformer isolated, they can be externally resistively scaled to accommodate the user's particular voltage levels.

A further advantage of the IRDC1731 is that it works on a ratiometric, amplitude comparison principle and therefore any voltage drops between the resolver or the Inductosyn and the converter does not substantially affect the accuracy. The amplitude measurement technique also ensures a high degree of immunity to noise which may exist on the signal input lines.

Inductosyn is a trademark of Farrand Industries Inc.

In addition to the serial output, a direction signal is provided as well as a Zero Crossing signal which gives a pulse every time the resolver input passes through the zero position or the Inductosyn slider moves to an adjacent pitch.

The IRDC1731 is housed in a 0.4" (10.2mm) low profile module and weights only 3.5 ozs. (100 G).

MODELS AVAILABLE

Two models of the IRDC1731 are available, viz:

Model IRDC1731550 which operates over a 0 to +70°C temperature range. (Commercial temperature option).

Model IRDC1731650 which operates over a -55°C to +105°C temperature range. (Extended temperature option).

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SPECIFICATIONS (typical @ +25°C unless otherwise stated)

Model	IRDC1731
ACCURACY[1]	±2 counts (static input) ±3 counts (50 pitches or revs/sec input) ±4 counts (100 pitches or revs/sec input)
RESOLUTION	4000 counts equals one revolution of resolver or one pitch of the Inductosyn
DIGITAL OUTPUT	Serial, negative going pulses, width 1.0 ±0.5μs 4 TTL loads – commercial temperature options 2 TTL loads – extended temperature options
SIGNAL AND REFERENCE FREQUENCY	5kHz
SIGNAL INPUT VOLTAGE[1]	2.5 volts rms
SIGNAL INPUT IMPEDANCE	5.6kΩ
REFERENCE INPUT VOLTAGE[1]	2.5 volts rms
REFERENCE INPUT IMPEDANCE	5.6kΩ
PHASE SHIFT (Signal to Reference) (See 'Dynamic Accuracy vs. Resolver Phase Shift')	±20° will give no additional error with a static input
TRANSFORMER ISOLATION	500 volts dc
TRACKING RATE (Minimum)	100revs/sec (Resolver input) 100 pitches/sec (Inductosyn input)
STEP RESPONSE (179° Step)	80ms max for ±1 count additional error
ACCELERATION Constant K_a	 650,000/sec^2
DIRECTION OUTPUT (DIR)	Logic "Lo" when counting up. Logic "Hi" when counting down. Direction output level changes at least 0.25μs before serial output pulse. 4 TTL loads – commercial temperature options 2 TTL loads – extended temperature options
ZERO CROSSING OUTPUT (Z.C. O/P)	Positive going pulse, 1.0 ±0.5μs in width produced when resolver input passes through zero position or Inductosyn slider moves to adjacent pitch. 4 TTL loads – commercial temperature options 2 TTL loads – extended temperature options
POWER SUPPLIES[1]	+15V dc @ 35mA max -15V dc @ 35mA max +5V dc @ 170mA max
POWER DISSIPATION	1.90 watts max
OPERATING TEMPERATURE RANGE Commercial Extended	 0 to +70°C -55°C to +105°C
STORAGE TEMPERATURE RANGE	-55°C to +125°C
DIMENSIONS	2.625" X 3.125" X 0.4" (66.7mm X 79.4mm X 10.2mm)
WEIGHT	3.5 ozs. (100 G)

NOTES

[1] Accuracy applies over the appropriate operating temperature range and:

(a) ±10% signal and reference voltage amplitude variation.
(b) ±10% signal and reference harmonic distortion.
(c) ±10% variation in reference frequency.
(d) ±5% power supply variation.

Specifications subject to change without notice.

OPERATION OF THE CONVERTER

The IRDC1731 is a tracking converter meaning that the output automatically follows the input up to a rate of 100 revs. or pitches per second without the need for any convert command signal. 4000 negative going pulses are output for each full revolution or pitch and a TTL direction output (DIR) indicates the direction of motion.

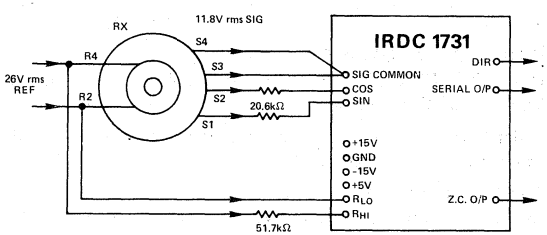
CONNECTING THE CONVERTER AND RESISTIVELY SCALING THE INPUTS

The sine and cosine signal inputs from the resolver or Inductosyn and the reference input are required to be 2.5 volts rms. The voltage scaling facility enables higher voltages to be interfaced by the simple addition of external series scaling resistors.

In the case of the signal voltages, the resistors should be 2.22kΩ per extra volt required. The matching of the resistors is more important than the absolute calculated value. A matching of 0.1% between the two resistors will give rise to an additional error of ±0.31 counts.

The reference input can be scaled resistively also using a resistance of 2.2kΩ per extra volt in the R_{HI} line. The absolute accuracy of this resistor value is not critical as long as the voltage appearing on the converter pins is within the tolerance specified for the 2.5 volt rms reference input.

An example of resistive scaling is shown below where a resolver with a signal voltage of 11.8 volts rms and a reference voltage of 26 volts rms is being used with the IRDC1731.



The electrical connections to the converter are straightforward. The power lines, which must not be reversed, are ±15V and +5V. They must be connected to the "±15V" and "+5V" pins with the common connection to the ground pin GND.

It is suggested that 0.1μF and 6.8μF capacitors be placed in parallel from +15V to GND, from -15V to GND and from +5V to GND.

USE OF THE IRDC1731 IN A RESOLVER MACHINE TOOL APPLICATION

In many machine tool applications, a resolver is fitted to the axis lead screw in order to provide a method of measuring linear displacement. The IRDC1731, being a tracking converter and having no drift or stale data problems, forms an ideal method of converting the output of the resolver into digital format, either for use by a processor or for a visual digital readout of axis position. The diagram shows how a resolver may be used in this type of application with the

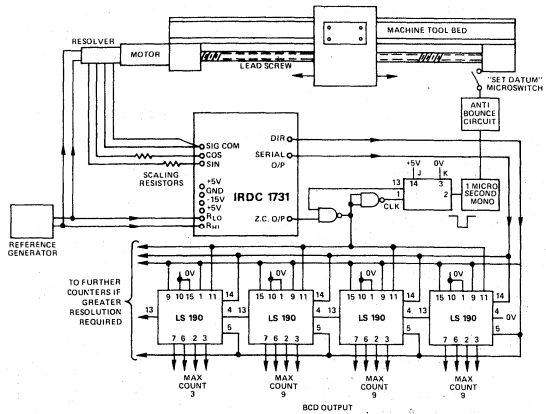


Figure 1. Diagram Showing IRDC1731 Used with a Resolver in a Machine Tool Axis Measurement System

IRDC1731 and external counters to provide a BCD (Binary Coded Decimal) indication of axis position.

In the diagram shown, the number of counters will be sufficient to register the 4000 counts produced by one revolution of the resolver. This means that the counter output will represent a distance equivalent to one pitch of the lead screw (normally 2, 5 or 10 millimeters). In order to provide a readout of the absolute position on the lead screw, more counters can be added as indicated in the diagram.

The "Set Datum" microswitch shown on the end of the lead screw and the associated circuitry is used to zero the counters when the axis movement is at the end of the lead screw. Once the microswitch has been activated, the counters will be reset to zero by the next zero crossing pulse (Z.C. O/P) and the counting will commence. This method gives the advantage that the lead screw zero datum can be accurately set to within one count while the microswitch is only required to operate within one revolution of the lead screw.

DYNAMIC ACCURACY VS. RESOLVER PHASE SHIFT

Most resolvers, particularly those of the brushless variety, exhibit a phase shift between the signal and the reference. This phase shift will give rise under dynamic conditions to an additional error defined by:

$$\frac{\text{Shaft Speed (R.P.S.)} \times \text{Phase Shift (Deg)}}{\text{Reference Frequency}}$$

For example, for a phase shift of 20°, a shaft rotation of 22 revs. per second and a reference frequency of 5kHz, the IRDC1731 will exhibit an additional error of:

$$\frac{20 \times 22}{5000} = 0.088^\circ = 0.98 \text{ counts}$$

This effect can be eliminated by putting a phase lead in the reference to the converter equivalent to the phase shift in the resolver.

USE OF THE IRDC1731 WITH AN INDUCTOSYN FOR MEASURING LINEAR DISPLACEMENT

The IRDC1731 can be used very effectively with an Inductosyn to provide a very accurate linear displacement measurement system. Inductosyns are normally of 2mm pitch and, therefore, the resolution obtainable will be 0.0005mm or 0.5 microns.

The diagram indicates the method of converting the Inductosyn output into digital format.

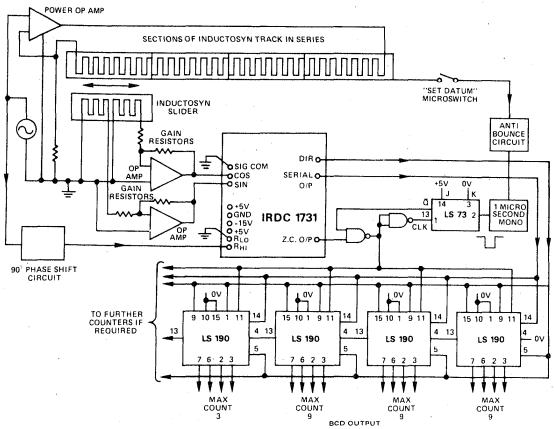


Figure 2. An Inductosyn Used with the IRDC1731 and External Counters

The Inductosyn in this case is made to behave like a resolver. The fixed track is driven from an ac current generator at a frequency of 5kHz, and the resolver format sine and cosine signals are available from the slider. The reason for using a current source is that the track is mainly resistive and it is better to determine the phase by deliberately driving the track from a current source and inserting a 90 degree phase advance into the reference rather than having a less accurately defined phase shift due to the track's X to R ratio.

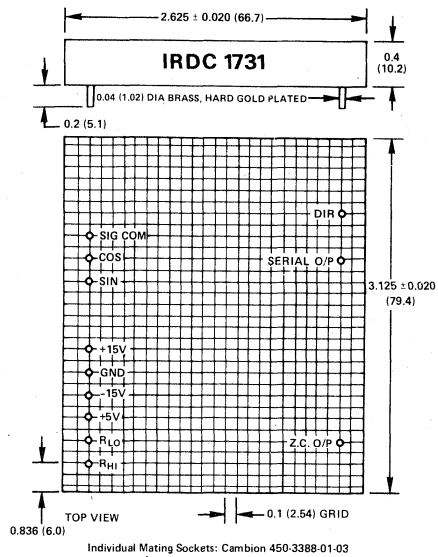
The amplifiers which are necessary between slider and converter need to have equal gains in order to amplify the signals to the 2.5 volts rms required by the converter. (A gain ratio of 1.002 will give rise to an inaccuracy of 1/6000 of a pitch.) A typical voltage which might be available at the input to the input to the amplifiers is 3mV. The amplifiers should be connected as close to the slider as possible with the longer connecting leads being at the high voltage level. The low output impedance of the amplifiers will then drive the cable.

Further information on interfacing the IRDC1731 to Inductosyns is available from the factory.

The "Set Datum" circuitry shown in the diagram is identical to that used for the resolver application, the only provision being that the microswitch always operates within the same pitch of the Inductosyn.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



Individual Mating Sockets: Cambion 450-3388-01-03

ORDERING INFORMATION

Order IRDC1731550 for operation over temperature range of 0 to +70°C. (Commercial)

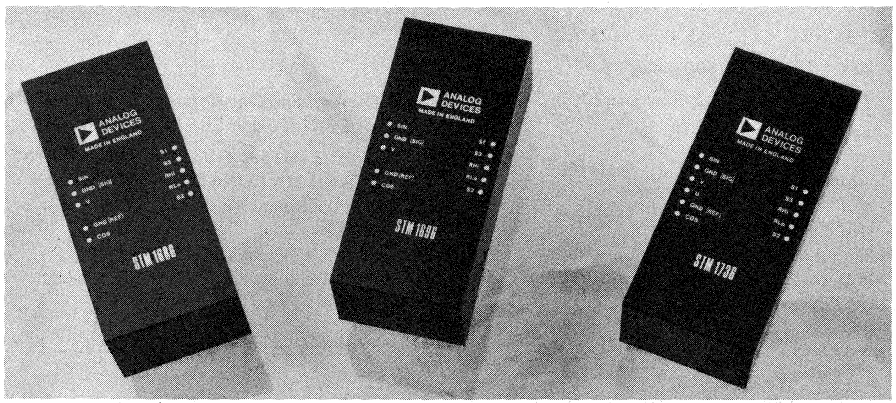
Order IRDC1731650 for operation over temperature range of -55°C to +105°C. (Extended)

OTHER PRODUCTS

In addition to the IRDC1731, we also manufacture a very comprehensive range of products which are concerned with the conversion of synchro and resolver information into digital format.

Of particular note is the IRDC1730 which accepts similar inputs to the IRDC1731 but provides a parallel 12-bit digital representation of the input as well as a direction and Zero crossing output. In addition a dc voltage is provided which represents input velocity.

RTM/STM 1686/1696/1736/1687/1697/1737



RTM/STM 1686

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

ACCURACY[1] (after balancing)	±2.4 arc minutes
OPERATING FREQUENCY	400Hz
LOAD CAPABILITY	5VA
OPERATING TEMPERATURE	-55°C to +105°C
STORAGE TEMPERATURE	-55°C to +125°C
VOLTAGE ISOLATION	500V dc
WEIGHT	21 ounces (580G)

NOTES

[1] Accuracy applies over the full operating temperature range of the option and for:

(a) ±10% reference frequency and amplitude variation.
(b) 10% harmonic distortion on the reference.
(c) Any balanced load from no load to full load.

Specifications subject to change without notice.

APPLICATION OF THE RTM/STM1686

The RTM/STM1686 should be used in conjunction with the DTM1716 or the DTM1717 Digital Vector Generator and the SPA1695 Power Amplifier.

ORDERING INFORMATION

Part Number	Operating Temp. Range	Line-to-Line Output Voltage and Format	Reference Voltage	Reference Frequency
STM1686611	-55°C to +105°C	11.8V Synchro	26V	400Hz
STM1686612	-55°C to +105°C	90.0V Synchro	115V	400Hz
RTM1686618	-55°C to +105°C	11.8V Resolver	26V	400Hz

Note: For options not shown above, consult the factory.

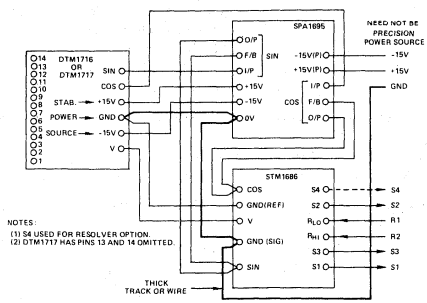
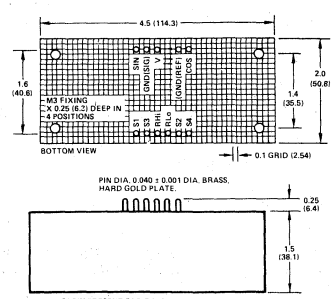


Figure 1. Diagram Showing Connection of the STM1686 to a DTM1716 or DTM1717 and SPA1695 (See Notes)

RTM/STM1686 OUTLINE DIMENSIONS AND PIN CONNECTION DIAGRAM

Dimensions shown in inches and (mm).



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RTM/STM 1696

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

ACCURACY[1] (after balancing)	±2.4 arc minutes
OPERATING FREQUENCY	400Hz
LOAD CAPABILITY	5VA
OPERATING TEMPERATURE	-55°C to +105°C
STORAGE TEMPERATURE	-55°C to +125°C
VOLTAGE ISOLATION	500V dc
WEIGHT	22 ounces (620G)

NOTE:
[1] See STM1686 note 1.
Specifications subject to change without notice.

APPLICATION OF THE RTM/STM1696

The RTM/STM1696 should be used in conjunction with the DSC1705 or DSC1706 Digital to Synchro (or Resolver) Converter and the SPA1695 Power Amplifier.

ORDERING INFORMATION

Part Number	Operating Temp. Range	Line-to-Line Output Voltage and Format	Reference Voltage	Reference Frequency
STM1696611	-55°C to +105°C	11.8V Synchro	26V	400Hz
STM1696612	-55°C to +105°C	90.0V Synchro	115V	400Hz
RTM1696618	-55°C to +105°C	11.8V Resolver	26V	400Hz

Note: For options not shown above, consult the factory.

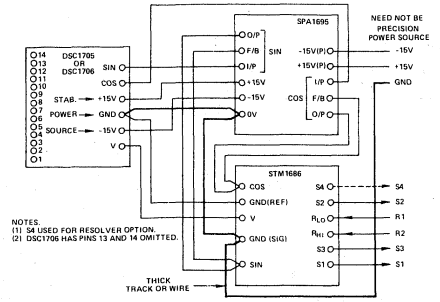
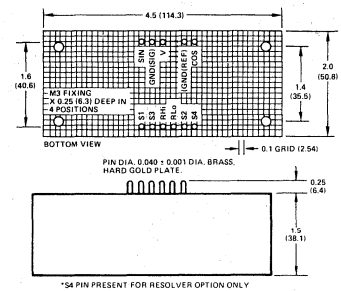


Figure 2. Diagram Showing Connection of the STM1696 to a DSC1705 or DSC1706 and SPA1695 (See Notes)

RTM/STM1686 OUTLINE DIMENSIONS AND PIN CONNECTION DIAGRAM

Dimensions shown in inches and (mm).



RTM/STM 1736

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

ACCURACY[1] (after balancing)	±2.4 arc minutes
OPERATING FREQUENCY	400Hz
LOAD CAPABILITY	5VA
OPERATING TEMPERATURE	-55°C to +105°C
STORAGE TEMPERATURE	-55°C to +125°C
VOLTAGE ISOLATION	500V dc
WEIGHT	19 ounces (540G)

Note:
[1] See STM1686 note 1.
Specifications subject to change without notice.

APPLICATIONS OF THE RTM/STM1736

The RTM/STM1736 should be used in conjunction with the DSC1605 or the DSC1606 Digital to Synchro Converter and the SPA1695 Power Amplifier.

ORDERING INFORMATION

Part Number	Operating Temp. Range	Line-to-Line Output Voltage and Format	Reference Voltage	Reference Frequency
STM1736611	-55°C to +105°C	11.8V Synchro	26V	400Hz
STM1736612	-55°C to +105°C	90.0V Synchro	115V	400Hz
RTM1736613	-55°C to +105°C	11.8V Resolver	11.8V	400Hz
RTM1736614	-55°C to +105°C	26V Resolver	26V	400Hz
RTM1736618	-55°C to +105°C	11.8V Resolver	26V	400Hz

Note: For options not shown above, consult the factory.

NOTES FOR FIGURES 1, 2, AND 3:

1. The "Sin F/B" and the "Cos F/B" pins of the SPA1695 should be connected directly of the "Sin" and "Cos" terminals on the output transformer *at the transformer.*

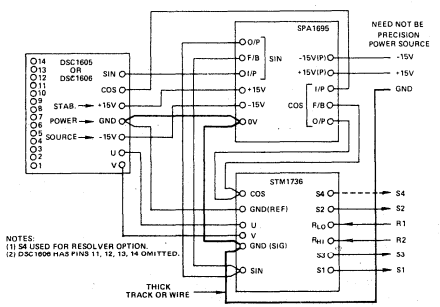
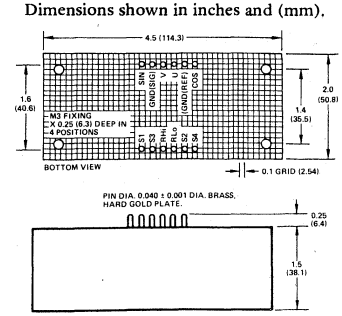


Figure 3. Diagram Showing Connection of the STM1736 to a DSC1605 or DSC1606 and SPA1695 (See Notes)

RTM/STM1736 OUTLINE DIMENSIONS AND PIN CONNECTION DIAGRAM

Dimensions shown in inches and (mm).



This is to compensate for any drop in voltage along the connections between the "Sin O/P" and "Cos O/P" pins of the amplifier and the transformer.

2. The "+15V" and "-15V" pins of the SPA1695 should be connected to a regulated power supply in order to drive the internal operational amplifiers. The "+15V(P)" and "-15V(P)" are used for the output stage and these supplies need not be a precision source, the range of voltage when considering all tolerances including ripple, should be between 14.75 and 20 volts.
3. The part of the 0 volt system local to the amplifier and converter should be tapped from the "GND(SIG)" pin on the transformer and should not interconnect with any other part of the 0 volt system by any other method (see above diagram).

STM 1687

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

ACCURACY[1] (after balancing)	±2.4 arc minutes
OPERATING FREQUENCY	60Hz
LOAD CAPABILITY	5VA
OPERATING TEMPERATURE	-55°C to +105°C
STORAGE TEMPERATURE	-55°C to +125°C
VOLTAGE ISOLATION	500V dc
WEIGHT	3 lbs (1.34kg)

Note:
[1] See STM1686 note 1.
Specifications subject to change without notice.

APPLICATION OF THE STM1687

The STM1687 should be used in conjunction with the DTM1716 or the DTM1717 Digital Vector Generator and the SPA1695 Power Amplifier.

DIMENSIONS AND CONNECTIONS

The STM1687 consists of a kit of two D3953 transformers and one A10163 transformer. These should be connected as shown in Figure 4.

The dimensions are given in Figures 7 and 8.

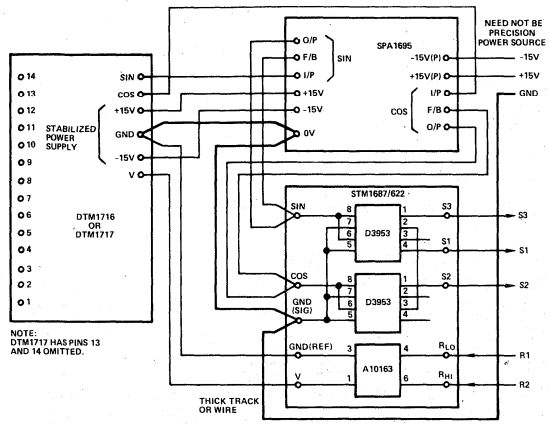


Figure 4. Diagram Showing the Connection of a STM1687 to a DTM1716 or DTM1717 and a SPA1695

ORDERING INFORMATION

The transformer should be ordered as:

STM1687622	50/60Hz, Synchro output, 90 volt signal, 115 volt reference.

Note: For options not shown above, consult the factory.

STM 1697

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

ACCURACY[1] (after balancing)	±2.4 arc minutes
OPERATING FREQUENCY	60Hz
LOAD CAPABILITY	5VA
OPERATING TEMPERATURE	-55°C to +105°C
STORAGE TEMPERATURE	-55°C to +125°C
VOLTAGE ISOLATION	500V dc
WEIGHT	3 lbs (1.34kg)

Note:
[1] See STM1686 note 1.

Specifications subject to change without notice.

APPLICATION OF THE STM1697

The STM1697 should be used in conjunction with the DSC1705 or the DSC1706 Digital to Synchro Converter and the SPA1695 Power Amplifier.

DIMENSIONS AND CONNECTIONS

The STM1697 consists of a kit of two D3953 transformers and one A10033 transformer. These should be connected as shown in Figure 5.

The dimensions are given in Figures 7 and 8.

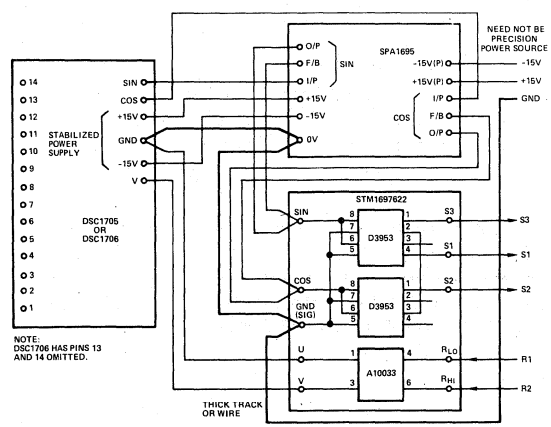


Figure 5. Diagram Showing the Connection of a STM1697 to a DSC1706 or DSC1705 and a SPA1695

ORDERING INFORMATION

This transformer should be ordered as:

STM1697622	50/60Hz, Synchro output, 90 volt signal, 115 volt reference.

Note: For options not shown above, consult the factory.

STM 1737

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

ACCURACY[1] (after balancing)	±2.4 arc minutes
OPERATING FREQUENCY	60Hz
LOAD CAPABILITY	5VA
OPERATING TEMPERATURE	-55°C to +105°C
STORAGE TEMPERATURE	-55°C to +125°C
VOLTAGE ISOLATION	500V dc
WEIGHT	3 lbs (1.34kg)

Note:
[1] See STM1686 note 1.

Specifications subject to change without notice.

APPLICATION OF THE STM1737

The STM1737 should be used in conjunction with the DSC1605 or the DSC1606 Digital to Synchro Converter and the SPA1695 Power Amplifier.

DIMENSIONS AND CONNECTIONS

The STM1737 consists of a kit of two D3953 transformers and one A10033 transformer. These should be connected as shown in Figure 6.

The dimensions are given in Figures 7 and 8.

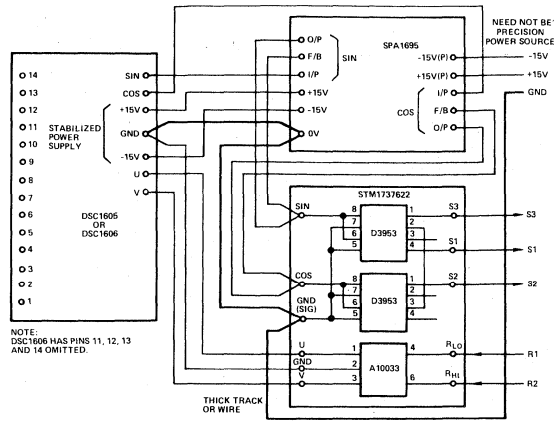


Figure 6. Diagram Showing the Connection of a STM1737 to a DSC1606 or DSC1605 and a SPA1695

ORDERING INFORMATION

This transformer should be ordered as:

STM1737622	50/60Hz, Synchro output, 90 volt signal, 115 volt reference.

Note: For options not shown above, consult the factory.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

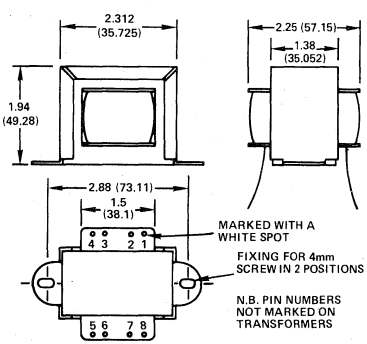


Figure 7. Outline Drawing and Dimensions of the D3953 Transformer

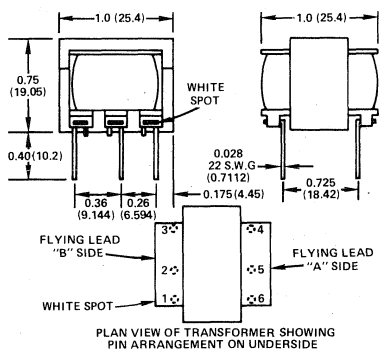


Figure 8. Outline Drawing and Dimensions of the A10163 and A10033 Transformers

BALANCING SCOTT-T TRANSFORMERS (APPLIES ONLY TO TRANSFORMERS IN KIT FORM).

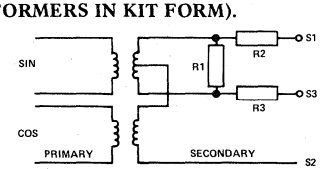


Figure 9. Diagram Showing Balancing Circuit

The Scott T transformers (two D3953 transformers) can be balanced by the following method:

Connect the primary windings of the transformers to give a known angle input of 45°. This can be done by connecting the two coils in parallel to a 7V rms supply, thus giving an equal sine and cosine contribution.

The 3 wire output signal is then monitored on an Angle Position Indicator (e.g. API1620 or API1718) with no load attached. A resistor R1 should be connected across S1 and S3 until the API reads 45.00°.

A balanced load is then connected across S1, S2 and S3 the change in angle is monitored by the API and minimized by adding resistors (R2 and R3) in series with S1 and S3. R2 and R3 will have equal values. Increasing R2 and R3 will decrease the angle monitored by the API.

Suggested initial values for R1 is 27kΩ and for R2 and R3 is 30Ω.

The transformer modules STM1686, 1696 and 1736 are balanced before leaving the factory.

Synchro/Resolver to Linear DC Converter

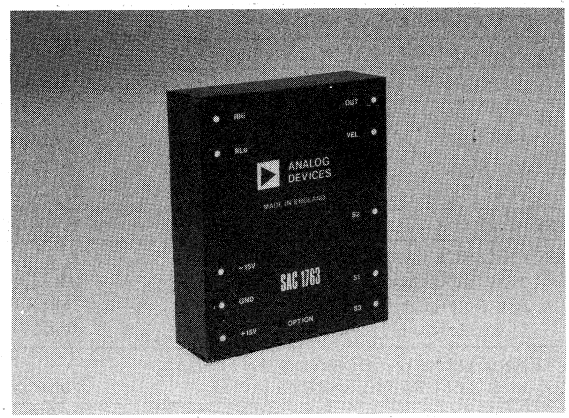
SAC1763

FEATURES

- High Dynamic Performance (27,000°/sec)
- High Accuracy (±11 Arc-Minutes)
- Internal Converter Tracking Loop Provides High Noise Immunity
- Low Output Ripple (Less than 5mV p-p)
- DC Output Proportional to Input Rate
- 50Hz to 2.6kHz Reference Frequency Operation
- Self Contained—No External Transformers or Adjustments Needed

APPLICATIONS

- Measurement and Recording of Synchro or Resolver Information on Chart Recorders, X-Y Plotters, FM Recorders, Etc.
- Servo Control and Positioning



GENERAL DESCRIPTION

The SAC1763 is a Synchro/Resolver to Linear dc Converter. It takes input angular information in synchro or resolver form voltages and gives an output voltage which is linearly proportional to the input angle. The output voltage of ±10V at ±5mA represents an input angular change of ±180 degrees of the synchro or resolver format signals applied to the converter input.

Options are available for all the standard line to line voltages and frequencies for either synchro or resolver inputs. These options together with commercial or extended temperature ranges are determined by a code following the type number (see ordering information).

An important feature of the SAC1763 series converters is that no external transformer modules are required. The transformer isolation is carried out by micro transformers which are inside the converter module *even for the 60Hz versions.*

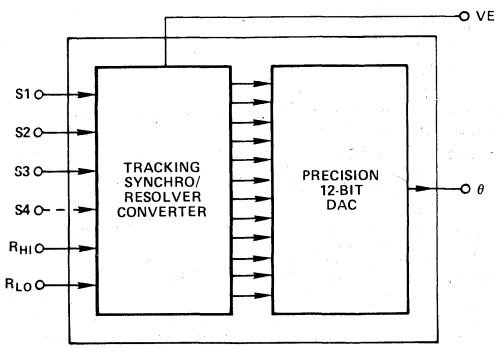
When converters are used in control loops, it is often useful to have a voltage which is proportional to angular velocity. This voltage is available and has been brought out on all SAC1763 converters. The availability of the velocity voltage eliminates the need for a tachometer for stabilization.

MODELS AVAILABLE

Options of the SAC1763 are available to cover all the standard synchro and resolver voltages and frequencies. In addition, options exist for standard operating temperature (0 to +70°C) and extended operating temperature (-55°C to +105°C) (see ordering information).

THEORY OF OPERATION

The SAC1763 is based upon the well proven 12-bit tracking Synchro/Resolver Converter type SDC1700. This is followed by a 12-bit precision DAC (Digital to Analog Converter).



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SPECIFICATIONS (max at 25°C unless otherwise stated)[1]

Model	SAC1763
ACCURACY[2]	±11 arc-minutes
RESOLUTION	1 part in 4096
ANALOG OUTPUT	±10V Representing ±180° 5mA is Available
OUTPUT DRIFT	0.175 arc-minutes per °C
OUTPUT RIPPLE AND NOISE	< 5mV p-p
SIGNAL AND REFERENCE FREQUENCY[1]	60Hz, 400Hz and 2.6kHz
SIGNAL INPUT VOLTAGE (LINE TO LINE)	90V, 26V or 11.8V rms
SIGNAL IMPEDANCE	
90V Signal	200kΩ Resistive
26V Signal	58kΩ Resistive
11.8V Signal	27kΩ Resistive
REFERENCE VOLTAGE	115V, 26V or 11.8V rms
REFERENCE IMPEDANCE	
115V Reference	270kΩ
26V Reference	56kΩ
11.8V Reference	27kΩ
TRANSFORMER ISOLATION ON SIGNAL AND REFERENCE INPUTS	500V dc
MAX INPUT RATES FOR FULL ACCURACY	
60Hz Options	5revs/sec
400Hz Options	36revs/sec
2.6kHz Options	75revs/sec
MAX ACCELERATION ON INPUT FOR ADDITIONAL ERROR LESS THAN 6 ARC-MINUTES	
60Hz Options	166°/sec²
400Hz Options	9668°/sec²
2.6kHz Options	45,528°/sec²
STEP RESPONSE (179° Step) (For less than 6 arc-minutes error)	
60Hz	1.5sec
400Hz	125ms
2.6kHz	50ms
VELOCITY VOLTAGE OUTPUT (See also Specifications on the next page)	±10V nominal for ∓max input rate of the option
POWER SUPPLY REQUIREMENTS	+15V at 150mA -15V at 45mA
POWER DISSIPATION	2.93 watts
OPERATING TEMPERATURE RANGE	
Standard	0 to +70°C
Extended	-55°C to +105°C
STORAGE TEMPERATURE	-55°C to +125°C
DIMENSIONS	3.12" X 2.625" X 0.8" (79.4mm X 66.7mm X 20.3mm)
WEIGHT	7 ozs. (200 grams)

NOTES

[1] The converters can be used over the following reference frequency ranges with no loss of accuracy. They will, however, retain the dynamic characteristics (input rate and acceleration) quoted for the particular option.

60Hz options can be used over 50Hz to 800Hz
400Hz options can be used over 400Hz to 2000Hz
2.6kHz options can be used over 2kHz to 3.5kHz

[2] Accuracy is specfied for the following conditions:

(a) ±10% signal and reference amplitude variation.
(b) ±10% signal and reference harmonic distortion.
(c) ±5% power supply variation.

Specifications subject to change without notice.

CONNECTING THE CONVERTER

The electrical connections to the converter are straighforward. The power lines, which must not be reversed, are ±15V. They must be connected to the "+15V" and "-15V" pins with the common connection to the ground pin "GND".

It is suggested that 0.1μF and 6.8μF capacitors be placed in parallel from +15V to GND, from -15V to GND.

In the case of a Synchro, the signals are connected to "S1", "S2" and "S3" according to the following convention:

$$E_{S1-S3} = E_{RLO-RHI} \sin \omega t \sin \theta$$
$$E_{S3-S2} = E_{RLO-RHI} \sin \omega t \sin (\theta + 120^\circ)$$
$$E_{S2-S1} = E_{RLO-RHI} \sin \omega t \sin (\theta + 240^\circ)$$

For a resolver, the signals are connected to "S1", "S2", "S3" and "S4" according to the following convention:

$$E_{S1-S3} = E_{RLO-RHI} \sin \omega t \sin \theta$$
$$E_{S2-S4} = E_{RHI-RLO} \sin \omega t \cos \theta$$

The system reference voltage is connected to pins "R_{HI}" and "R_{LO}" in accordance with the above convention.

The analog output voltage representing the digital angle is between the pin "OUT" and "GND", ±10V corresponding to ±180 degrees. Up to 5mA may be taken from the "OUT" pin. The relationship between the output voltage and the input angle is shown in the diagram below.

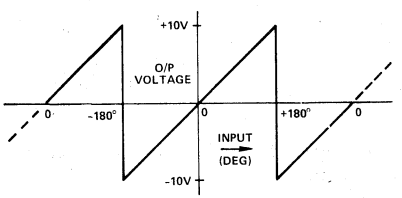


Diagram Showing Relationship Between Input and Output

Sometimes, it is required that the input/output relationship of the converter is the other way round. This can be achieved in the case of synchro options by interchanging connections "S1" and "S3". This is shown in the diagram below.

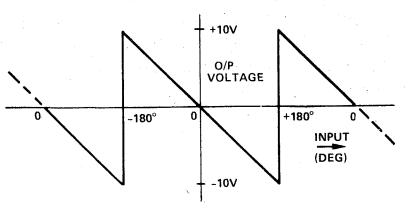


Diagram Showing Relationship Between Input and Output When "S1" and "S3" are Interchanged

VELOCITY PIN

The analog voltage proportional to the rate of change of angle is provided between the pins VEL and GND. The variation is ±10.0V nominal for the maximum velocity of the option.

This pin provides a dc voltage output which is proportional to the angular velocity of the input. The voltage goes negative for an increasing digital angle and goes positive for a decreasing digital angle.

The characteristics of the velocity pin output are given in the following table.

Scaling of Output Voltage for One Fifth max Velocity	2 Volts (Nominal)
Output Voltage Temp. Coeff.	0.05%/°C of Output
Output Voltage Drift (All Models)	0 to +70°C ±50μV/°C -55°C to +105°C ±100μV/°C
Linearity	0 to 100°/sec 60Hz Options 1.5% 0 to 800°/sec 400Hz Options 2% 0 to 1600°/sec 2.6kHz Options 2%
Noise (0 to 20Hz)	60Hz Options: 0 to 200°/sec 2mV rms 400Hz Options: 0 to 1600°/sec 2mV rms 2.6kHz Options: 0 to 3300°/sec 2mV rms
Impedance (Output)	1Ω
max Current Available	1mA

The velocity voltage can be used in closed loop servo systems for stabilization instead of a tachometer.

The SAC1763 velocity outputs do not have the disadvantages of being inefficient at low speeds and do not need gearing required by tachometers. In addition, the output is available at no extra cost.

For other velocity output scaling and linearity consult the factory.

RESISTIVE SCALING OF INPUTS

A feature of this converter is that the signal and reference inputs can be resistively scaled to accommodate any range of input signal and reference voltages.

This means that a standard converter can be used with a personality card in systems where a wide range of input and reference voltages are encountered.

To calculate the values of the external scaling resistors in the case of a Synchro Converter, add 1.11kΩ per extra volt of signal in series with "S1", "S2" and "S3", and 2.2kΩ per extra volt of reference in series with "R_{HI}".

In the case of a Resolver to Digital Converter, add 2.22kΩ in series with "S1" and "S2" per extra volt of signal and 2.2kΩ per extra volt of reference in series with "R_{HI}".

For example, assume that we have an 11.8V line to line, 26V reference Synchro Converter, and we wish to use it with a 60V line to line signal with a 115V reference.

In each signal input line, the extra voltage capability required is:

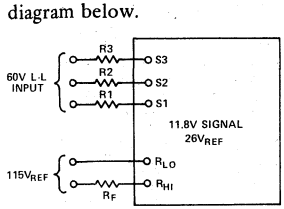
$$60 - 11.8 = 48.2V$$

Therefore each one of the three resistors needs to have a value of:

$$48.2 \times 1.11 = 53.5k\Omega$$

Similarly the single resistor needed in series with "R_{HI}" can be calculated as being 195.8kΩ.

The inputs of the converter can therefore be scaled as in the diagram below.



R1, R2, R3 = 53.5kΩ
R_F = 195.8kΩ

NOTE
IN THE CASE OF THE SIGNAL RESISTORS THE RATIO ERRORS BETWEEN THE RESISTANCES IS MORE IMPORTANT THAN THE ABSOLUTE RESISTANCE VALUES.

IN GENERAL A 1% RATIO ERROR WILL GIVE RISE TO AN EXTRA INACCURACY OF 17 ARC-MINUTES WHILE A RATIO ERROR OF 0.1% WILL GIVE RISE TO AN EXTRA INACCURACY OF 1.7 ARC-MINUTES.

THE ABSOLUTE VALUE OF R_F IS NOT CRITICAL.

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USING THE CONVERTERS WITH OTHER THAN THE SPECIFIED REFERENCE FREQUENCY

The converters can be used with different reference frequencies, other than those for which they are basically specified, with no resulting loss of accuracy (see below). However, they will retain the dynamic characteristics given in the specification.

Basic Option	Frequency Range for no Loss in Accuracy
60Hz	50Hz → 800Hz
400Hz	400Hz → 2000Hz
2.6kHz	2kHz → 3.5kHz

TRANSFER FUNCTION

The transfer functions for the three reference frequency options of the converters are shown below.

60Hz Options

$$\frac{\theta_0}{\theta_1} = \frac{1.9 \times 10^5 \, (1 + 5.6 \times 10^{-2} s)}{s^3 + 1.03 \times 10^2 s^2 + 1.08 \times 10^4 s + 1.9 \times 10^5}$$

400Hz Options

$$\frac{\theta_0}{\theta_1} = \frac{8.8 \times 10^7 \, (1 + 6.8 \times 10^{-3} s)}{s^3 + 8.04 \times 10^2 s^2 + 6.1 \times 10^5 s + 8.8 \times 10^7}$$

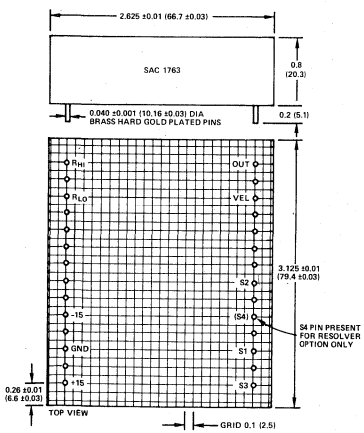
2.6kHz Options

$$\frac{\theta_0}{\theta_1} = \frac{10^9 \, (1 + 3.3 \times 10^{-3} s)}{s^3 + 1.7 \times 10^3 s^2 + 3.303 \times 10^6 s + 10^9}$$

OUTLINE DIMENSIONS AND PIN CONNECTION DIAGRAM

Dimensions shown in inches and (mm).

MATING SOCKET: CAMBION 450-3388-01-03



APPLICATIONS OF THE SAC1763

The SAC1763 may be used to record synchro or resolver information, from for example gyrocompasses or other navigational aids, on to equipment such as X-Y recorders, chart recorders or FM tape recorders, see below.

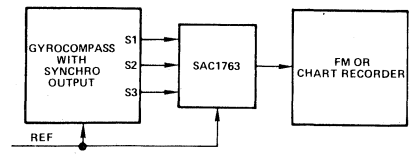


Diagram Showing Gyrocompass Information Being Recorded Using SAC1763

The applications of the SAC1763 are not only in measurement of synchro or resolver information but also in controlling angular movement. The diagram below shows the SAC1763 being used inside an angular control loop where the input is a dc voltage. The availability of the velocity voltage eliminates the need for an electromechanical tachometer for stabilization purposes.

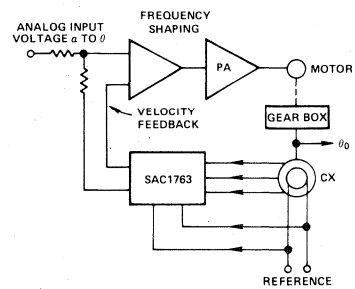


Diagram Showing the SAC1763 Used in a Servo System Where the Input is a dc Voltage

ORDERING INFORMATION

The full part number for all the standard converter options defining reference and signal voltage and frequency, operating temperature range and whether Synchro or Resolver format is given below. It should also be remembered that the signal and reference inputs can be resistively scaled (see section "Resistive Scaling of Inputs") and that in certain cases reference frequencies other than those specified can be used. (See section "Using the Converters with other than the Specified Reference Frequency".)

Part Number	Operating Temp. Range	L to L Voltage/Format	Ref. Voltage	Ref. Freq.
SAC1763511	0 to +70°C	11.8V Synchro	26 Volts	400Hz
SAC1763611	-55°C to +105°C	11.8V Synchro	26 Volts	400Hz
SAC1763512	0 to +70°C	90.0V Synchro	115 Volts	400Hz
SAC1763612	-55°C to +105°C	90.0V Synchro	115 Volts	400Iz
SAC1763522	0 to +70°C	90.0V Synchro	115 Volts	60Hz
SAC1763622	-55°C to +105°C	90.0V Synchro	115 Volts	60Hz
SAC1763513	0 to +70°C	11.8V Resolver	11.8 Volts	400Hz
SAC1763613	-55°C to +105°C	11.8V Resolver	11.8 Volts	400Hz
SAC1763514	0 to +70°C	26.0V Resolver	26 Volts	400Hz
SAC1763614	-55°C to +105°C	26.0V Resolver	26 Volts	400Hz
SAC1763518	0 to +70°C	11.8V Resolver	26 Volts	400Hz
SAC1763618	-55°C to +105°C	11.8V Resolver	26 Volts	400Hz
SAC1763543	0 to +70°C	11.8V Resolver	11.8 Volts	2.6kHz
SAC1763643	-55°C to +105°C	11.8V Resolver	11.8 Volts	2.6kHz
SAC1763544	0 to +70°C	26.0V Resolver	26 Volts	2.6kHz
SAC1763644	-55°C to +105°C	26.0V Resolver	26 Volts	2.6kHz
SAC1763548	0 to +70°C	11.8V Resolver	26 Volts	2.6kHz
SAC1763648	-55°C to +105°C	11.8V Resolver	26 Volts	2.6kHz

BCD Output Synchro to Digital Converters

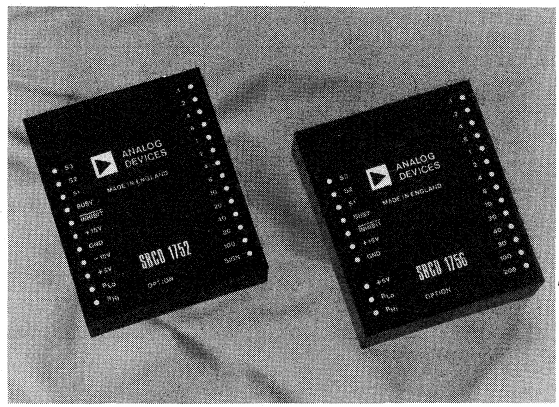
SBCD 1752/1753/1756/1757

FEATURES

- **BCD (Binary Coded Decimal) Output Representing 0 to 359.9° or 0 to ±179.9°**
- **-15V Power Supply Requirement Optional**
- **High Tracking Rate (75 revs/sec)**
- **Internal Microtransformers for 60Hz, 400Hz and 2.6kHz Options**
- **Voltage Scaling with External Resistors (Unique Feature)**
- **Transformer Isolated Outputs**
- **Low Cost**
- **MIL Spec/Hi Rel Options Available**

APPLICATIONS

- **Visual Display of Angular Information**
- **Valve Position Indication**
- **Antenna Monitoring**
- **Industrial Controls**



GENERAL DESCRIPTION

The SBCD1752, SBCD1753, SBCD1756 and the SBCD1757 are modular, continuous tracking Synchro/Resolver to Digital converters which employ a type 2 servo loop.

They are intended for use in both Industrial and Military applications either for displaying angular data directly, or for inputting BCD information directly into a data processing system.

The input signals can be either 3 wire synchro plus reference or 4 wire resolver plus reference, depending on the option. The outputs will be presented in parallel Binary Coded Decimal (BCD).

Particular attention has been paid in the design, to achieving the highest tracking rates and accelerations possible, compatible with the resolution and carrier frequency used, while at the same time obtaining a high overall accuracy.

One of the outstanding features of these converters is the use made of precision Scott T and reference microtransformers. *This has made it possible to include the transformers within the module, even for the 60Hz version as well as providing facilities for external voltage scaling.*

MODELS AVAILABLE

The four Synchro to Digital converters described in this data sheet, differ primarily in the areas of output format and power supply requirements.

Model SBCD1752XYZ is a 13-bit plus sign, BCD output converter, giving -180.0° to -0.1° and +0.0 to +179.9° requiring ±15V and +5V power supplies, and having an overall accuracy of ±0.2 Degrees.

Model SBCD1753XYZ is a 14-bit, BCD output converter, giving 0 to 359.9°, requiring ±15V and +5V power supplies, and having an overall accuracy of ±0.2 Degrees.

Model SBCD1756XYZ is a 13-bit plus sign, BCD output converter, giving -180.0° to -0.1° and +0.0 to +179.9° requiring +15V and +5V power supplies, and having an overall accuracy of ±0.2 Degrees.

Model SBCD1757XYZ is a 14-bit, BCD output converter, giving 0 to 359.9°, requiring +15V and +5V power supplies, and having an overall accuracy of ±0.2 Degrees.

The XYZ code defines the option thus:

X signifies the operating temperature range.
Y signifies the reference frequency.
Z signifies the input voltage and range and whether it will accept Synchro or Resolver information.

More information about the option code is given under the heading "Ordering Information".

DATA TRANSFER (ALL MODELS)

The readiness of the converters for data transfer is indicated by the state of the BUSY pin. The voltage appearing on the BUSY pin consists of a train of pulses, at TTL levels, of length according to the option (see Specifications table). The converter is busy when the BUSY pin is at TTL "High" level. The pulses occur for increasing and decreasing counts.

The most suitable time for transferring data is 400ns after the trailing edge of the BUSY pulse, and the times allowable for data transfer are shown in the specification. Even at the maximum speed of the option, these times will be sufficient to transfer data before the next BUSY pulse occurs.

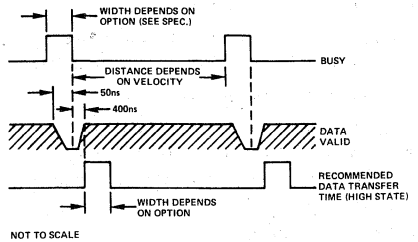
SPECIFICATIONS (typical at 25°C unless otherwise stated)

MODELS	SBCD1752	SBCD1753	SBCD1756	SBCD1757
ACCURACY[1] (max Error)				
All Frequency Options	±0.2 Degrees	*	*	*
OUTPUT	Parallel BCD, 8TTL Loads	*	*	*
RESOLUTION	13-Bit + Sign Representing −180.0° to −0.1° and +0.0° to +179.9°	14 Bit Representing 0 to 359.9°	*	**
SIGNAL AND REFERENCE FREQUENCY	60Hz, 400Hz and 2.6kHz	*	*	*
SIGNAL VOLTAGE (Line to Line)				
Low Level	11.8V rms	*	*	*
High Level	90.0V rms	*	*	*
SIGNAL IMPEDANCES				
Low Level	26kΩ (Resistive)	*	*	*
High Level	200kΩ (Resistive)	*	*	*
REFERENCE VOLTAGE				
Low Level	26V (11.8V Signal)	*	*	*
High Level	115V (90V Signal)	*	*	*
REFERENCE IMPEDANCE				
Low Level	56kΩ (Resistive)	*	*	*
High Level	270kΩ (Resistive)	*	*	*
TRANSFORMER ISOLATION	500V dc	*	*	*
TRACKING RATE (min)				
60Hz	5 Revolutions Per Second	*	*	*
400Hz	36 Revolutions Per Second	*	*	*
2.6kHz	75 Revolutions Per Second	*	*	*
Accel.[1] Constant K_a				
60Hz	2000/sec^2	*	*	*
400Hz	120,000/sec^2	*	*	*
2.6kHz	600,000/sec^2	*	*	*
STEP RESPONSE (179° Step) (For 0.1° Error)				
60Hz	1.5sec	*	*	*
400Hz	125ms	*	*	*
2.6kHz	50ms	*	*	*
POWER LINES	+15V @ 25mA	*	+15V @ 80mA	***
	−15V @ 25mA	*	+5V @ 500mA	***
	+5V @ 500mA	*		
POWER DISSIPATION	3.25 Watts	*	3.7 Watts	***
BUSY LOGIC OUTPUT, POSITIVE PULSE (1 TTL Load)				
60Hz	3.5 to 4.5μs	*	*	*
400Hz	0.5 to 1.25μs	*	*	*
2.6kHz	0.5 to 1.25μs	*	*	*
MAX DATA TRANSFER TIME (From 400ns After Trailing Edge of BUSY at max Velocity)				
60Hz	40μs	*	*	*
400Hz	5.0μs	*	*	*
2.6kHz	1.8μs	*	*	*
$\overline{\text{INHIBIT}}$ INPUT (To Inhibit)	Logic "0" 1TTL Load	*	*	*
TEMPERATURE RANGE				
Operating	0 to +70°C Standard	*	*	*
	−55°C to +105°C Extended	*	*	*
Storage	−55°C to +125°C	*	*	*
DIMENSIONS	3.125" x 2.625" x 0.8"	*	*	*
	(79.4 x 66.7 x 20.4mm)	*	*	*
WEIGHT	6.4 ozs. (180 grams)	*	6.5 ozs. (185 grams)	***

[1] Specified over the appropriate operating temperature range and for
(a) ±10% signal and reference amplitude variation
(b) 10% signal and reference harmonic distortion
(c) ±5% power supply variation
(d) ±10% variation in reference frequency.

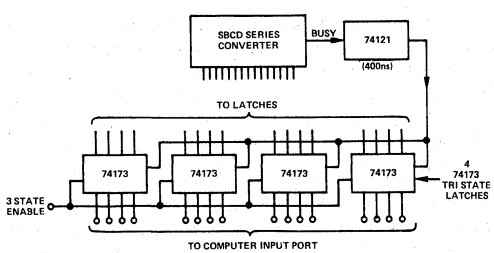
*Specifications same as SBCD1752
**Specifications same as SBCD1753
***Specifications same as SBCD1756

Specifications subject to change without notice.



Data Transfer Diagram

The function of the $\overline{\text{INHIBIT}}$ pin is to enable the user to inhibit the update of the converter's output counter. This is achieved by taking the $\overline{\text{INHIBIT}}$ pin to a TTL Logic zero. If used, the $\overline{\text{INHIBIT}}$ should be applied 400ns after the trailing edge of the BUSY pulse. This will ensure that the data on the output pins is valid. The data should then be transferred and the $\overline{\text{INHIBIT}}$ released before the next BUSY pulse occurs. The worst case times allowable for data transfer in this case are shown in the Specifications under the heading of "MAX DATA TRANSFER TIME (from 400ns After Trailing Edge of BUSY at Max Velocity)". It should be noted that the application of the $\overline{\text{INHIBIT}}$ will not prevent the BUSY pulses appearing on the BUSY pin, and thus if the $\overline{\text{INHIBIT}}$ is not released by the time that the next BUSY pulse occurs, the BUSY pulse will still appear, although the internal converter loop will have been opened. Under this condition, a worst case recovery time, equivalent to that of a step of 179 degrees may be encountered (see Spec.). To avoid this and to ensure valid data transfer, the system shown in the diagram is recommended.



Suggested External Interface Circuitry

In cases where the converter is connected to a data bus or used as a peripheral, the method outlined in the above diagram is recommended. The $\overline{\text{INHIBIT}}$ is not necessary in this case, and the external "Enable" has control of the converter output.

The AC1755 mounting card described later in this data sheet contains the external components shown in the diagram.

CONNECTING THE CONVERTER

The power lines, which should not be reversed, should be connected to "+15V", "-15V" and "+5V" in the case of the SBCD1752 and SBCD1753, and to "+15V" and "+5V" in the case of the SBCD1756 and SBCD1757, with the common connection to "GND" in all cases.

It is suggested that 0.1μF and 6.8μF capacitors be placed in parallel from +15V to GND, from -15V to GND and from +5V to GND.

The digital output connections in the case of the SBCD1753 and SBCD1757 should be taken from the pins marked "0.1" through to "200"; these values being represented in degrees.

In the case of the SBCD1752 and SBCD1756, the data should be taken from the pins marked "0.1" through to "100", these values also being represented in degrees. In the case of these latter units the "SIGN" pin will indicate the polarity of the output, Logic "0" representing positive angles and Logic "1" representing negative angles.

In the case of a synchro, the signals are connected to S_1, S_2 and S_3 according to the following convention:

Synchro connection

$E_{S1-S3} = E_{RLO-RHI} \sin \omega t \sin \theta$
$E_{S3-S2} = E_{RLO-RHI} \sin \omega t \sin (\theta + 120^\circ)$
$E_{S2-S1} = E_{RLO-RHI} \sin \omega t \sin (\theta + 240^\circ)$

For a resolver, the signals are connected to "S1", "S2", "S3" and "S4" according to the following convention:

Resolver Connection

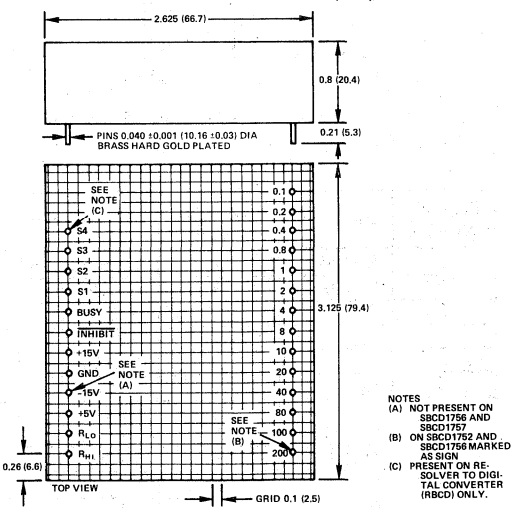
$E_{S1-S3} = E_{RLO-RHI} \sin \omega t \sin \theta$
$E_{S2-S4} = E_{RHI-RLO} \sin \omega t \cos \theta$

The BUSY and $\overline{\text{INHIBIT}}$ pin (if used), should be connected as described under the heading "DATA TRANSFER".

The reference connections are made to pins R_{HI} and R_{LO}.

PIN CONNECTION DIAGRAM

Dimensions shown in inches and (mm).



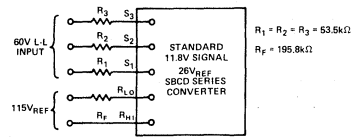
MATING SOCKET: CAMBION 450-3388-01-03

RESISTIVE SCALING OF INPUTS

A unique feature of the SBCD1752/1753/1756/1757 converters is that the inputs can be resistively scaled to accommodate any value of input signal and reference voltage.

In order to calculate the values of the external scaling resistors necessary, add 1.11kΩ in series with the input per extra volt in the case of the signal, and 2.2kΩ per extra volt in the case of the reference.

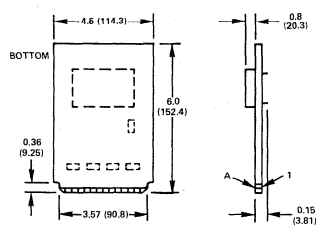
For example, assume that it is required to use a standard 11.8V line to line signal, 26V reference converter with 60V line to line signal and a 115V reference. The resistors should be arranged as in the diagram.



Note: In the case of R_1, R_2, and R_3, the ratio error between the resistances is more critical than the absolute value. In general a 1% ratio error will give rise to an extra inaccuracy of 0.28 Degrees, while a ratio accuracy of 0.1% will give rise to an extra inaccuracy of 0.028 Degrees. The absolute value of R_F is not critical.

CARD MOUNTING

All the converters can be mounted on an AC1755 mounting card. This card contains the latches and monostable, described under the "DATA TRANSFER" heading, which are necessary to transfer the data on to a computer bus system, as well as sockets for the converter. The latches have a tri-state output to facilitate ease of use. The AC1755 also contains facilities for the inclusion of input signal scaling and reference resistors as described under the heading "RESISTIVE SCALING OF INPUTS". The card uses a 22/22 0.156″ pitch edge connector. The pin-out is shown below. If it is not required to use the external latches, they can be jumpered on the board.



AC1755 Mounting Card (First Angle Projection). Dimensions Shown in Inches and (mm).

Edge Pin Number	Function	Edge-Pin Letter	Function
1	R (Lo)	A	Tri-State Enable
2	R (Hi)	F	+15 Volts
3	S_3	H	+15 Volts
4	S_2	J	-15 Volts (3)
5	S_1	K	-15 Volts (3)
6	S_4	L	GND
		M	GND
13	BUSY	N	+5 Volts
15	INHIBIT	P	+5 Volts
16	0.1	T	8
17	0.2	U	10
18	0.4	V	20
19	0.8	W	40
20	1	X	80
21	2	Y	100
22	4	Z	200 (1) SIGN (2)

NOTES
(1) SBCD1753 and SBCD1757 only
(2) SBCD1752 and SBCD1756 only
(3) SBCD1752 and SBCD1753 only

AC1755 Mounting Card Edge Connections

ORDERING INFORMATION

Converters should be ordered by the appropriate part number (i.e., SBCD1752, SBCD1753, SBCD1756 or SBCD1757) followed by the appropriate option code.

If the unit is to be a Resolver to Digital converter, the SBCD should be replaced by RBCD in the part number.

The XYZ options are as follows:

X signifies the operating temperature range thus;
- X = 5 0 to +70°C (Commercial Temp.)
- X = 6 -55°C to +105°C (Extended Temp.)

Y signifies the reference frequency thus;
- Y = 1 signifies 400Hz
- Y = 2 signifies 60Hz*
- Y = 4 signifies 2.6kHz

Z signifies the input signal and reference voltages and whether the converter is a Synchro to Digital or a Resolver to Digital converter. The options for Z are:
- Z = 1 signifies Synchro, signal 11.8 Volts, reference 26 Volts
- Z = 2 signifies Synchro, signal 90 Volts, reference 115 Volts
- Z = 8 signifies Resolver, signal 11.8 Volts, reference 26 Volts

Thus an SBCD1753 with a commercial (0 to +70°C) operating range, using a 400Hz, 26 volt reference with an 11.8 volt signal would be ordered as an SBCD1753511.

*For 50Hz operation, a 60Hz converter can be used with no reduction in accuracy.

In addition a 400Hz unit will work with a 2.6kHz reference and a 60Hz unit will work with a 400Hz reference; however they will have the velocity and acceleration characteristics of the lower frequency rated unit.

OTHER PRODUCTS

The SBCD series of Synchro to Digital converters are just a few of the modules and instruments concerned with Synchro conversion manufactured by us. Some of our other products are listed below and technical data is available. If you have any questions about our products or require advice about the use of them for a particular application, please contact our Applications Engineering Department.

SYNCHRO TO DIGITAL CONVERTERS

The SDC1700 is a low profile (0.4″) converter with a 12-bit natural binary output. Its overall accuracy is ±8.5 arc-minutes, and the module contains internal transformers for all reference frequency options including 60Hz. The SDC1702 is similar to the SDC1700 but has a 10-bit natural binary output and an overall accuracy of ±22 arc-minutes.

The SDC1704 is similar to the above two converters, but has a 14-bit natural binary output and an overall accuracy of ±2.0 arc-minutes ±1LSB.

TWO SPEED PROCESSORS

The TSL1612 and the TSL1729 both produce one digital output word up to 20 bits in length from the outputs of 2 Synchro to Digital converters in a coarse/fine system. The TSL1612 is used for ratios of 9:1, 18:1 and 36:1, while the TSL1729 is programmable for all ratios from 1:1 to 63:1.

DIGITAL TO SYNCHRO CONVERTERS

Resolutions of between 10 and 16 bits are available as well as the DSC1710, a one card, 2 channel, 40VA, DSC system including power amps for use with 2 speed coarse/fine ratios of 9:1, 18:1, 36:1.

ANALOG DEVICES

Low Profile Synchro/Resolver to Digital Converter

SDC1700/1702/1704 Series

FEATURES

- Internal Microtransformers for 60Hz, 400Hz and 2.6kHz References
- Low Profile (0.4")
- 10-, 12- or 14-Bit Resolution for 360°
- High Tracking Rates (75 revs/sec)
- Voltage Scaling with External Resistors (Unique Feature)
- DC Voltage Output Proportional to Angular Velocity
- Low Cost
- Lightweight 3oz. (85 grams)
- MIL Spec/Hi Rel Options Available

APPLICATIONS

- Servo Mechanisms
- Retransmission Systems
- Coordinate Conversion
- Antenna Monitoring
- Simulation
- Industrial Controls
- Fire Control Systems
- Machine Tool Control Systems

GENERAL DESCRIPTION

The SDC1700, SDC1702 and SDC1704 are modular, continuous tracking Synchro/Resolver to Digital Converters which employ a type 2 servo loop.

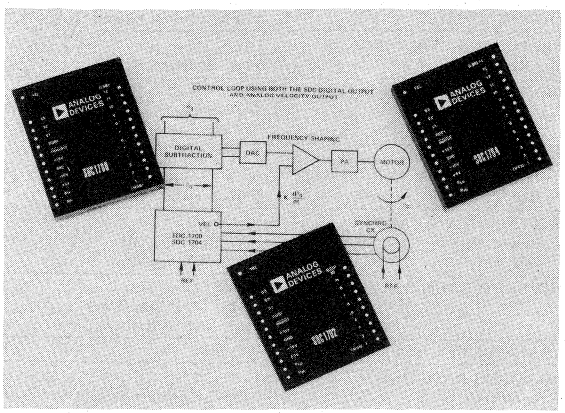
They are intended for use in both Industrial and Military applications.

The input signals can be either 3 wire synchro plus reference or 4 wire resolver plus reference, depending on the option. The outputs will be presented in TTL compatible, parallel natural binary.

One of the outstanding features of the converters is the use of precision Scott T and reference microtransformers. *This has made it possible to include the transformers within the module, even on the 60Hz option, and yet still maintain the profile height of 0.4".*

Particular attention has been paid in the design, to achieving the highest tracking rates and accelerations possible, compatible with the resolution and carrier frequency used, while at the same time obtaining a high overall accuracy.

When SDC's are used in control loops, it is often useful to have a voltage which is proportional to angular velocity. This voltage is available and has been brought out on all the SDC1700 converters.



Extended temperature range versions of all the converters are available.

MODELS AVAILABLE

The three Synchro to Digital Converters described in this data sheet differ primarily in the areas of resolution, accuracy and dynamic performance as follows:

Model SDC1702XYZ is a 10-bit converter which has an overall accuracy of ±22 arc-minutes and a resolution of 21 arc-minutes.

Model SDC1700XYZ is a 12-bit converter with an overall accuracy of ±8.5 arc-minutes and a resolution of 5.3 arc-minutes.

Model SDC1704XYZ is a 14-bit converter with an overall accuracy of ±2.2 arc-minutes ±1LSB and a resolution of 1.3 arc-minutes.

The XYZ code defines the option thus: (X) signifies the operating temperature range, (Y) signifies the reference frequency, (Z) signifies the input voltage and range, and whether it will accept synchro or resolver format.

More information about the option code is given under the heading of "Ordering Information".

NOTE
For all the standard options, no external transformers are needed with these converters.

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SPECIFICATIONS (typical @ +25°C unless otherwise noted)

MODELS	SDC1702	SDC1700	SDC1704
ACCURACY[1] (max error)			
60Hz	±22 arc-minutes	±8.5 arc-minutes	±2.9 arc-minutes ±1LSB
400Hz	±22 arc-minutes	±8.5 arc-minutes	±2.2 arc-minutes ±1LSB
2.6kHz	±22 arc-minutes	±8.5 arc-minutes	±2.9 arc-minutes ±1LSB
RESOLUTION	10 Bits (1LSB = 21 arc-mins)	12 Bits (1LSB = 5.3 arc-mins)	14 Bits (1LSB = 1.3 arc-mins)
OUTPUT (In Parallel)	10 Bits (Natural Binary)	12 Bits (Natural Binary)	14 Bits (Natural Binary)
SIGNAL AND REFERENCE FREQUENCY	60Hz, 400Hz, 2.6kHz	*	*
SIGNAL VOLTAGE (Line-to-Line)			
Low Level	11.8V rms	*	*
High Level	90V rms	*	*
SIGNAL IMPEDANCES			
Low Level	26kΩ (Resistive)	*	*
High Level	200kΩ (Resistive)	*	*
REFERENCE VOLTAGE			
Low Level	26V (11.8V Signal)	*	*
High Level	115V (90V Signal)	*	*
REFERENCE IMPEDANCE	270kΩ (115V Signal)	*	*
	56kΩ (26V Reference)	*	*
	(Impedance is Resistive)	*	*
TRANSFORMER ISOLATION	500V dc	*	*
TRACKING RATE (min)			
60Hz	5 Revolutions Per Second	*	500°/sec
400Hz	36 Revolutions Per Second	*	12 Revolutions Per Second
2.6kHz	75 Revolutions Per Second	*	25 Revolutions Per Second
Accel.[1] Constant K_a			
60Hz	1880/sec²	*	520/sec²
400Hz	110,000/sec²	*	36,000/sec²
2.6kHz	518,000/sec²	*	170,000/sec²
STEP RESPONSE (179° Step) (For 1LSB Error)			
60Hz	1.5sec	*	*
400Hz	125ms	*	*
2.6kHz	50ms	*	*
POWER LINES	±15V @ 25mA, +5V @ 70mA } ±5%	*	±15V @ 30mA, +5V @ 85mA } ±5%
POWER DISSIPATION	1.1 Watts	*	1.3 Watts
DATA LOGIC OUTPUT[2] (TTL Compatible)	2TTL Loads SDC17026YZ 4TTL Loads SDC17025YZ	2TTL Loads SDC17006YZ 4TTL Loads SDC17005YZ	2TTL Loads on All Options
BUSY LOGIC OUTPUT, POSITIVE PULSE (1 TTL Load)			
60Hz	9.0μs } ±30%	*	9.0μs } ±30%
400Hz	2.0μs } ±30%	*	2.0μs } ±30%
2.6kHz	2.0μs } ±30%	*	1.3μs } ±30%
MAX DATA TRANSFER TIME			
60Hz	40μs	*	35μs
400Hz	5.0μs	*	3.0μs
2.6kHz	1.8μs	*	0.8μs
INHIBIT INPUT (To Inhibit)	Logic "0" 1 TTL Load	*	Logic "0" 2 TTL Loads
WARM UP TIME	1 sec to Rated Accuracy	*	*
TEMPERATURE RANGE			
Operating	0 to +70°C Standard	*	*
	−55°C to +105°C Extended	*	*
Storage	−55°C to +125°C	*	*
DIMENSIONS	3.125" x 2.625" x 0.4" (79.4 x 66.7 x 10.2mm)	*	*
WEIGHT	3 ozs. (85 grams)	*	*

*Specification same as SDC1702

[1] Specified over the appropriate operating temperature range of the option and for: (a) ± 10% signal and reference amplitude variation (b) 10% signal and reference Harmonic Distortion (c) ±5% power supply variation (d) ±10% variation in reference frequency.

[2] It is recommended that buffers should be used if the above converters are required to drive over a distance greater than 6".

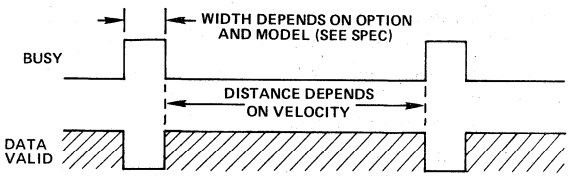
Specifications subject to change without notice.

DATA TRANSFER (All Models)

The readiness of the converters for data transfer is indicated by the state of the BUSY pin.

The voltage appearing on the BUSY pin consists of a train of pulses, at TTL levels, of length according to the model and option (see specification table). The converter is busy when the BUSY pin is at a TTL "High" level. These pulses correspond to those delivered by the VCO to increment or decrement the up-down counter (see schematic diagram). Thus the pulses will occur for increasing and decreasing counts.

The most suitable time for transferring data is when the BUSY is at a logic "Lo" state, and the times allowable for data transfer are shown in the specification. Even at the maximum speed of the option, these times will be sufficient to transfer data before the next BUSY pulse occurs.



Data Transfer Diagram

DATA TRANSFER DIAGRAM

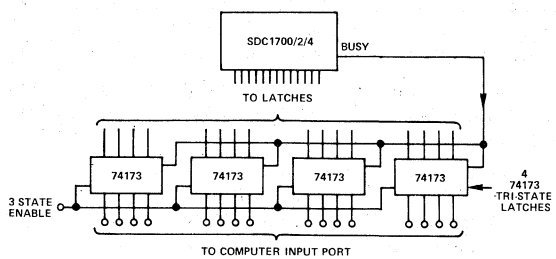
Taking the INHIBIT to a logic "Lo" state prevents the VCO (BUSY) pulses from updating the up-down counter. However, if applied during a BUSY pulse, the INHIBIT will not become effective until the end of the BUSY pulse.

The best method of transferring the data is by applying the INHIBIT (taking it to a logic "Lo" state), waiting for at least the width of a BUSY pulse, transferring the data and releasing the INHIBIT.

Note that sustained application of the INHIBIT opens the internal control loop and the converter may take on appreciable time to recover to full accuracy when the loop is restored.

INTERFACING WITH A COMPUTER

It is recommended that external latches are used to enable data to be transferred onto a computer data bus. One method is shown in the diagram. Using this method will mean that the latches are constantly updated by the BUSY signal, while at the same time enabling inputs to be made to the computer by means of normal data transfer procedures. The AC1755 mounting card contains these external components.



Suggested External Computer Interface Circuitry

THEORY OF OPERATION

If the unit is a Synchro to Digital Converter, then the 3 wire synchro output will be connected to S1, S2 and S3 on the module and the Scott T transformer pair will convert these signals into resolver format.

i.e., $V_1 = K E_O \text{ Sin } \omega t \text{ Sin } \theta$

$V_2 = K E_O \text{ Sin } \omega t \text{ Cos } \theta$

Where θ is the angle of the Synchro Shaft.

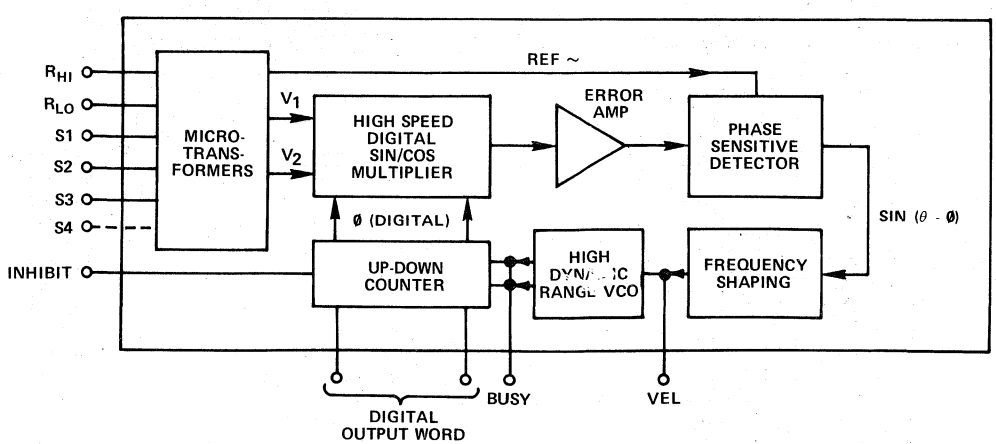
If the unit is a Resolver to Digital Converter, then the 4 wire resolver output will be connected to S1, S2, S3 and S4 on the module and the microtransformer will act purely as an isolator.

To understand the conversion process, then assume that the current word state of the up-down counter is ϕ.

The V_1 is multiplied by Cos ϕ and V_2 is multiplied by Sin ϕ to give

$K E_O \text{ Sin } \omega t \text{ Sin } \theta \text{ Cos } \phi$

and $K E_O \text{ Sin } \omega t \text{ Cos } \theta \text{ Sin } \phi$



Functional Diagram of the SDC1700/2/4 Converters

These signals are subtracted by the error amplifier to give:

$$K E_O \text{ Sin } \omega t \text{ (Sin } \theta \text{ Cos } \phi - \text{Cos } \theta \text{ Sin } \phi)$$

or $$K E_O \text{ Sin } \omega t \text{ Sin } (\theta - \phi)$$

A phase sensitive detector, integrator and Voltage Controlled Oscillator (VCO) form a closed loop system which seeks to null Sin $(\theta - \phi)$.

When this is accomplished, the word state of the up-down counter (ϕ), equals within the rated accuracy of the converter, the synchro shaft angle θ.

CONNECTING THE CONVERTER

The electrical connections to the converter are straightforward. The power lines, which must not be reversed, are ±15V and 5V. They must be connected to the "±15V" and "5V" pins with the common connection to the ground pin GND.

It is suggested that 0.1μF and 6.8μF capacitors be placed in parallel from +15V to GND, from -15V to GND and from +5V to GND.

The digital output is taken from pins:

1 through to 10 for the SDC1702
1 through to 12 for the SDC1700
1 through to 14 for the SDC1704

Pin 1 represents the MSB in each case. The reference connections are made to pins "R_{HI}" and "R_{LO}".

In the case of a Synchro, the signals are connected to "S1", "S2" and "S3" according to the following convention:

$$E_{S1-S3} = E_{RLO-RHI} \text{ Sin } \omega t \text{ Sin } \theta$$
$$E_{S3-S2} = E_{RLO-RHI} \text{ Sin } \omega t \text{ Sin } (\theta + 120^\circ)$$
$$E_{S2-S1} = E_{RLO-RHI} \text{ Sin } \omega t \text{ Sin } (\theta + 240^\circ)$$

For a resolver, the signals are connected to "S1", "S2", "S3" and "S4" according to the following convention:

$$E_{S1-S3} = E_{RLO-RHI} \text{ Sin } \omega t \text{ Sin } \theta$$
$$E_{S2-S4} = E_{RHI-RLO} \text{ Sin } \omega t \text{ Cos } \theta$$

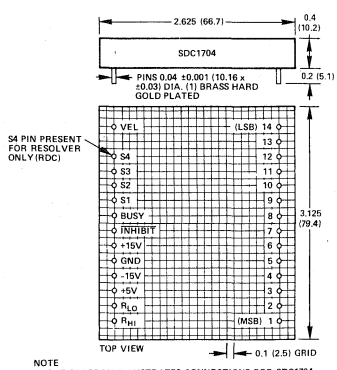
The analog voltage representing velocity is available between "VEL" and "GND".

The "BUSY" and "INHIBIT" pin (if used), should be connected as described under the heading "Data Transfer".

NOTE: If the INHIBIT pin is used (i.e., driven to 0 volts), the control loop will be opened and a finite time will be required (see spec) for the converter to recover.

OUTLINE DIMENSIONS AND PIN CONNECTION DIAGRAM

Dimensions are shown in inches and (mm).



NOTE
ABOVE DIAGRAM ILLUSTRATES CONNECTIONS FOR SDC1704. FOR SDC1700, PINS 13 AND 14 ARE OMITTED. PIN 12 IS LSB. FOR SDC1702, PINS 11, 12, 13, 14 ARE OMITTED. PIN 10 IS LSB.

MATING SOCKET: CAMBION 450-3388-01-03

RESISTIVE SCALING OF INPUTS

A unique feature of the SDC1700 series of converters is that the inputs can be resistively scaled to accommodate any range of input signal and reference voltages.

This means that a standard converter can be used with a personality card in systems where a wide range of input and reference voltages are encountered. In addition it should be noted that a 400Hz unit will operate from a 2.6kHz reference. It will however have the velocity and acceleration characteristics as specified for the 400Hz converter. A 60Hz converter will operate from a 400Hz reference and will have the velocity and acceleration characteristics as specified for the 60Hz converter.

To calculate the values of the external scaling resistors for a synchro converter, add 1.11kΩ in series with S1, S2 and S3 per extra volt in the case of the signal, and 2.2kΩ in the case of the reference. In the case of a resolver converter add 2.22kΩ per extra volt in series with S1 and S2 for the signal and 2.2kΩ per extra volt in series with R_{HI} for the reference.

For example, assume that we have an 11.8 volt line to line signal/26.0 volt reference converter, and we wish to use a 60 volt line to line signal with a 115 volt reference.

Thus in each signal input line, the extra voltage capability required is:

60 - 11.8 = 48.2 volts

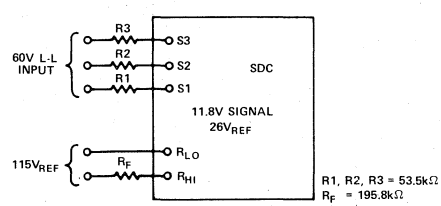
Therefore each resistor needs to have a value of 48.2 x 1.11 = 53.5kΩ. In the case of the reference, the extra voltage capability required is:

115 - 26.0 = 89 volts

Therefore the resistor needs to have a value of:

89.0 x 2.2 = 195.8kΩ

Thus the inputs can be scaled as in the diagram below.



NOTE
IN THE CASE OF R1, R2 AND R3, THE RATIO ERRORS BETWEEN THE RESISTANCES IS MORE IMPORTANT THAN THE ABSOLUTE RESISTANCE VALUES.

IN GENERAL A 1% RATIO ERROR WILL GIVE RISE TO AN EXTRA INACCURACY OF 17 ARC-MINUTES WHILE A RATIO ERROR OF 0.1% WILL GIVE RISE TO AN EXTRA INACCURACY OF 1.7 ARC-MINUTES.

THE ABSOLUTE VALUE OF R_F IS NOT CRITICAL.

BIT WEIGHT TABLE

Bit Number	Weight in Degrees
1 (MSB)	180.0000
2	90.0000
3	45.0000
4	22.5000
5	11.2500
6	5.6250
7	2.8125
8	1.4063
9	0.7031
10 (LSB for SDC1702)	0.3516
11	0.1758
12 (LSB for SDC1700)	0.0879
13	0.0439
14 (LSB for SDC1704)	0.0220

VELOCITY PIN

This pin provides a voltage output which is proportional to the angular velocity of the input. The voltage goes negative for an increasing digital angle and goes positive for a decreasing digital angle.

The characteristics of the velocity pin output are given in the table below.

Scaling of Output Voltage for One Fifth max Velocity	2Volts (Nominal)
Output Voltage Temp. Coeff.	0.05%/°C of Output
Output Voltage Drift (All Models)	0 to +70°C ±50μV/°C -55°C to +105°C ±100μV/°C
Linearity:	0°/sec to 800°/sec SDC1704 400Hz 1% 0°/sec to 100°/sec SDC1704 60Hz 1% 0°/sec to 800°/sec SDC1700/2 400Hz 2% 0°/sec to 100°/sec SDC1700/2 60Hz 1.5%
Noise: (0 to 20Hz)	@1600°/sec SDC1700/2/4 400Hz 2mV rms @200°/sec SDC1700/2/4 60Hz 2mV rms
Impedance (Output)	1Ω
max Current Available	1mA

The velocity voltage can be used in closed loop servo systems for stabilization instead of a tachometer.

The SDC1700/2/4 velocity outputs do not have the disadvantages of being inefficient at low speeds and do not need gearing required by tachometers. In addition, the output is available at no extra cost.

For other velocity output scaling and linearity consult the factory.

Two examples of the use of the velocity pin are shown in the diagram below.

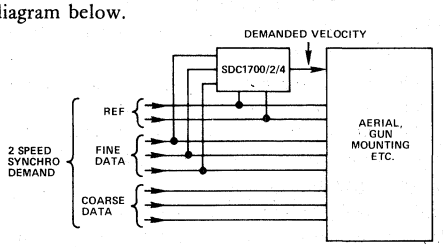


Diagram showing a velocity feed forward application. The SDC is used to produce the demanded velocity from Synchro form inputs.

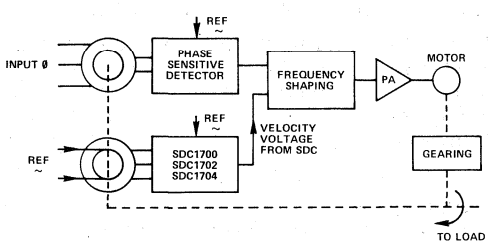
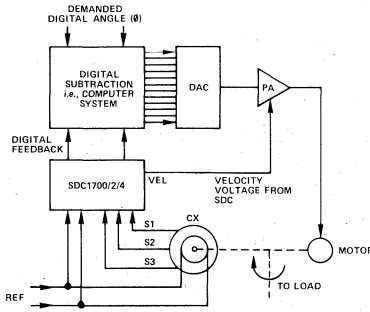


Diagram showing the velocity voltage being used to stabilize an electro-mechanical control loop

APPLICATIONS OF SYNCHRO TO DIGITAL CONVERTERS

SDCs can be used in a variety of ways in control loops as well as for the conversion of angular data into a form which is readily acceptable to digital displays or computers.

The diagram below shows an SDC being used in a digitally controlled feedback loop.



An SDC Being Used in a Digitally Controlled Feedback Loop

Such loops as shown in the diagram above require the high dynamic performance of the SDC1700 series converters. It should be noted that in this application, the SDC1700 series will replace conventional tachometers and phase sensitive detectors while at the same time provide digital position feedback.

Many synchro systems employ a two speed, geared arrangement utilizing one synchro for the fine shaft and one for the coarse. An example of this type is shown below.

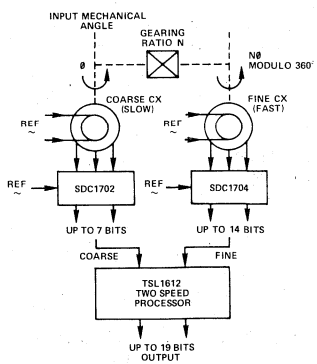


Diagram Showing Coarse/Fine Synchro Processor System

In the above example, two tracking SDC's are being used to provide data for coarse/fine (two speed) data transmission systems.

The TSL1612 is a processor which combines the outputs of two SDC's to provide one output word of up to 19 bits in length.

The TSL1612 is available for any ratio between 2:1 and 36:1 and provides automatic compensation for misalignment of the coarse synchro relative to its shaft. It also corrects for any overlap between the digits of the coarse and fine shafts.

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MEAN TIME BETWEEN FAILURES (M.T.B.F.)

The estimated mean time between failures is given as follows:

SDC1700/2	174,000 Hours
SDC1704	167,000 Hours

Further information relating to M.T.B.F. and to the quality control and test procedures employed by us can be obtained from the factory on request.

TRANSFER FUNCTION

The transfer function of the SDC1700/2 and SDC1704, 400Hz versions, is given below.

For the transfer functions of the other models or for a detailed analysis of those given here, please contact us.

SDC1700/2 400Hz

$$\frac{\theta_0}{\theta_1} = \frac{8.8 \times 10^7 (1 + 6.8 \times 10^{-3} s)}{s^3 + 8.04 \times 10^2 s^2 + 6.1 \times 10^5 s + 8.8 \times 10^7}$$

SDC1704 400Hz

$$\frac{\theta_0}{\theta_1} = \frac{2.95 \times 10^7 (1 + 8.2 \times 10^{-3} s)}{s^3 + 8.05 \times 10^2 s^2 + 1.95 \times 10^5 s + 2.95 \times 10^7}$$

CARD MOUNTING

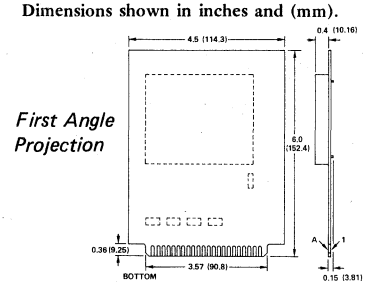
All the converters can be mounted on an AC1755 mounting card. This card contains the latches described under the "Data Transfer" heading, which are necessary to transfer the data on to a computer bus system, and sockets for the converter.

The latches have a tri-state output to facilitate ease of use.

The AC1755 also contains facilities for the inclusion of input signal and reference scaling resistors as described under the heading "Resistive Scaling of Inputs".

The card uses a 22/22 0.156″ pitch edge connector. The pin out is shown below. If it is not required to use the external latches, they can be jumpered on the board.

AC1755 MOUNTING CARD
Dimensions shown in inches and (mm).



EDGE CONNECTIONS AC1755

Edge Pin Number	Function	Edge Pin Letter	Function
1	R (Lo)	A	Tri-State Enable
2	R (Hi)	F	+15V
3	S3	H	+15V
4	S2	J	-15V
5	S1	K	-15V
6	S4	L	GND
8	VEL	M	GND
13	BUSY	N	+5V
15	INHIBIT	P	+5V
16	BIT 14	T	BIT 7
17	BIT 13	U	BIT 6
18	BIT 12	V	BIT 5
19	BIT 11	W	BIT 4
20	BIT 10	X	BIT 3
21	BIT 9	Y	BIT 2
22	BIT 8	Z	BIT 1

NOTE: SDC1702 does not use pins 16, 17, 18 or 19. SDC1700 does not use pins 16 and 17.

ORDERING INFORMATION

Parts should be ordered by the appropriate part number (i.e., SDC1700, SDC1702, SDC1704) followed by the appropriate XYZ option code.

If the unit is to be a Resolver to Digital Converter, the SDC should be replaced by RDC in the part number.

The XYZ options are as follows:
X signifies the operating temperature range and the options are:

X = 5 signifies 0 to +70°C (commercial) temperature.
X = 6 signifies -55°C to +105°C (extended) temperature.

Y signifies the reference frequency and the options are:

Y = 1 signifies 400Hz
Y = 2 signifies 60Hz *
Y = 4 signifies 2.6kHz

Z signifies the input signal and reference voltages and whether the converter is an SDC or an RDC. The options are:

Z = 1 signifies synchro, signal 11.8V rms, reference 26V rms
Z = 2 signifies synchro, signal 90V rms, reference 115V rms
Z = 3 signifies resolver, signal 11.8V rms, reference 11.8V rm
Z = 4 signifies resolver, signal 26V rms, reference 26V rms
Z = 8 signifies resolver, signal 11.8V rms, reference 26V rms

Thus, for example, an SDC1704 with a commercial (0 to +70°C) operating range, using a 400Hz, 26V reference with an 11.8V signal would be ordered as an SDC1704511.

For other than these options, consult the factory.

CAUTIONS

Do not reverse the power supplies.
Do not connect signal and/or reference inputs to other than S1, S2, S3, S4, R_{HI} or R_{LO}.

Do not connect signals and/or references to a lower voltage rated converter. (Such as a 115V Synchro into a 26V Converter).

Misconnections as per the above will damage the units and void the warranty.

OTHER PRODUCTS

The SDC1700/2/4 converters are just a few of the modules and instruments concerned with Synchro and Resolver conversion manufactured by us.

Other products are listed below and technical data is available. If you have any questions about our products, or require advice about the use of them for a particular application, please contact our Applications Engineering Department.

TWO SPEED PROCESSORS

Which utilize the digital outputs of two SDCs in a 2 speed coarse/fine system to produce one combined digital word of up to 19 bits in length. The TSL1612 in particular is available for any ratio between 2:1 and 36:1.

DIGITAL TO SYNCHRO CONVERTERS

Resolutions of between 10 and 14 bits are available.

BCD OUTPUT SYNCHRO TO DIGITAL CONVERTERS

The SBCD1752 and SBCD1753 are converters with a BCD instead of a binary output based upon the SDC1700. They have outputs of ±180.0 degrees and 0 to 360.0 degrees respectively.

***50Hz Operation**

For 50Hz operation, a 60Hz converter can be used with no reduction in accuracy.

Ultra-Low Profile (0.35") Three-State Latched Output S to D Converters

SDC1725/1726

FEATURES

- Three-State Latched Output
- Continuous Tracking Even During Data Transfer
- Simple Data Transfer Facility
- Low Profile 0.35" (8.9mm)
- Internal Transformers for 60Hz, 400Hz and 2.6kHz References
- Signal and Reference Voltage Scaling with External Resistors
- High Tracking Rates (50 revs/sec)
- Lightweight 3.3 oz. (93 gms)
- MIL Spec/Hi Rel Options Available

APPLICATIONS

- Servo Mechanisms
- Retransmission Systems
- Coordinate Conversion
- Antenna Monitoring
- Simulators
- Industrial Controls
- Artillery Fire Control Systems
- Machine Tool Control Systems

GENERAL DESCRIPTION

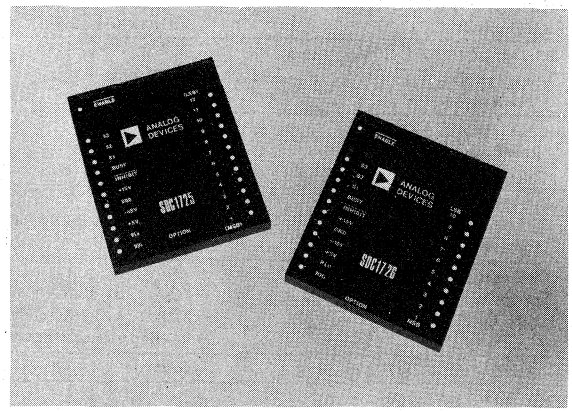
The SDC1725 and SDC1726 are modular, continuous tracking Synchro/Resolver to Digital Converters which employ a type 2 servo loop and contain three-state latches on the digital outputs.

The input signals can be either 3 wire synchro plus reference or 4 wire resolver plus reference depending on the option. The outputs will be presented in TTL compatible parallel natural binary, buffered by three-state latches.

The three-state output facility not only simplifies multiplexing of more than one device onto a single data bus but also enables the "INHIBIT" to be used without opening the internal converter loop.

Another outstanding feature of these converters is the use of precision Scott T and reference microtransformers. This has made it possible to include internal transformers, even on the 60Hz options, and yet obtain a profile height lower than any other modular Synchro/Resolver to Digital Converter currently available.

NOTE
No external transformers are required with these converters.



MODELS AVAILABLE

The two Synchro/Resolver to Digital Converters described in this data sheet differ primarily in the areas of resolution and accuracy as follows:

Model SDC1725XYZ is a 12-bit converter with an overall accuracy of ±3.2 arc-minutes ±1LSB and a resolution of 5.3 arc-minutes.

Model SDC1726XYZ is a 10-bit converter with an overall accuracy of ±22 arc-minutes and a resolution of 21 arc-minutes.

The XYZ code defines the option as follows: (X) signifies the operating temperature range, (Y) signifies the reference frequency, (Z) signifies the signal and reference voltage and whether it will accept synchro or resolver format.

More information about the option code is given under the heading of "Ordering Information".

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SPECIFICATIONS (typical at +25°C unless otherwise stated)

Models	SDC1725	SDC1726
ACCURACY[1] (max Error all Options)	±3.2 arc-minutes ±1LSB	±22 arc-minutes
RESOLUTION	12 Bits	10 Bits
OUTPUT	12-Bits Parallel Natural Binary	10-Bits Parallel Natural Binary
SIGNAL AND REFERENCE FREQUENCY	60Hz, 400Hz, 2.6kHz	*
SIGNAL VOLTAGE (Line to Line)		
Low Level	11.8V rms	*
High Level	90.0V rms	*
SIGNAL IMPEDANCES		
Low Level	26kΩ Resistive	*
High Level	200kΩ Resistive	*
REFERENCE VOLTAGE		
Low Level	26V rms (11.8V Signal)	*
High Level	115V rms (90.0V Signal)	*
REFERENCE IMPEDANCE		
Low Level	56kΩ (26V Reference)	*
High Level	270kΩ (115V Reference)	*
	(Impedance is Resistive)	*
TRANSFORMER ISOLATION	500V dc	*
TRACKING RATE (Minimum)		
60Hz Options	5 Revolutions Per Second	*
400Hz Options	36 Revolutions Per Second	*
2.6kHz Options	50 Revolutions Per Second	*
ACCELERATION		
Constant K_a		
60Hz Options	2000/sec^2	*
400Hz Options	120,000/sec^2	*
2.6kHz Options	600,000/sec^2	*
STEP RESPONSE (179° Step) (For 1LSB Error)		
60Hz Options	1.5sec	*
400Hz Options	125ms	*
2.6kHz Options	50ms	*
POWER LINES	+15V @ 25mA	*
	-15V @ 25mA	*
	+5V @ 120mA	*
POWER DISSIPATION	1.35 Watts	*
DATA LOGIC OUTPUTS[2] (TTL Compatible)	6TTL Loads All Options	*
BUSY LOGIC OUTPUT LOADING[2]	2TTL Loads	*
BUSY LOGIC OUTPUT WIDTH[2]	330ns max, 200ns min	*
INHIBIT INPUT (TO INHIBIT)	Logic "0" 1 TTL Load	*
ENABLE INPUT (TO ENABLE)	Logic "0" 1 TTL Load	*
WARM UP TIME	1sec to Rated Accuracy	*
TEMPERATURE RANGE		
Operating	0 to +70°C Standard	*
	-55°C to +105°C Extended	*
Storage	-55°C to +125°C	*
DIMENSIONS	3.125" X 2.625" X 0.35"	*
	(79.4 X 66.7 X 8.9mm)	*
WEIGHT	3.3 ozs (93 gms)	*

*Specifications the same as for SDC1725.

NOTES
[1] Specified over the appropriate operating temperature range and for: (a) ±10% signal and reference amplitude variation; (b) 10% signal and reference harmonic distortion; (c) ±5% power supply variation; and (d) ±10% variation in reference frequency.
[2] Schottky logic loading rules apply.

Specifications subject to change without notice.

THEORY OF OPERATION

If the unit is a Synchro to Digital Converter the 3 wire synchro output will be connected to S1, S2 and S3 on the module and the Scott T transformer pair will convert these signals into resolver format.

i.e., $V_1 = K E_O \text{ Sin } \omega t \text{ Sin } \theta$

$V_2 = K E_O \text{ Sin } \omega t \text{ Cos } \theta$

Where θ is the angle of the synchro shaft.

If the unit is a Resolver to Digital Converter, the 4 wire resolver output will be connected to S1, S2, S3 and S4 on the module and the microtransformers will act purely as isolators.

To understand the conversion process, assume that the current word state of the up-down counter is ϕ.

Then V_1 is multiplied by Cos ϕ and V_2 is multiplied by Sin ϕ to give:

$K E_O \text{ Sin } \omega t \text{ Sin } \theta \text{ Cos } \phi$

and

$K E_O \text{ Sin } \omega t \text{ Cos } \theta \text{ Sin } \phi$

These signals are subtracted by the error amplifier to give:

$K E_O \text{ Sin } \omega t \text{ (Sin } \theta \text{ Cos } \phi - \text{Cos } \theta \text{ Sin } \phi)$

or

$K E_O \text{ Sin } \omega t \text{ Sin } (\theta - \phi)$

A phase sensitive detector, integrator and voltage controlled oscillator (VCO) form a closed loop system which seeks to null Sin $(\theta - \phi)$.

When this is accomplished, the word state of the up-down counter (ϕ) equals, within the rated accuracy of the converter, the synchro shaft angle θ.

Assuming that the "$\overline{\text{INHIBIT}}$" is at a logic high state, then the digital word ϕ will be strobed into the latches 150ns after the up-down counter has been updated. If the three state "$\overline{\text{ENABLE}}$" is at a logic low, then the digital output word will be presented to the output pins of the module.

DATA TRANSFER

Data transfer from the SDC1725 and SDC1726 is very straightforward.

Consider the timing sequence shown in the timing diagram which assumes that the input to the converter is changing.

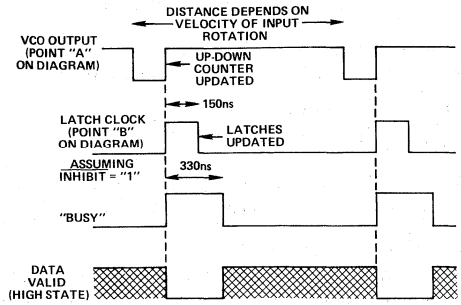
From this diagram, it can be seen that there are two ways to transfer data.

One method is to detect the state of the BUSY signal, which is high for 330ns while the up-down counters and latches are settling, and transfer data when it is in a low state.

However, a much more satisfactory method is to use the "$\overline{\text{INHIBIT}}$" input. As can be seen from the functional diagram application of the "$\overline{\text{INHIBIT}}$" prevents the two monostables being triggered and consequently the latches being updated. Therefore, it follows that data will always be valid from 330ns after the $\overline{\text{INHIBIT}}$ has been taken to a logic low state. It can also be seen that this method of data transfer is valid regardless of when the $\overline{\text{INHIBIT}}$ is applied.

The three-state $\overline{\text{ENABLE}}$ can be used at any time in order to present the data in the latches to the output pins. A logic low on this pin will cause the data to be presented to the outputs.

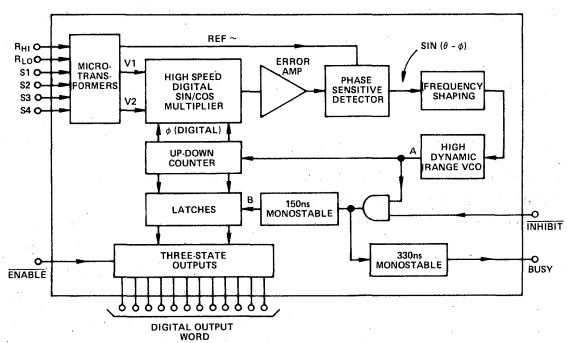
Note that the operation of the internal converter loop cannot be affected in any way by the logic state present on the $\overline{\text{INHIBIT}}$ and $\overline{\text{ENABLE}}$ pins.



Timing Diagram

Bit Number	Weight in Degrees
1	180.0000
2	90.0000
3	45.0000
4	22.5000
5	11.2500
6	5.6250
7	2.8125
8	1.4063
9	0.7031
10 (LSB - SDC1726)	0.3516
11	0.1758
12 (LSB - SDC1725)	0.0879

Bit Weight Table



Functional Diagram SDC1725

CONNECTING THE CONVERTER

The electrical connections to the converter are straightforward. The power lines, which must not be reversed, should be connected to the "+15V", "-15V" and "+5V" pins with the common connection to the ground pin "GND". It is suggested that a parallel combination of a 0.1μF and a 6.8μF capacitor is placed in each of the three positions from "+15V" to "GND", from "-15V" to "GND" and from "+5V" to "GND".

The digital output is taken from pins:

"1" through to "10" for the SDC1726

"1" through to "12" for the SDC1725

Pin "1" represents the MSB in each case.

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The reference connections are made to "R_{HI}" and "R_{LO}".

In the case of a Synchro the signals are connected to "S1", "S2" and "S3" according to the following convention:

$$E_{S1-S3} = E_{RLO-RHI} \sin \omega t \sin \theta$$
$$E_{S3-S2} = E_{RLO-RHI} \sin \omega t \sin (\theta + 120^\circ)$$
$$E_{S2-S1} = E_{RLO-RHI} \sin \omega t \sin (\theta + 240^\circ)$$

For a resolver, the signals are connected to "S1", "S2", "S3" and "S4" according to the following convention:

$$E_{S1-S3} = E_{RLO-RHI} \sin \omega t \sin \theta$$
$$E_{S2-S4} = E_{RHI-RLO} \sin \omega t \cos \theta$$

The "BUSY", "$\overline{\text{INHIBIT}}$" and "$\overline{\text{ENABLE}}$" pins should be connected as described under the heading "Data Transfer".

RESISTIVE SCALING OF INPUTS

A feature of this range of converters is that the signal and reference inputs can be resistively scaled to accommodate any range of input signal and reference voltages.

This means that a standard converter can be used with a personality card in systems where a wide range of input and reference voltages are encountered.

To calculate the values of the external scaling resistors in the case of a Synchro Converter, add 1.11kΩ per extra volt of signal in series with "S1", "S2" and "S3", and 2.2kΩ per extra volt of reference in series with "R_{HI}".

In the case of a Resolver to Digital Converter, add 2.22kΩ in series with "S1" and "S2" per extra volt of signal and 2.2kΩ per extra volt of reference in series with "R_{HI}".

For example, assume that we have an 11.8V line to line, 26V reference Synchro Converter, and we wish to use it with a 60V line to line signal with a 115V reference.

In each signal input line, the extra voltage capability required is:

$$60 - 11.8 = 48.2V$$

Therefore each one of the three resistors needs to have a value of:

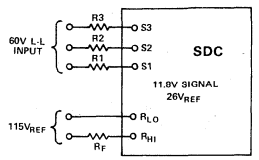
$$48.2 \times 1.11 = 53.5k\Omega$$

Similarly the single resistor needed in series with "R_{HI}" can be calculated as being 195.8kΩ.

The inputs of the converter can therefore be scaled as in the diagram below.

USING THE CONVERTERS WITH OTHER THAN THE SPECIFIED REFERENCE FREQUENCY

A 60Hz converter can be used from 50Hz to 400Hz, and a 400Hz converter can be used from 400Hz up to 2.6kHz, but they will have the dynamic characteristics specified for the unit concerned.



R1, R2, R3 = 53.5kΩ
R_F = 195.8kΩ

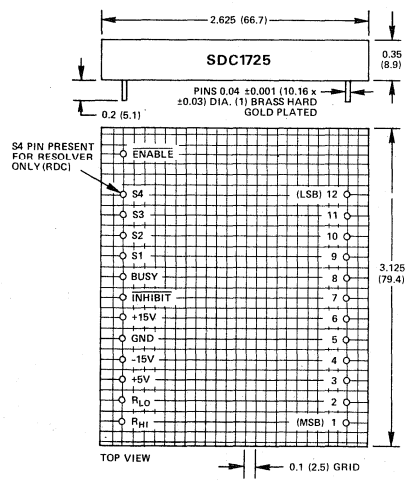
NOTE
IN THE CASE OF THE SIGNAL RESISTORS THE RATIO ERRORS BETWEEN THE RESISTANCES IS MORE IMPORTANT THAN THE ABSOLUTE RESISTANCE VALUES.

IN GENERAL A 1% RATIO ERROR WILL GIVE RISE TO AN EXTRA INACCURACY OF 17 ARC-MINUTES WHILE A RATIO ERROR OF 0.1% WILL GIVE RISE TO AN EXTRA INACCURACY OF 1.7 ARC-MINUTES.

THE ABSOLUTE VALUE OF R_F IS NOT CRITICAL.

OUTLINE DIMENSIONS AND PIN CONNECTION DIAGRAM

Dimensions shown in inches and (mm).



NOTE
THE ABOVE DIAGRAM SHOWS THE CONNECTIONS FOR THE SDC1725. ON THE SDC1726, PINS 11 AND 12 ARE OMITTED AND PIN 10 IS THE LSB.

MATING SOCKET: CAMBION 450-3388-01-03

ORDERING INFORMATION

When ordering, the converter part numbers should be suffixed by an option code in order to fully define them. All the standard options and their option codes are shown below. For options not shown, please consult the factory.

Part Number	Resolution	Operating Temp. Range	L to L Voltage/Format	Ref. Voltage	Ref. Freq.
SDC1725511	12 Bits	0 to +70°C	11.8V Synchro	26 Volts	400Hz
SDC1725611	12 Bits	-55°C to +105°C	11.8V Synchro	26 Volts	400Hz
SDC1725512	12 Bits	0 to +70°C	90.0V Synchro	115 Volts	400Hz
SDC1725612	12 Bits	-55°C to +105°C	90.0V Synchro	115 Volts	400Hz
RDC1725518	12 Bits	0 to +70°C	11.8V Resolver	26 Volts	400Hz
RDC1725618	12 Bits	-55°C to +105°C	11.8V Resolver	26 Volts	400Hz
SDC1725522	12 Bits	0 to +70°C	90.0V Synchro	115 Volts	60Hz
SDC1725622	12 Bits	-55°C to +105°C	90.0V Synchro	115 Volts	60Hz
SDC1725541	12 Bits	0 to +70°C	11.8V Synchro	26 Volts	2.6kHz
SDC1725641	12 Bits	-55°C to +105°C	11.8V Synchro	26 Volts	2.6kHz
RDC1725548	12 Bits	0 to +70°C	11.8V Resolver	26 Volts	2.6kHz
RDC1725648	12 Bits	-55°C to +105°C	11.8V Resolver	26 Volts	2.6kHz

NOTE
For 10-bit resolution, substitute 1726 in place of 1725 in the part number above.

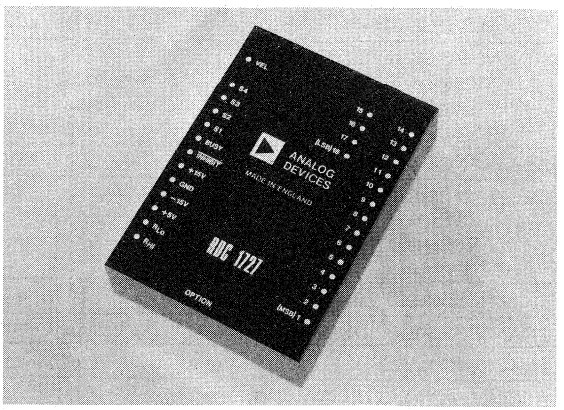
ANALOG DEVICES

18-Bit Synchro/ Resolver to Digital Converter

SDC/RDC 1727

FEATURES

- **High Accuracy (±19.8 arc-seconds Over Full Temperature Range)**
- **High Resolution (18 Bits)**
- **Compatible with Most Synchro and Resolver Transmitters**
- **Industry Standard Pin-Out**
- **DC Output Voltage Proportional to Angular Velocity**
- **Internal Transformers**
- **Mil Spec/High Rel Versions Available**
- **Meets MIL-STD-202E Requirements**
- **Design Incorporates Reference Synthesizer which Eliminates Errors Due to Signal to Reference Phase Shift**



APPLICATIONS

Very high accuracy angular measurement systems. For example gun sights, stabilized platforms and fire control systems.

GENERAL DESCRIPTION

The SDC1727 and RDC1727 are very high accuracy, high resolution synchro and resolver to digital converters. They work on a type 2 tracking principle which ensures that nonstale data with zero velocity lag error is available for input rotational velocities of up to 720°/sec.

They are intended for use with high accuracy synchros and resolvers in order to provide an alternative to two speed (coarse/fine) synchro and resolver systems. The SDC1727 or RDC1727 in conjunction with a high accuracy synchro or resolver provides an angular measurement system which can often be comparable in accuracy and has none of the wear problems associated with coarse/fine mechanical gearing.

The converters are compatible with most resolver and synchro transmitters operating on either 400Hz or 1000Hz reference systems.

All of the converters are internally transformer isolated on both the signal and reference inputs and an output is available which provides a dc voltage proportional to velocity.

The pin-out configuration of the converters is such that it is compatible with other synchro and resolver to digital converters apart from the addition of the extra pins for the increased resolution.

An outstanding feature of the converters is that due to the unique ratiometric technique employed in the design, they have a very low variation in accuracy with temperature, changes in power supply levels, reference and signal voltages and the reference frequency (see note 1 on Specifications page).

The converter design incorporates a reference synthesizer circuit which eliminates errors due to phase shifts of up to 45° between the signal and reference waveforms at tracking rates of up to 720°/sec.

MODELS AVAILABLE

The SDC1727XYZ is available for synchro inputs and the RDC1727XYZ is available for resolver inputs.

The XYZ code defines the option thus:

X specifies the operating temperature range, i.e., Commercial (0 to +70°C) or extended (−55°C to +105°C).

Y specifies the reference frequency.

Z specifies the signal and reference input voltages.

See "Ordering Information."

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SPECIFICATIONS (typical @ +25°C unless otherwise stated)

Model	SDC/RDC1727
ACCURACY[1]	±19.8 arc-seconds max
RESOLUTION	18 Bits (1LSB = 4.94 arc-seconds)
OUTPUT	18 Bits, Parallel Natural Binary with MSB = 180°
SIGNAL AND REFERENCE FREQUENCY	400Hz or 1000Hz
SIGNAL VOLTAGE	11.8V, 26V or 90V rms
SIGNAL INPUT IMPEDANCE	
11.8V Signal	26kΩ
26V Signal	58kΩ
90V Signal	200kΩ
REFERENCE VOLTAGE	11.8V, 26V or 115V rms
REFERENCE INPUT IMPEDANCE	
11.8V Reference	27kΩ
26V Reference	56kΩ
115V Reference	270kΩ
SIGNAL TO REFERENCE PHASE SHIFT	±45° Degrees Gives No Additional Error up to 720°/sec
TRANSFORMER ISOLATION	500V dc
TRACKING RATE	720°/sec max
ACCELERATION CONSTANT (K_a)	
400Hz Options	10,000/sec^2
1000Hz Options	23,000/sec^2
STEP RESPONSE FOR 179° STEP INPUT	600ms for 1LSB (4.94 arc-seconds) Additional Error
POWER LINES	
	+15V @ 60mA max
	-15V @ 60mA max
	+5V @ 240mA max
POWER DISSIPATION	3 Watts max
DATA LOGIC OUTPUT DRIVE[2]	2TTL Load max
BUSY LOGIC OUTPUT DRIVE	1TTL Load max
BUSY OUTPUT PULSE WIDTH	0.5μs max
INHIBIT INPUT (To Inhibit)	Logic "Lo"
INHIBIT INPUT LOADING	1TTL Load max
TEMPERATURE RANGE	
Operating	0 to +70°C (Commercial)
	-55°C to +105°C (Extended)
Storage	-55°C to +125°C
DIMENSIONS	3.5" X 2.5" X 0.875"
	(63.5 X 88.9 X 22.2mm)
WEIGHT	7 ozs (200 grams)

NOTES:

[1] The accuracy is specified over the following: (a) ±10% signal and reference amplitude variation (b) 10% signal and reference harmonic distortion (c) ±5% power supply variation (d) ±10% reference frequency variation (e) signal to reference waveform phase shifts of up to 45° (f) tracking rates of up to 720°/sec.

[2] The outputs are from Low power Schottky counters and should be buffered for distances greater than 6".

Specifications subject to change without notice.

THEORY OF OPERATION

If the unit is a synchro to digital converter, then the 3 wire synchro output will be connected to S1, S2 and S3 on the module and a Scott T transformer pair will convert these signals into resolver format:

i.e., $V_1 = K E_O \text{ Sin } \omega t \text{ Sin } \theta$

and $V_2 = K E_O \text{ Sin } \omega t \text{ Cos } \theta$

where θ is the angle of the synchro shaft.

If the unit is a resolver to digital converter, then the 4 wire resolver output will be connected to S1, S2, S3 and S4 on the module and the signal input transformers will act purely in an isolation mode.

To understand the conversion process, assume that the current word state of the up-down counter is ϕ.

V1 is multiplied by Cos ϕ and V2 is multiplied by Sin ϕ to give:

$K E_O \text{ Sin } \omega t \text{ Sin } \theta \text{ Cos } \phi$

and $K E_O \text{ Sin } \omega t \text{ Cos } \theta \text{ Sin } \phi$

These signals are subtracted by the error amplifier to give:

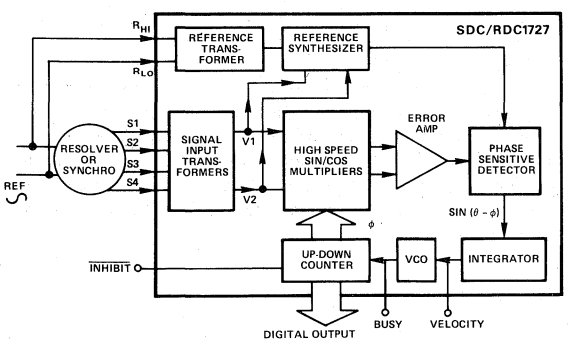
$K E_O \text{ Sin } \omega t \text{ (Sin } \theta \text{ Cos } \phi - \text{Cos } \theta \text{ Sin } \phi)$

or $K E_O \text{ Sin } \omega t \text{ (Sin } (\theta - \phi))$

The reference is fed via input transformers and a reference synthesizer into a phase sensitive detector and the above error signal is demodulated to give Sin $(\theta - \phi)$.

An integrator, a Voltage Controlled Oscillator (VCO) and the up-down counter then form a closed loop system which seeks to null Sin $(\theta - \phi)$.

When this is accomplished, the word state of the up-down counter (ϕ) equals, within the rated accuracy of the converter, the shaft angle θ.



Functional Diagram of the SDC/RDC1727 Converter

CONNECTING THE CONVERTER

The electrical connections to the converter are straightforward. The power lines, which must not be reversed, are ±15V and 5V. They must be connected to the "±15V" and "5V" pins with the common connection to the ground pin GND.

It is suggested that 0.1μF and 6.8μF capacitors be placed in parallel from +15V to GND, from −15V to GND and from +5V to GND.

The digital output is taken from pins 1 through 18 where pin 1 represents the Most Significant Bit (MSB) and pin 18 the Least Significant Bit (LSB).

It is important that buffers should be used on the digital output if it is required to drive distances of greater than six inches. This is because the output is taken directly from the up-down counter which is Low Power Schottky.

The reference connections are made to pins R_{HI} and R_{LO}.

In the case of a Synchro, the signals are connected to "S1", "S2" and "S3" according to the following convention:

$$E_{S1-S3} = E_{RLO-RHI} \text{ Sin } \omega t \text{ Sin } \theta$$
$$E_{S3-S2} = E_{RLO-RHI} \text{ Sin } \omega t \text{ Sin } (\theta + 120^\circ)$$
$$E_{S2-S1} = E_{RLO-RHI} \text{ Sin } \omega t \text{ Sin } (\theta + 240^\circ)$$

For a resolver, the signals are connected to "S1", "S2", "S3" and "S4" according to the following convention:

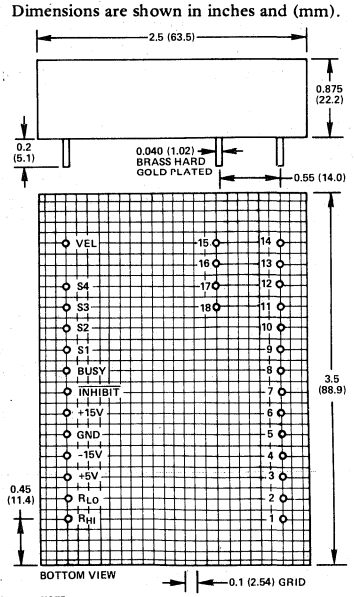
$$E_{S1-S3} = E_{RLO-RHI} \text{ Sin } \omega t \text{ Sin } \theta$$
$$E_{S2-S4} = E_{RHI-RLO} \text{ Sin } \omega t \text{ Cos } \theta$$

The analog voltage representing velocity is available between "VEL" and "GND".

The "BUSY" and "INHIBIT" pin (if used), should be connected as described under the heading "Data Transfer".

OUTLINE DIMENSIONS AND PIN CONNECTION DIAGRAM

Dimensions are shown in inches and (mm).



NOTE
1. S4 PIN PRESENT ON RDC1727 ONLY.

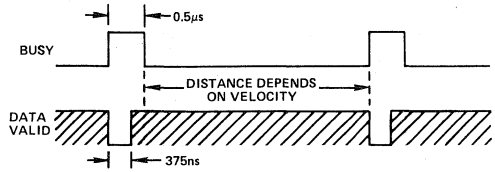
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DATA TRANSFER

The readiness of the converters for data transfer is indicated by the state of the BUSY pin.

The voltage appearing on the BUSY pin consists of a train of pulses, at TTL levels, of width 0.5 microseconds (see Specifications table). The converter is busy when the BUSY pin is at a TTL "High" level. These pulses correspond to those delivered by the VCO to increment or decrement the up-down counter (see schematic diagram). Thus the pulses will occur for increasing and decreasing counts.

The most suitable time for transferring data is when the BUSY is at a logic "Lo" state, and the time allowable for data transfer will depend on the input rotational speed. I.E., at 720°/sec (2 RPS), 2 X 262144 BUSY pulses will occur per second. ($262144 = 2^{18}$.) Note that data is solid coincident with the high to low transition of BUSY.



Data Transfer Diagram

Taking the INHIBIT to a logic "Lo" state prevents the VCO (BUSY) pulses from updating the up-down counter. However, if applied during a BUSY pulse, the INHIBIT will not become effective until the end of the BUSY pulse.

The best method of transferring the data is by applying the INHIBIT (taking it to a logic "Lo" state), waiting for at least the width of a BUSY pulse, transferring the data and releasing the INHIBIT.

Note that sustained application of the INHIBIT opens the internal control loop and the converter may take on appreciable time to recover to full accuracy when the loop is restored.

TRANSFER FUNCTION

400Hz Options

$$\frac{\theta_0}{\theta_1} = \frac{6.21 \times 10^6 (1 + 1.80 \times 10^{-2} s)}{s^3 + 6.10 \times 10^2 s^2 + 1.12 \times 10^5 s + 6.21 \times 10^6}$$

1000Hz Options

$$\frac{\theta_0}{\theta_1} = \frac{2.11 \times 10^7 (1 + 1.2 \times 10^{-2} s)}{s^3 + 9.17 \times 10^2 s^2 + 2.53 \times 10^5 s + 2.11 \times 10^7}$$

VELOCITY PIN

This pin provides a voltage output which is proportional to the angular velocity of the input. The voltage goes negative for an increasing digital angle and goes positive for a decreasing digital angle.

The characteristics of the velocity pin output are given in the table below.

Scaling of Output Voltage for One Fifth max Velocity	2 Volts (Nominal)
Output Voltage Temp. Coeff.	0.05%/°C of Output
Output Voltage Drift	0 to +70°C Options ±50μV/°C −55°C to +105°C Options ±100μV/°C
Linearity:	0°/sec to ±60°/sec 2%
Offset:	5mV max
Noise: (0 to 20Hz)	@ 60°/sec 2mV rms
Impedance (Output)	1Ω
Max Current Available	1mA

The velocity voltage can be used in closed loop servo systems for stabilization instead of a tachometer.

BIT WEIGHT TABLE

Bit Number	Weight in Degrees	Bit Number	Weight in Degrees
1 (MSB)	180.00000	10	0.35156
2	90.00000	11	0.17578
3	45.00000	12	0.08789
4	22.50000	13	0.04395
5	11.25000	14	0.02197
6	5.62500	15	0.01099
7	2.81250	16	0.00549
8	1.40625	17	0.00275
9	0.70313	18 (LSB)	0.00137

OTHER PRODUCTS

The SDC/RDC1727 is just one of the modules and instruments concerned with Synchro and Resolver conversion manufactured by us. Full technical data and applications literature is available for all products. If you have any questions about our products or require advice about the use of them for a particular application, please contact our Applications Engineering Department.

ORDERING INFORMATION

When ordering please use the XYZ option code as defined below to fully specify the part number.

SDC1727XYZ

SDC = Synchro to Digital Converter
RDC = Resolver to Digital Converter

Z = 1 Signal	11.8V	Reference	26V	Synchro
Z = 2 Signal	90V	Reference	115V	Synchro
Z = 3 Signal	11.8V	Reference	11.8V	Resolver
Z = 4 Signal	26V	Reference	26V	Resolver
Z = 8 Signal	11.8V	Reference	26V	Resolver

X = 5 0 to +70°C Operating Temperature Range
X = 6 −55°C to +105°C Operating Temperature Range

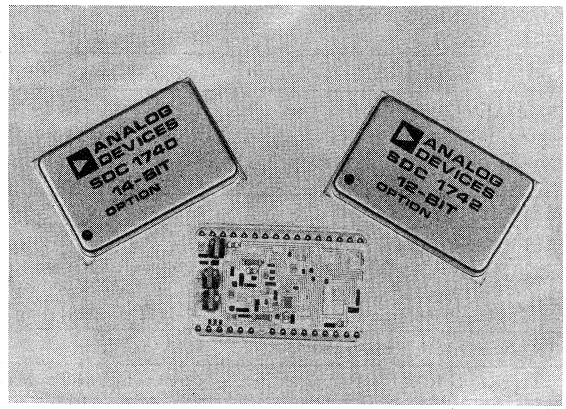
Y = 1 400Hz Reference Frequency
Y = 3 1000Hz Reference Frequency

12- and 14-Bit Hybrid Synchro/ Resolver to Digital Converters

SDC/RDC1740/1741/1742

FEATURES
- Internal Isolating Transformers
- 14-Bit or 12-Bit Resolution
- Three Accuracy Options
- Three-State Latched Output
- Continuous Tracking – Even During Data Transfer
- Simple Data Transfer
- Laser Trimmed – No External Adjustments
- MIL Spec/Hi Rel Options Available
- Hermetically Sealed

APPLICATIONS
- Avionic Systems
- Servo Mechanisms
- Coordinate Conversion
- Axis Transformation
- Antenna Monitoring
- Artillery Fire Control Systems
- Engine Controllers



GENERAL DESCRIPTION

The SDC1740, SDC1741 and SDC1742 are hybrid, continuous tracking synchro or resolver to digital converters which employ a type 2 servo loop and contain three-state latches on the digital outputs.

The input signals can either be 3 wire synchro plus reference or 4 wire resolver format plus reference depending on the option; and the outputs are presented in TTL compatible parallel natural binary buffered by three-state latches.

The three state output facility, which has separate $\overline{\text{ENABLE}}$ inputs for the most significant 8 bits and the least significant 4 bits (or 6 bits in the case of the SDC1740), not only simplifies multiplexing of more than one device onto a single data bus, but also enables the $\overline{\text{INHIBIT}}$ to be used without opening the internal converter loop.

An outstanding feature of these converters is that although the profile height is only 0.28 inches (7.1mm) they contain internal transformers which provide for true isolation on the signal and reference inputs.

The converters are hermetically sealed in a metal 32-pin dual in line package.

To ensure a level of reliability consistent with the performance, each converter receives a stringent pre-cap visual inspection, high temperature storage and temperature cycling, fine and gross leak testing, acceleration testing and operating burn-in.

The converters are also available processed in accordance with MIL-STD-883, Method 5008, Class B.

MODELS AVAILABLE

The three synchro/resolver to digital converters described in this data sheet differ primarily in the areas of resolution, accuracy and dynamic performance as follows:

Model SDC1740XYZ is a 14-bit converter with an overall accuracy of ±4 arc-minutes and a resolution of 1.3 arc-minutes.

Model SDC1741XYZ is a 12-bit converter with an accuracy of ±15.3 arc-minutes and a resolution of 5.3 arc-minutes.

Model SDC1742XYZ is a 12-bit converter with an accuracy of ±8.5 arc-minutes and a resolution of 5.3 arc-minutes.

The XYZ code defines the option as follows: (X) signifies the operating temperature range, (Y) signifies the reference frequency, (Z) signifies the signal and reference voltage and whether it will accept synchro or resolver format.

More information about the option code is given under the heading of "Ordering Information".

THEORY OF OPERATION

If the unit is a Synchro to Digital Converter the 3 wire synchro output will be connected to S1, S2 and S3 on the unit and the Scott T transformer pair will convert these signals into resolver format.

i.e., $V_1 = K E_O \text{ Sin } \omega t \text{ Sin } \theta$

$V_2 = K E_O \text{ Sin } \omega t \text{ Cos } \theta$

Where θ is the angle of the synchro shaft.

SPECIFICATIONS (typical @ +25°C unless otherwise specified)

Models	SDC/RDC1742	SDC/RDC1741	SDC/RDC1740
ACCURACY[1] (Max Error on all Options)	±8.5 arc-minutes	±15.3 arc-minutes	±4 arc-minutes
RESOLUTION	12 Bits (1LSB = 5.3 arc-minutes)	*	14 Bits (1LSB = 1.3 arc-minutes)
OUTPUT	12 Bits Parallel Natural Binary	*	14 Bits Parallel Natural Binary
SIGNAL AND REFERENCE FREQUENCY	400Hz or 2.6kHz	*	*
SIGNAL VOLTAGE (Line to Line)	90V, 26V or 11.8V rms	*	*
SIGNAL IMPEDANCE			
90 Volt Signal	200kΩ (Resistive)	*	*
26V Signal	57.7kΩ (Resistive)	*	*
11.8V Volt Signal	26kΩ (Resistive)	*	*
REFERENCE VOLTAGE	115V, 26V or 11.8V rms	*	*
REFERENCE IMPEDANCE			
115 Volt Reference	120kΩ (Resistive)	*	*
26 Volt Reference	27kΩ (Resistive)	*	*
11.8 Volt Reference	12.3kΩ (Resistive)	*	*
TRANSFORMER ISOLATION	350V dc	*	*
TRACKING RATE (Minimum)	18 Revolutions Per Second	*	12 Revolutions Per Second
ACCELERATION Constant K_a	66,000/sec^2	*	36,000/sec^2
STEP RESPONSE (179° Step for Settling to 1LSB of Error)	150ms	*	*
POWER LINES			
+15V	19mA (typ) 23mA (max)	*	23mA (typ) 30mA (max)
-15V	19mA (typ) 23mA (max)	*	23mA (typ) 30mA (max)
+5V	45mA (typ) 110mA (max)	*	150mA (typ) 180mA (max)
POWER DISSIPATION	0.8 Watts (typ) 1.3 Watts (max)	*	1.44 Watts (typ) 1.8 Watts (max)
DATA LOGIC OUTPUTS[2]	6TTL Loads	*	*
BUSY LOGIC OUTPUT LOADING[2]	2TTL Loads	*	*
BUSY LOGIC OUTPUT WIDTH	3μs (max)	*	*
$\overline{\text{INHIBIT}}$ INPUT (TO INHIBIT)	Logic "0" 1TTL Load	*	*
$\overline{\text{ENABLE}}$ INPUTS (TO ENABLE)[3]	Logic "0" 1TTL Load	*	*
TEMPERATURE RANGE			
Operating	-55°C to +125°C	*	*
Storage	-65°C to +150°C	*	*
DIMENSIONS	1.74" X 1.14" X 0.28" (44.2 X 28.9 X 7.1mm)	* *	* *
WEIGHT	0.8 ozs (23 G)	*	*

*Specifications the same as for SDC/RDC1742.

NOTES
[1] Specified over the appropriate operating temperature range and for: (a) ±10% signal and reference amplitude variation; (b) 10% signal and reference harmonic distortion; (c) ±5% power supply variation; and (d) ±10% variation in reference frequency.
[2] Schottky logic loading rules apply.
[3] $\overline{\text{ENABLE M}}$ enable most significant 8 bits.
$\overline{\text{ENABLE L}}$ enable least significant 4 bits (or 6 bits for the SDC/RDC1740).

Specifications subject to change without notice.

If the unit is a Resolver to Digital Converter, the 4 wire resolver output will be connected to S1, S2, S3 and S4 on the unit and the transformers will act purely as isolators.

To understand the conversion process, assume that the current word state of the up-down counter is ϕ.

Then V_1 is multiplied by Cos ϕ and V_2 is multiplied by Sin ϕ to give:

$$K E_O \text{ Sin } \omega t \text{ Sin } \theta \text{ Cos } \phi$$

and

$$K E_O \text{ Sin } \omega t \text{ Cos } \theta \text{ Sin } \phi$$

These signals are subtracted by the error amplifier to give:

$$K E_O \text{ Sin } \omega t \text{ (Sin } \theta \text{ Cos } \phi - \text{Cos } \theta \text{ Sin } \phi)$$

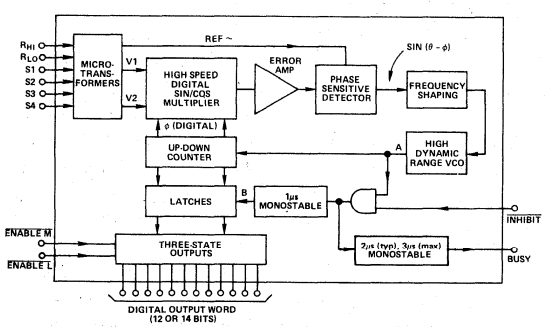
or

$$K E_O \text{ Sin } \omega t \text{ Sin } (\theta - \phi)$$

A phase sensitive detector, integrator and voltage controlled oscillator (VCO) form a closed loop system which seeks to null Sin $(\theta - \phi)$.

When this is accomplished, the word state of the up-down counter (ϕ) equals, within the rated accuracy of the converter, the synchro shaft angle θ.

Assuming that the "$\overline{\text{INHIBIT}}$" is at a logic high state, then the digital word ϕ will be strobed into the latches 1μs after the up-down counter has been updated. If the three state "$\overline{\text{ENABLE}}$" is at a logic low, then the digital output word will be presented to the output pins of the unit.



Functional Diagram of the SDC/RDC1740, SDC/RDC1741 and the SDC/RDC1742

DATA TRANSFER

Data transfer from the converters is straightforward.

Consider the timing sequence shown in the timing diagram which assumes that the input to the converter is changing.

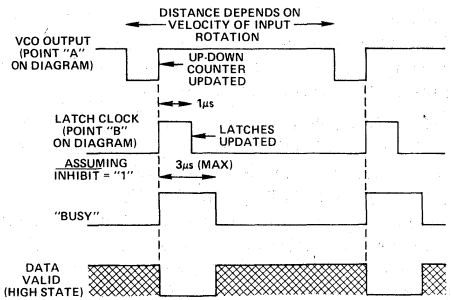
From this diagram, it can be seen that there are two ways to transfer data.

One method is to detect the state of the BUSY signal, which is high for up to 2.0 microseconds (typical) while the up-down counters and latches are settling, and transfer data when it is in a low state.

An alternative method is to use the "$\overline{\text{INHIBIT}}$" input. As can be seen from the functional diagram, application of the "$\overline{\text{INHIBIT}}$" prevents the two monostables being triggered and consequently the latches being updated. Therefore, it follows that data will always be valid after 3μs has elapsed from the application of the $\overline{\text{INHIBIT}}$ (i.e. taken to logic low). It can also be seen that this method of data transfer is valid regardless of when the $\overline{\text{INHIBIT}}$ is applied.

The three-state $\overline{\text{ENABLE}}$ can be used at any time in order to present the data in the latches to the output pins. $\overline{\text{ENABLE M}}$ enables the most significant 8 bits while $\overline{\text{ENABLE L}}$ enables the least significant 4 bits (6 bits in the SDC/RDC1740).

Note that the operation of the internal converter loop cannot be affected in any way by the logic state present on the $\overline{\text{INHIBIT}}$ and $\overline{\text{ENABLE}}$ pins.



Timing Diagram

Bit Number	Weight in Degrees
1 (MSB)	180.0000
2	90.0000
3	45.0000
4	22.5000
5	11.2500
6	5.6250
7	2.8125
8	1.4063
9	0.7031
10	0.3516
11	0.1758
12 (LSB) For 1741/1742	0.0879
13	0.0439
14 (LSB For 1740	0.0220

Bit Weight Table

CONNECTING THE CONVERTER

The electrical connections to the converter are straightforward. The power lines, which must not be reversed, should be connected to the "+15V", "-15V" and "+5V" pins with the common connection to the ground pin "GND". It is suggested that a parallel combination of a 0.1μF and a 6.8μF capacitor is placed in each of the three positions from "+15V" to "GND", from "-15V" to "GND" and from "+5V" to "GND".

The pin marked "case" is connected electrically to the case and should be taken to a convenient zero volt potential in the system.

The digital output is taken from Pin "1" through to "12" for the SDC/RDC1742 and SDC/RDC1741 and "1" through to "14" for the SDC/RDC1740, where Pin "1" is the MSB.

The reference connections are made to "R_{HI}" and "R_{LO}".

In the case of a Synchro, the signals are connected to "S1", "S2" and "S3" according to the following convention:

$$E_{S1-S3} = E_{RLO-RHI} \text{ Sin } \omega t \text{ Sin } \theta$$

$$E_{S3-S2} = E_{RLO-RHI} \text{ Sin } \omega t \text{ Sin } (\theta + 120^\circ)$$

$$E_{S2-S1} = E_{RLO-RHI} \text{ Sin } \omega t \text{ Sin } (\theta + 240^\circ)$$

For a resolver, the signals are connected to "S1", "S2", "S3" and "S4" according to the following convention:

$E_{S1-S3} = E_{RLO-RHI} \sin \omega t \sin \theta$

$E_{S2-S4} = E_{RHI-RLO} \sin \omega t \cos \theta$

The "BUSY", "$\overline{\text{INHIBIT}}$" and "$\overline{\text{ENABLE}}$" pins should be connected as described under the heading "Data Transfer".

RESISTIVE SCALING OF INPUTS

A feature of these converters is that the signal and reference inputs can be resistively scaled to accommodate any range of input signal and reference voltages.

This means that a standard converter can be used with a personality card in systems where a wide range of input and reference voltages are encountered.

To calculate the values of the external scaling resistors in the case of a Synchro Converter, add 1.11kΩ per extra volt of signal in series with "S1", "S2" and "S3", and 1kΩ per extra volt of reference in series with "R_{HI}".

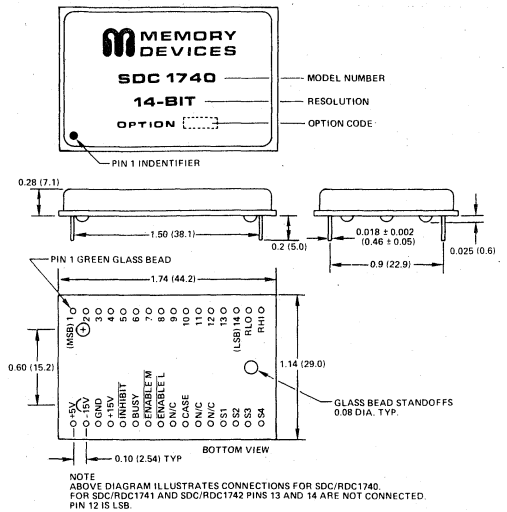
In the case of a Resolver to Digital Converter, add 2.22kΩ in series with "S1" and "S2" per extra volt of signal and 1kΩ per extra volt of reference in series with "R_{HI}".

MEAN TIME BETWEEN FAILURES (MTBF)

The reliability of these products is very high due to the extensive use of custom chip circuitry. For details of MTBF figures under particular conditions please consult the factory.

OUTLINE DIMENSIONS
PACKAGING SPECIFICATIONS

Dimensions shown in inches and (mm).



NOTE
ABOVE DIAGRAM ILLUSTRATES CONNECTIONS FOR SDC/RDC1740.
FOR SDC/RDC1741 AND SDC/RDC1742 PINS 13 AND 14 ARE NOT CONNECTED.
PIN 12 IS LSB.

PROCESSING FOR HIGH RELIABILITY

STANDARD PROCESSING

As part of the standard manufacturing procedure, all converters receive the following processing:

PROCESS	CONDITIONS
1. Pre-Cap Visual Inspection	In-House Criteria to manufacturing spec. MD4-6
2. Stabilization Bake	10 cycles, -65°C to +150°C
3. Temperature Cycling	5000G
4. Constant Acceleration	160 hours @ +125°C
5. Operating Burn-In	In-House Criteria to manufacturing spec. MD5-2
6. Seal Test, Fine and Gross	Performed at 25°C
7. Final Electrical Test	

PROCESSING TO MIL-STD-883

All models ordered to the requirements of MIL-STD-883, Method 5008, Class B are identified with a /883B suffix, and receive the following processing:

1. Pre-Cap Visual Inspection	2017
2. Stabilization Bake	1008, 24 hours @ +150°C
3. Temperature Cycling	1010, Test Condition C, 10 cycles, -65°C to +150°C
4. Constant Acceleration	2001, Y_1 plane, 5000G
5. Seal Test, Fine and Gross	1014, Test Condition A and C
6. Operating Burn-In	1015, Test Condition B, 160 hours @ +125°C
7. Final Electrical Testing	Performed at max and min operating temperatures
8. External Visual Inspection	2009

ORDERING INFORMATION

When ordering, the converter part numbers should be suffixed by an option code in order to fully define them. All the standard options and their option codes are shown below. For options not shown, please consult the factory.

SDC 1740 X Y Z

SDC = Synchro to Digital Converter
RDC = Resolver to Digital Converter

1740 = 14-bit resolution, ±4 arc-min accuracy
1741 = 12-bit resolution, ±15.3 arc-min accuracy
1742 = 12-bit resolution, ±8.5 arc-min accuracy

Z = 1	Signal	11.8V	Reference	26V	Synchro
Z = 2	Signal	90V	Reference	115V	Synchro
Z = 3	Signal	11.8V	Reference	11.8V	Resolver
Z = 4	Signal	26V	Reference	26V	Resolver
Z = 8	Signal	11.8V	Reference	26V	Resolver

Y = 1 400Hz Reference Frequency
Y = 4 2.6kHz Reference Frequency

X = 4 -55°C to +125°C Operating Temperature Range

ANALOG DEVICES

Synchro/Resolver Power Amplifier

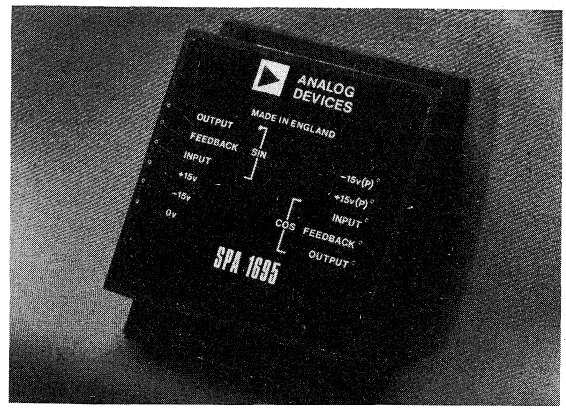
SPA1695

FEATURES

- 5VA Output – Capable of Driving 4 Size 11 CT's
- Indefinite Short Circuit Protection
- Metal Case Acts as Heatsink
- Easily Mounted
- Voltage Sensing Facility
- Operation with No Derating Up to +105°C
- Suitable for 50 to 400Hz Operation

APPLICATIONS

- Can Be Used With the Digital Vector Generators (DTM1716 and DTM1717) to Drive Control Transformers (CT's)



GENERAL DESCRIPTION

The SPA1695 is a two channel amplifier intended for use in conjunction with the DTM1716 and DTM1717 Digital Vector Generators for driving Control Transformers (CT's).

The unit is capable of supplying 5VA to the load and therefore can be used in cases where the internal amplifiers of a Digital to Synchro Converter are not sufficient (i.e., in general when the load exceeds 1.3VA).

The SPA1695 is contained in an aluminium case which has predrilled flanges for mounting purposes and excellent heatsinking properties.

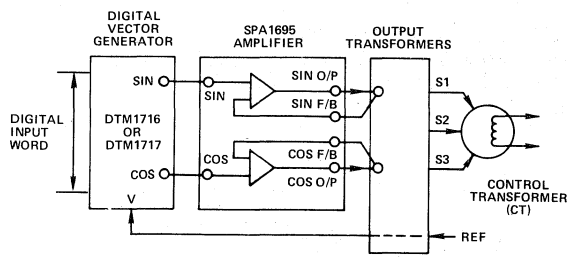
The amplifier has no derating up to +105°C and is indefinitely short circuit protected at 25°C ambient.

The unit accepts resolver format inputs (Sine and Cosine) at 7 volts rms max. The output of the amplifier is in resolver format at 7 volts rms max and should be fed into suitable transformers (see ordering information).

Voltage sensing pins are provided to compensate for any voltage drop which may occur between the output of the amplifier and the output transformer.

MODELS AVAILABLE

The SPA1695 does not require any option numbers in order to fully specify it. The standard unit operates over the frequency range 50 to 400Hz and over the temperature range of -55°C to +105°C.



Implementation of the SPA1695 Amplifier

SCHEMATIC DIAGRAM OF AN SPA1695 AMPLIFIER BEING USED TO DRIVE A CONTROL TRANSFORMER (CT)

The above diagram shows a Digital Vector Generator being used in conjunction with the SPA1695 amplifier and external transformers to drive a Control Transformer.

The diagram illustrates the use of the Sine and Cosine feedback pins ("Sin F/B" and "Cos F/B").

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SPECIFICATIONS (typical at 25°C unless otherwise noted)

POWER OUTPUT[1]	5VA
ACCURACY[2] (between channels)	2 arc-minutes
GAIN ACCURACY[2] (matching)	0.1%
INPUT VOLTAGE (per channel)	7V rms
OPERATING FREQUENCY	50 to 400Hz
INPUT IMPEDANCE	Greater than 50kΩ
INPUT BIAS CURRENT	Less than 1μA
GAIN (per channel)	Unity
INPUT DRIFT	50μV/°C
INITIAL OUTPUT OFFSET	3mV max at 25°C
CROSS OVER DISTORTION	0.01% max
DERATING OF AMPLIFIER	None up to +105°C
POWER SUPPLY REQUIREMENTS:	
±15V(P) No Load	115mA Unregulated
±15V(P) Average Full Load	630mA Unregulated
±15V	15mA Regulated
WEIGHT	275 Grams (9.7 ozs)
SIZE	3.46" x 2.68" x 0.98" (88mm x 68mm x 25mm)
OPERATING TEMERATURE RANGE	-55°C to +105°C
STORAGE TEMPERATURE RANGE	-55°C to +125°C

NOTES:
1. Power output is sufficient to drive four 400Hz 90 volts line to line control transformers.
2. Valid over full temperature range of -55°C to +105°C.

Specifications subject to change without notice.

CONNECTING THE SPA1695

The diagram shows the connection of the SPA1695 to the DTM1716 or DTM1717 Digital Vector Generator, and STM1686 output and reference transformers.

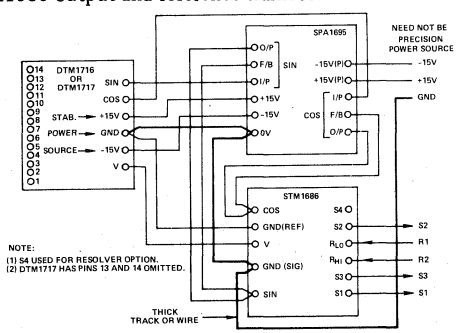


Diagram Showing Connection of the SPA1695 to a DTM1716 or DTM1717 and STM1686

NOTES:
1. The "Sin F/B" and the "Cos F/B" pins of the SPA1695 should be connected directly the the "Sin" and "Cos" terminals on the output transformer at the transformer. This is to compensate for any drop in voltage along the connections between the "Sin O/P" and "Cos O/P" pins of the amplifier and the transformer.
2. The "+15V" and "-15V" pins of the SPA1695 should be connected to a regulated power supply in order to drive the internal operational amplifiers. The "+15V(P)" and "-15V(P)" are used for the output stage and these supplies need not be a precision source. The minimum voltage when considering all tolerances including ripple, should be between 14.75 and 20 volts.
3. The part of the 0 volt system local to the amplifier and converter should be tapped from the "GND(SIG)" pin on the transformer and should not interconnect with any other part of the 0 volt system by any other method (see above diagram).
4. In the above diagram, connection is also shown between the reference transformers, contained in the STM1686 and the Digital Vector Generator.

USING TWO SPA1695 AMPLIFIERS IN PUSH-PULL CONFIGURATION

Twice the output power may be achieved by connecting the outputs from two SPA1695 amplifiers in push-pull configuration, the two devices being fed with out of phase signals.

For more information consult the factory.

ADDITIONAL HEATSINKING

Although the SPA1695 case will provide the necessary heatsink properties to allow the amplifier to provide the 5VA power output over the full temperature range, it is recommended that additional heatsinking be provided where possible.

ORDERING INFORMATION AND TRANSFORMER TYPE

Part number SPA1695 is sufficient to specify the amplifier – no option codes are needed.

The transformers should be ordered according to the following:

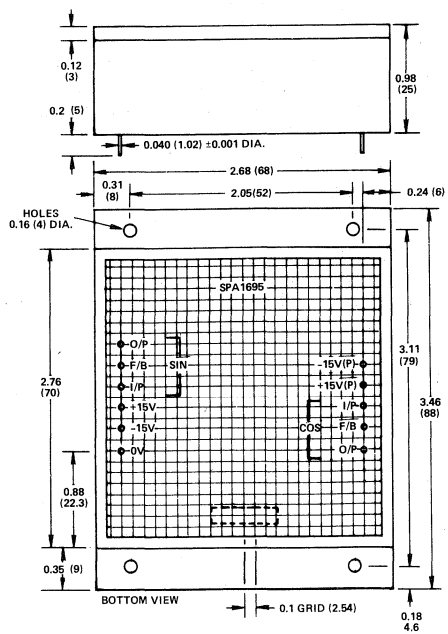
STM1686611	400Hz, Synchro output, 11.8 volt signal, 26 volt reference.
STM1686612	400Hz, Synchro output, 90 volt signal, 115 volt reference.
RTM1686618	400Hz, Resolver output, 11.8 volt signal, 26 volt reference.
STM1687622	50/60Hz, Synchro output, 90 volt signal, 115 volt reference.

NOTES:
1. Above transformers are suitable for use over the temperature range -55°C to +105°C.
2. If it is required to use the SPA1695 with Digital to Resolver converters, then use:
   a. STM1736 for 400HZ and STM1737 for 50/60Hz systems in the case of the DRC1605 and DRC1606 converters.
   b. STM1696 for 400Hz and STM1697 for 50/60Hz systems in the case of the DRC1705 and DRC1706 converters.

AMPLIFIER OUTLINE DIMENSIONS AND PIN CONNECTION DIAGRAM

Dimensions shown in inches and (mm).

MATING SOCKET: CAMBION 450-3388-01-03



Two Speed Processor (for Coarse/Fine Synchro/Resolver Systems)

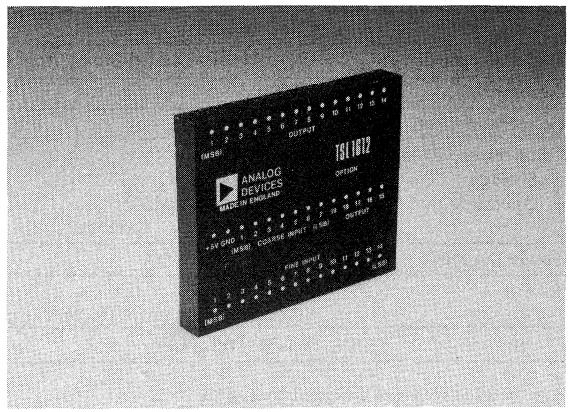
TSL1612

FEATURES

- **36:1, 18:1 or 9:1 Ratios with Same Module**
- **No False Output Readings**
- **Fast (500ns) Parallel Operation**
- **Easy to Use**
- **Up to 19-Bits Resolution**
- **Automatic Correction for Misalignment Between Synchros or Resolvers**
- **Low Profile – 0.4" (10.2mm)**

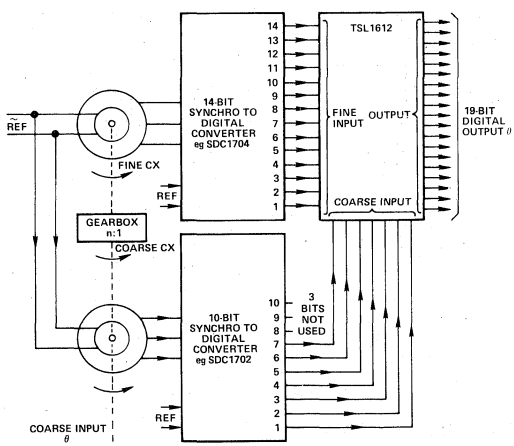
APPLICATIONS

- **Combining the Digital Outputs of Synchro or Resolver to Digital Converters in Coarse/Fine Systems**



GENERAL DESCRIPTION

The TSL1612 is used for combining the digital outputs of two Synchro or Resolver to Digital Converters in a mechanically or electrically geared coarse/fine system in order to produce a single unambiguous digital word representing the coarse shaft angle (see diagram).



DIGITIZING THE OUTPUT OF THE COARSE AND FINE SYNCHRO TRANSMITTERS (CX'S) IN A TWO SPEED SYSTEM

The unit described in this data sheet provides for ratios of 9:1, 18:1 and 36:1 in a single module. However, other ratios are sometimes encountered in coarse/fine Synchro or Resolver Systems, and details of special versions of the TSL1612 for use with ratios of 2:1 thru 35:1 are available on request.

The digital inputs to the TSL1612 are up to 14 bits from the fine converter and up to 7 bits from the coarse converter according to the gear ratio required. The output is up to 19-bits parallel binary angle data. The module may be used with any Synchro or Resolver Converters which produce parallel binary output.

MODELS AVAILABLE

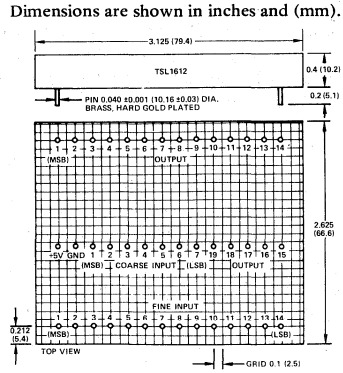
The standard TSL1612 which provides for ratios of 36:1, 18:1 and 9:1 has two options. They are as follows:

TSL1612500	0 to +70°C Operating Temperature
TSL1612600	−55°C to +105°C Operating Temperature

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OUTLINE DIMENSIONS AND PIN CONNECTION DIAGRAM

Dimensions are shown in inches and (mm).



MATING SOCKET: CAMBION 450-3388-01-03

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

Ratios:	36:1, 18:1, 9:1
Fine Synchro Input	Up to 14-Bits Parallel Binary Angle
Coarse Synchro Input	Up to 7-Bits Parallel Binary Angle
Logic Levels	DTL/TTL Compatible
Input Loading	2TTL Loads
Output Fan Out	5TTL Loads
Digital Output	Up to 19-Bits Parallel Binary Angle
Accuracy	±1LSB
Conversion Time	500ns
Temperature Range	
Storage	−55°C to +125°C
Operating	0 to +70°C Standard
	−55°C to +105°C Extended
Power Supplies	+5V ±5% @ 600mA
Size	3.125" X 2.625" X 0.4"
	79.4mm X 66.6mm X 10.2mm
Weight	3.5ozs. 100 grams

Specifications subject to change without notice.

CONNECTING THE TSL1612

For all ratios the fine SDC outputs connect directly to the fine TSL1612 inputs i.e. bit (1) out to bit (1) in through to bit 14 out to bit 14 in. If a Synchro or Resolver to Digital Converter with a resolution of less than 14 bits is used to provide the fine input, then the unused inputs to the TSL1612 should be grounded and the output accuracy will be reduced accordingly by the same number of bits.

The connections of the coarse inputs and the TSL1612 outputs change according to the ratio to be obtained ie:−

36:1 RATIOS

Bits 1 to 7 from the coarse Synchro or Resolver to Digital Converter should be connected to bits 1 to 7 on the coarse input of the TSL1612. The output is taken from bits 1 to 19.

18:1 RATIOS

Bits 1 to 6 from the coarse Synchro or Resolver to Digital Converter should be connected to bits 2 to 7 on the coarse input of the TSL1612. The output is taken from bits 2 to 19 (bit 2 is the MSB of the output word).

9:1 RATIOS

Bits 1 to 5 from the coarse Synchro or Resolver to Digital Converter should be connected to bits 3 to 7 on the coarse input of the TSL1612. The output is taken from bits 3 to 19 (bit 3 is the MSB of the output word).

CORRECTION FOR MISALIGNMENT OF THE COARSE AND FINE SYNCHROS OR RESOLVERS

In the two speed digital converters which receive inputs from both the coarse and fine synchros, circumstances will occur when the coarse angle determined by the most significant digits of fine synchro will conflict with the overlapping least significant digits of the coarse synchro. (This is due to the backlash in the gearing or misalignment in the synchros causing different readings at the major transition points.) Digital logic circuits for resolving this conflict are included in the TSL1612. The digital reading from the fine synchro is made to dominate in the overlapping region, and a correction is made bringing the coarse reading into line to provide an unambiguous digital representation of the angle of the coarse shaft. The TSL1612 will correct for a misalignment of (90 divided by the ratio) degrees.

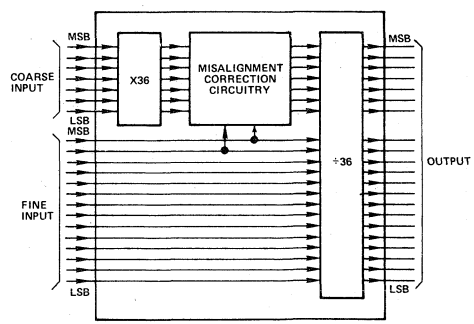
DATA TRANSFER FROM THE TSL1612

Data transfer can be made in a number of ways in which two are listed below.

1. The BUSY outputs of the fine and coarse Synchro/Resolver to Digital Converter can be "OR"ed together to give an indication of when neither converter is being updated (see appropriate converter data sheet). The data can then be taken from the TSL1612. (The conversion time of the TSL1612 is usually insignificant.)
2. The INHIBIT can be applied to both the Synchro/Resolver to Digital Converters simultaneously in order to freeze their outputs (see appropriate data sheet). When the inputs to the TSL1612 are frozen the output data can be taken. In cases where 12 bits is sufficient for the fine input, the three-state input SDC1725 Synchro/Resolver to Digital Converter should be used in conjunction with the SDC1726 on the coarse input. These converters allow the INHIBIT to be used without any risk of opening the internal converter tracking loop (see data sheet).

THEORY OF OPERATION

The theory of operation of the TSL1612 is shown in the diagram below.



FUNCTIONAL DIAGRAM OF TSL1612

ORDERING INFORMATION

Order:−

TSL1612500 for 0 to +70°C Operating Temperature Range.

TSL1612600 for −55°C to +105°C Operating Temperature Range.

Sample/Track-Hold Amplifiers

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THS/THC Modules, Ultra-High-Speed Track-Hold Amplifier Series	14–15

•New product since *1980 Data-Acquisition Components and Subsystems Catalog*

Selection Guide
Sample/Track-Hold Amplifiers

1. GENERAL PURPOSE

Model	Acquisition Time	Characteristics	Vol I Page	Vol II Page
AD583K	4μs to ±0.1% (C = 50pF)	Aperture time 50ns, 10pC charge transfer	14-13	–
AD582K/S	6μs to ±0.1% (C = 100pF)	Aperture time 150ns, nonlinearity ±0.01%, low cost	14-9	–

2. HIGH SPEED

Model	Acquisition Time	Characteristics		
AD346	2μs to ±0.01%	Aperture time 60ns, low droop 0.5mV/μs	14-7	–
ADSHC-85	4.5μs to ±0.01%	Aperture time 25ns, low droop 0.2mV/μs	14-17	–

3. VERY HIGH SPEED

Model	Acquisition Time	Characteristics		
HTS-0025	20ns to 1%	Aperture jitter 20ps, 0.01% nonlinearity	14-23	–
THS-0025	20ns to 1%	Aperture jitter 20ps, 0.01% nonlinearity	–	14-15
THS-0060	75ns to 1%	Aperture jitter 20ps, 0.01% nonlinearity	–	14-15
THS-0225	300ns to 1%	Aperture jitter 20ps, 0.01% nonlinearity	–	14-15
HTC-0300	100ns to 0.1%	Aperture jitter 100ps, max, 0.01% nonlinearity	14-23	–
THC-0300	100ns to 0.1%	Aperture jitter 100ps, max, 0.01% nonlinearity	–	14-15
THC-0750	300ns to 0.1%	Aperture jitter 100ps, max, 0.01% nonlinearity	–	14-15
THC-1500	1000ns to 0.1%	Aperture jitter 100ps, max, 0.01% nonlinearity	–	14-15
ADSHM-5	350ns to 0.01%	Low droop 20μV/μs, 0.005% nonlinearity	14-21	14-7
ADSHM-5K	250ns to 0.01%	Low droop 12μV/μs, 0.005% nonlinearity	14-21	14-7

4. HIGH RESOLUTION

Model	Acquisition Time	Characteristics		
SHA1144	8μs max to 0.003%	Aperture jitter 500ps, gain nonlinearity ±0.001%	14-29	14-11

Orientation
Sample/Track-Hold Amplifiers

The technical data in this volume embrace high-performance (high-resolution and high-speed) sample/track-holds, in the form of encapsulated modules. As the Selection Guide indicates, data on a variety of monolithic and hybrid sample/track-holds can be found in Volume I.

Besides the products in this section (stand-alone devices for performing the sample/track-hold function) similar functions can be found integrated into a variety of component and subsystem products. Component examples: a number of video A/D converters have on-board track-holds (MOD-1205); some high-speed D/A converters have on-board sample-holds for deglitching (MDD); and high-resolution D/A converters have deglitcher options (Deglitcher IV for the DAC1138). Besides these, sample-hold functions are inherent in Data-Acquisition Subsystems, Microcomputer Analog I/O Boards, Intelligent Measurement-and-Control Subsystems, and MACSYM.

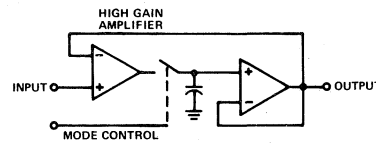
The principal application for sample/track-hold amplifiers is to maintain an analog-to-digital converter's input constant during conversion, at a value representing the analog input as of a certain precisely known time. The characteristics of the SHA are crucial to system accuracy and the reliability of the digital data, especially in 12-bit and/or high-throughput-rate applications.

A sample/track-hold amplifier (s/h or SHA), as its name indicates, has two modes of operation, programmed by a digital control-input. In the *track*– or *sample*–mode, the output follows the input, usually with a gain of +1. When the mode-input switches to *hold*, the output of the SHA ideally retains the last value it had when the command to hold was given, and it retains that value until the logic input dictates *track (sample)*, at which time the output ideally jumps to the input value and follows the input until the next *hold* command is given.

Analog Devices *track-holds* and *sample-holds* are functionally identical; they are designed to acquire input signals for either immediate hold or for a possibly extended period of tracking. They should not be confused with ac devices termed "sample-hold" that can *only* obtain quick samples and cannot track the input continuously.

SHA CIRCUITRY AND HARDWARE

A sample-hold amplifier usually consists of a storage capacitor, input- and output buffer-amplifiers, and a switch and its drive-circuitry. During *sample*, the circuit is connected to promote rapid charging of the capacitor. During *hold,* the capacitor is disconnected from its charging source and–ideally– retains its charge. The figure below shows a typical feedback configuration: the input buffer is a high-gain differential amplifier with a current output that charges the capacitor through the logic-controlled switch. The capacitor is unloaded by a unity-gain buffer-follower. The output is fed back to the negative input (as in an op-amp follower configuration), and thus, in *sample*, the charge on the capacitor is compelled to follow the input. In *hold*, the input amplifier no longer drives the capacitor; it retains its charge, unloaded by the output follower. In another popular configuration, the capacitor is used as the feedback element of an inside-the-loop integrator (SHA1144). The highest-speed devices usually run open-loop.

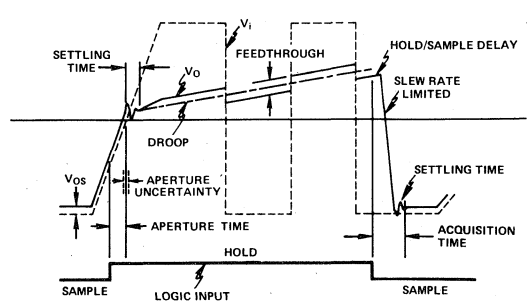


Since drive current is finite, and leakage current in *hold* is not zero, the capacitance–if large–limits the slewing rate in *sample* and–if small–converts leakage current to "droop" in *hold.* In s/h *modules*, the capacitance is usually fixed, and the properties of the complete device are optimized for one condition– and so specified. In s/h *monolithic ICs*, the capacitor is omitted, and furnished by the user (both for flexibility and because good capacitors for this purpose are hard to integrate). The optimum capacitance can be selected for the specific application. In some types, (e.g., SHA1144), the gain connections are external, like those of an op amp, permitting gains other than +1.

PERFORMANCE

In the *sample* mode, it is useful to consider that a SHA's performance can be characterized by specifications similar to those of a closed-loop operational amplifier (offset, drift, nonlinearity, gain error, bias current, etc.), but with somewhat slower response (gain-bandwidth, slewing rate, settling time) because of the need to charge the storage capacitor.

However, during the *sample-to-hold, hold,* and *hold-to-sample* states, the dynamic nature of the mode-switching introduces a number of specifications that are peculiar to SHAs. The most-important of these are defined below and illustrated in the adjoining figure. They include the *aperture time* and its *uncertainty*, the *sample-to-hold step, feedthrough* and *droop* (in hold), and *acquisition time.*



DEFINITIONS

Acquisition Time is the time required by the output of the device to reach its final value, within a specified error band, after the *sample* command has been given. Included are switch-delay time, the slewing interval, and settling time for a specified output-voltage change.

Aperture (Delay) Time is the time required after the *hold* command for the switch to open fully. The sample is, in effect, delayed by this interval, and the *hold* command would have to be advanced by this amount for precise timing.

Aperture Uncertainty—or *Aperture (Delay) Jitter*—is the range of variation in the *aperture time*. If the *aperture time* is "tuned out" by advancing the *hold* command a suitable amount, this spec establishes the ultimate timing error, hence, the maximum sampling frequency to a given resolution. For example, the ADSHM-5K specs are 20ns and 100ps.

Charge Transfer (or *offset step*), the principal component of *sample-to-hold* offset (or *pedestal*), is the charge transferred to the storage capacitor via stray capacitance when switching to the *hold* mode. It can sometimes be reduced by lightly coupling an appropriate-polarity version of the *hold* signal to the capacitor for cancellation. The associated voltage error ($\Delta Q/C$) can be reduced by using greater capacitance for storage; but this increases response time.

Droop is the change of the output voltage during *hold* as a result of leakage or bias currents flowing through the storage capacitor. Its polarity depends on the sources of leakage current within a given device. In ICs, it is specified as a *(droop* or *drift)* current, in modules, a dV/dt. (Note: $I = CdV/dt$.)

Feedthrough is the fraction of the input signal variation or ac input waveform that appears at the output in *hold*. It is caused by stray capacitive coupling from the input to the storage capacitor, principally across the open switch.

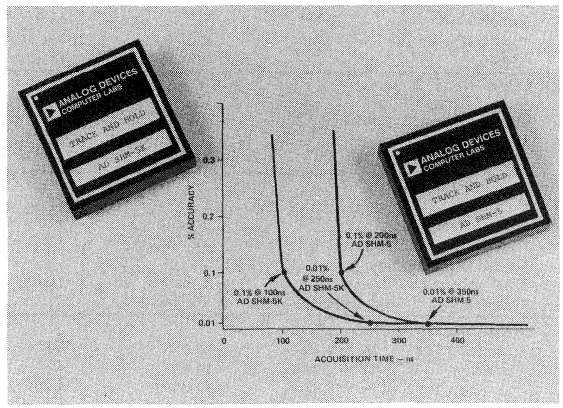
Sample-to-Hold Offset, a shift in level between the last value in *sample* and the value settled-to in *hold*, is the residual step error after the *charge transfer* is accounted for and/or cancelled. Since it is unpredictable in magnitude and may be a function of the signal, it is also known as *offset nonlinearity*.

Ultra Fast 0.01% Track/Sample - Hold Amplifiers

ADSHM-5 / ADSHM-5K

FEATURES
ADSHM-5
2nd Source—Replaces all SHM-5 Series
Fast 350ns Acquisition Time to ±0.01%
Aperture Uncertainty 250ps
ADSHM-5K
Ultra Fast 250ns Acquisition Time to ±0.01%
100ns Acquisition Time to ±0.1%
Wide 12MHz Bandwidth
300V/μs Slew Rate
Super Low 2nA Input Bias Current

APPLICATIONS
Fast Data Acquisition
Data Distribution Systems
Peak Measurement
Simultaneous Sample & Hold
Analog Delay & Storage



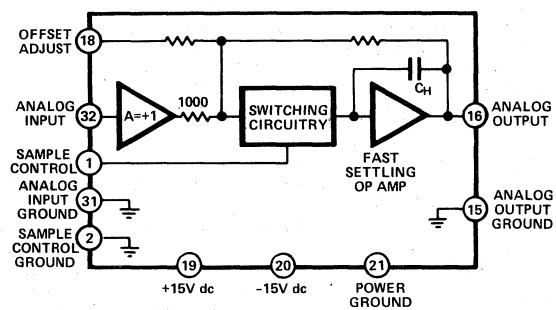


Figure 1. ADSHM-5; ADSHM-5K Block Diagram

GENERAL DESCRIPTION

The ADSHM-5 is a new ultra-fast (350ns to 0.01%) sample-hold amplifier designed for use with high-speed 10- and 12-bit analog-to-digital converters, such as Analog Devices' MAH, MAS, and HAS Series, as well as other manufacturers' types.

Designed specifically to second source other SHM-5's, the ADSHM-5 is a fit, form and function equivalent for these modules.

When used in a 12-bit data acquisition system, the ADSHM-5 acquires to within 12 bits (±0.01%) in 350ns for a 10V step change. For systems requiring 10-bit performance, the ADSHM-5 acquires to within ±0.1% in just 200ns max.

Other salient features of the ADSHM-5 include 0.005% max Tracking Nonlinearity and a Small Signal Bandwidth of 5MHz.

To upgrade system performance one need only to look at the new ADSHM-5K. While sharing the same pinout and package of the ADSHM-5, this all new module utilizes the latest "state-of-the-art" hybrid techniques to offer the user the optimum in specifications. The ADSHM-5K features a maximum 12-bit acquisition time of only 250ns and 10-bit acquisition time of an astonishing 100ns max. Another improvement is in acquisition time where the input buffer must also respond to a 10V step change, such as in multiplexed applications. The total acquisition time in this application is only 350ns max. Further, the Small Signal Bandwidth has been improved from 5MHz to 12MHz.

Both units are packaged in a 2″ X 2″ X 0.4″ case. The operating temperature range is 0 to +70°C, and the power requirements are ±15V dc @ 75mA max.

TRACK-AND-HOLD (T/H) MODE

When a unit is operated in the T/H mode, it is allowed to "track" the input signal for a period of time prior to initiating a "Hold Command." During the track period, the output follows the input, and the device functions like a unity gain amplifier.

When a Logic "0" is applied to the "Sample Control" input of the T/H, its output is frozen. This output level is held until the track mode is reestablished by a Logic "1" at the "Sample Control" input. This operation is shown graphically in Figure 4. The held output level is the voltage value at the input at the instant the hold command is applied, plus the aperture time.

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SPECIFICATIONS (typical @ +25°C and ±15V dc power supplies unless otherwise noted)

MODEL	UNITS	ADSHM-5	ADSHM-5K
ANALOG INPUT			
Input Voltage Range	V min	±10	*
Input Overvoltage, No Damage	V max	±15	*
Input Impedance	Ω	100M	1000
Input Bias Current	nA max	250	2
Offset Adjustment Range	mV	±300	*
SAMPLE CONTROL INPUT			
Sample Mode: Logic "1", TTL[1]	V	+2.0 to +5.5	*
Hold Mode: Logic "0", TTL	V	0 to +0.8	*
Loading	mA	+1	*
ANALOG OUTPUT			
Output Voltage Range	V min	±10	*
Output Current, S.C. Protected	mA	±40	±50
Output Impedance	Ω max	0.1	*
Noise (dc to 2.5MHz)	μV	100	*
ACCURACY/STABILITY DC			
Gain[2]	V/V	−1.000 ±0.1%	*
Gain vs. Temperature	ppm/°C	±10	*
Output Offset vs. Temperature	μV/°C max	±30	*
Output Offset vs. Supply	mV/V	1	*
Tracking Nonlinearity	% max	±0.005	*
Output Offset Voltage, Sample Mode	mV max	±50	*
DYNAMIC RESPONSE[3]			
Acquisition Time[4], 10V to 0.1%	ns max	200	100
Acquisition Time[4], 10V to 0.01%	ns max	350	250
Acquisition Time[5], 10V to 0.01%	ns typ	1,000	300
Bandwidth, Tracking, −3dB	MHz	5	12
Slew Rate, Tracking	V/μs	25	300
Aperture Delay Time[6]	ns	20	*
Aperture Uncertainty Time	ps	250	100
Hold Mode Droop	μV/μs max	20	12
Hold Mode Feedthrough, dc to 500kHz	dB	70	*
Sample to Hold Offset Error	mV max	±5	*
POWER REQUIREMENT			
Power Supply Voltage	V dc	±15 ±0.5	*
Quiescent Current	mA max	75	*
PHYSICAL–ENVIRONMENTAL			
Operating	°C	0 to +70	*
Storage	°C	−55 to +125	*
Relative Humidity	%	Up to 100%, noncondensing	*
Case Size	"	2.0 X 2.0 X 0.4	*
Case Material	N/A	Diallyl Phthalate per MIL-M-14 Type SDG-f	
Pins	N/A	0.020" round, gold plated; 0.25" long min	

NOTES
[1] TTL compatible. Schottky Pull Up (74S132 or equivalent) recommended to supply the 1mA required.
[2] The Gain Error of ±0.1% can be adjusted out most easily by using the Gain Adjust of the companion A/D converter.
[3] When switched into Hold, about 50ns is required for switching transients to settle. This time should be allowed before initiating the first conversion.
[4] From Tracking Mode.
[5] From Input Buffer.
[6] The Analog Signal Delay from the input to the Sampling Switch is approximately 32ns. Aperture Delay time is 20ns.

*Specifications same as ADSHM-5.

Specifications and prices subject to change without notice.

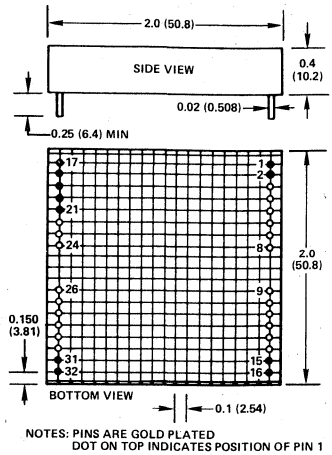


Figure 2. Mechanical Dimensions Dimensions shown in inches and (mm).

PIN	FUNCTION
1	SAMPLE CONTROL
2	SAMPLE CONTROL GND
15	ANALOG OUTPUT GND
16	ANALOG OUTPUT
17	NC
18	OFFSET ADJUST
19	+15V POWER
20	−15V POWER
21	POWER GROUND
31	ANALOG INPUT GND
32	ANALOG INPUT

Figure 3. Pin Designations

Variations in the instants of sampling are called Aperture Uncertainty. It appears as jitter in the sampling point and can cause significant errors when very high dV/dt inputs are sampled.

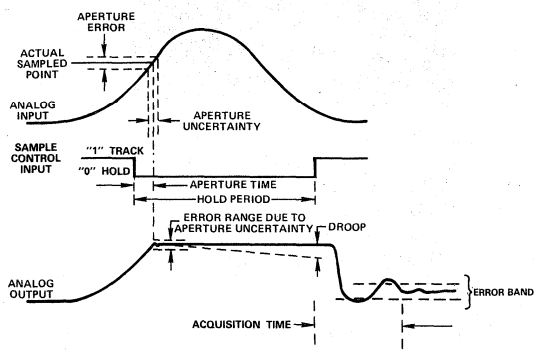


Figure 4. Track-and-Hold Operation

During the hold period, feedthrough and droop rate can introduce errors at the output. It is important that a track-and-hold have high feedthrough rejection to prevent input to output leakage during the hold period. The droop rate is the amount the output changes during the hold period, as a result of loading on the internal hold capacitor.

When the sample control input returns to the track condition, the amount of time required for the T/H output to reestablish accurate tracking of the input signal is called the acquisition time. Figure 5 shows settling accuracy versus acquisition time for the ADSHM-5 and ADSHM5-K.

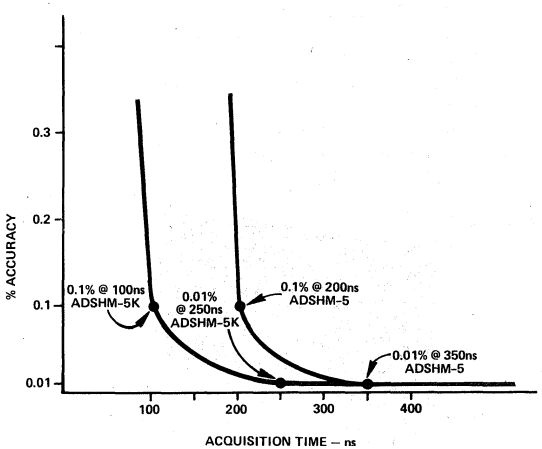


Figure 5. Acquisition Time vs. Settling Accuracy

SAMPLE-AND-HOLD (S/H) MODE

In the S/H mode of operation, devices are normally left in the hold condition. A very short sample pulse is applied to the sample control input when a new sample needs to be obtained at the output. The sample pulse width is dictated by the acquisition time.

OPERATION WITH A/D CONVERTER

The most common use for a track-and-hold is to place it ahead of an A/D converter to allow the digitizing of signals with bandwidths higher than the digitizer alone can handle. The use of the ADSHM series track-and-holds can allow a reduction of system aperture to 100ps. These track-and-holds may also be used for peak holding functions, simultaneous sampling A/Ds (with appropriate analog multiplexing), and other high-speed analog signal processing applications. The ADSHM series is designed to operate in either the track-and-hold or sample-and-hold modes. They perform well with the MAH series A/D converters as well as several other manufacturers' types, such as the Datel ADCEH series.

By using the circuit shown in Figure 6 using a 12-bit, 2μs A/D converter, throughput rates of up to 450kHz can be achieved for ultra-high-speed data acquisition applications.

The maximum value of input signal frequency that can be acquired and digitized (by the A/D converter) to within ±1/2LSB can be determined by the following:

$$fs = \frac{2^{-N}}{2\pi T_A} = \frac{1}{2\pi \cdot 4096 \cdot 1 \times 10^{-10}} = 388.7\text{kHz}$$

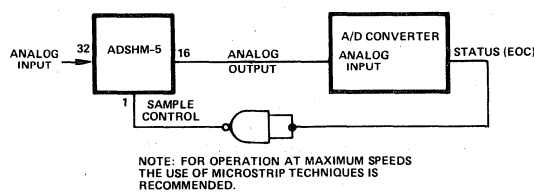


Figure 6. Typical Circuit for Operation with A/D Converter

PEAK DETECTOR

Figure 7 shows a slope-sensitive circuit which is capable of finding the peaks of positive excursions of an input waveform and digitizing the result. The circuit may be implemented without the A/D converter, in which case the output is an analog level held by the T/H module that may be observed or measured in some other manner.

The comparator triggers the T/H module when the positive slope of the input signal drops below a threshold slope equal to 15V/R2C1. A minimum positive slope of 15V/R1C1 is required to arm the detector. Resistors R1 and R2 are used to provide a guard band to prevent noise from triggering the circuit. The guard-band voltage is equal to 15V X R1/R2 and is generally set to approximately 5mV to 20mV.

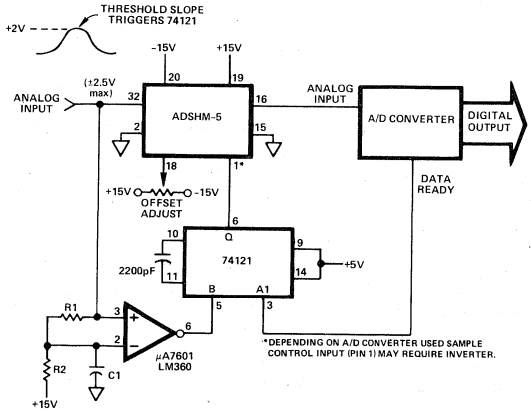


Figure 7. Peak Detector Circuit

OFFSET ADJUSTMENT

The maximum sample-to-hold offset error of 5mV is constant with signal level. The circuit of Figure 8 can be used to adjust this error out while in the hold mode. Please note that the ADSHM-5 or ADSHM-5K can be adjusted for zero output offset in either the tracking (sample) mode or the hold mode, but not in both at the same time.

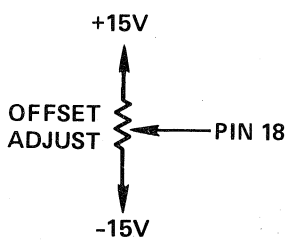


Figure 8. Offset Adjustment

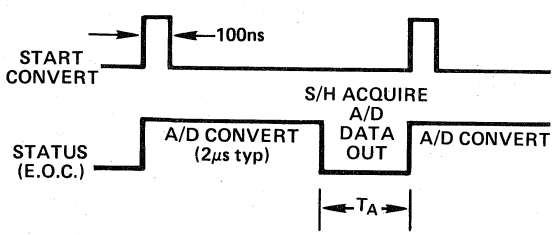


Figure 9. Timing Diagram Acquisition Time
T_A = ADSHM-5 = 350ns; T_A = ADSHM-5K = 250ns

RECOMMENDED FOR USE WITH THESE POPULAR A/D CONVERTERS

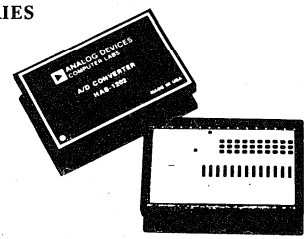
MAS SERIES



FEATURES
High Speed at Low Cost
- 8 Bits 1μs max
- 10 Bits 1.5μs max
- 12 Bits 2μs max

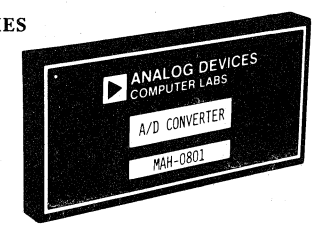
No Missing Codes Over Temperature
Low Power
Industry Standard Pin Out
Parallel and Serial Outputs
Pin and Function Compatible with ADCEH Series

HAS SERIES



FEATURES
Reliable Hybrid Construction
Conversion Times as Low as 1.2μs
Resolution: 8, 10 and 12 Bits
Exceptional Accuracy, 0.012% or FS
Low Power
Contained in Glass or Metal 32-Pin DIP
Adjustment-Free Operation

MAH SERIES



FEATURES
High Speed at Low Cost
- 8 Bits @ 750ns max
- 10 Bits @ 1μs max

Monotonic Over Temperature
Differential Nonlinearity ±1/4LSB typ
Parallel and Serial Outputs
Pin and Function Compatible with 4130, 4131

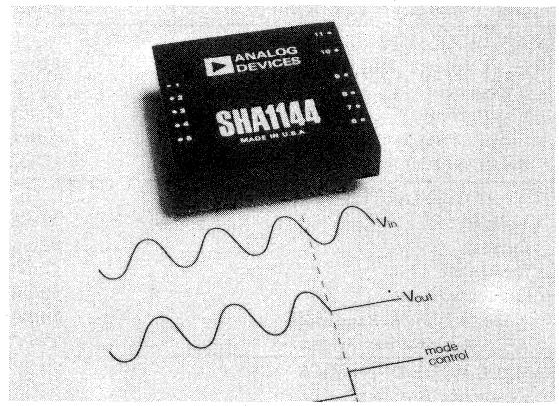
ANALOG DEVICES

High Resolution 14-Bit Sample and Hold Amplifier

SHA1144

FEATURES
- ±10V min Input/Output Range
- 50ns Aperture Delay
- 0.5ns Aperture Jitter
- 6μs Settling Time
- ±0.001% Max Gain Linearity Error
- Complete with Input Buffer

APPLICATIONS
- Track and Hold
- Peak Measurement Systems
- Data Acquisition Systems
- Simultaneous Sample-and-Hold



GENERAL DESCRIPTION

The SHA1144 is a fast sample-hold amplifier module with accuracy and dynamic performance appropriate for applications with fast 14-bit A/D converters. In the "sample" mode, it acts as a fast amplifier, tracking the input signal. When switched to the "hold" mode, the output is held at a level corresponding to the input signal voltage at the instant of switching. The droop rate in "hold" is appropriate to allow accurate conversion by 14-bit A/D converters having conversion times of up to 150μs.

DYNAMIC PERFORMANCE

The SHA1144 was designed to be compatible with fast 14-bit A/D converters such as the Analog Devices' ADC1130 and ADC1131 series, which convert 14 bits in 25μs and 12μs, respectively. Maximum acquisition time of 8μs for the SHA1144 permits high sampling rates for 14-bit conversions. The SHA1144 is guaranteed to have a maximum gain nonlinearity of ±0.001% of full scale to insure 1/2LSB accuracy in 14-bit systems. When in the "hold" mode, the droop rate is 1μV/μs, so the SHA1144 will hold an input signal to ±0.003% of full scale (20V p-p) for over 600μs.

PRINCIPLE OF OPERATION

The SHA1144 consists basically of two high speed operational amplifiers, a storage capacitor, and a digitally controlled switch. It differs from typical sample-and-hold modules in one important respect; application versatility. The user completes the SHA1144 feedback circuit external to the module. Therefore, the module may be used in inverting or noninverting configurations and can easily be arranged to provide circuit gain of more than unity to simplify signal conditioning in a subsystem.

FEEDBACK CONNECTIONS

A block diagram of the SHA1144 is shown in Figure 1. The input section acts as a voltage-to-current converter, providing the current needed to charge the "hold" capacitor. The output amplifier isolates the "hold" capacitor and provides low output impedance for driving the load. Since feedback is not hardwired in the module, both inverting and noninverting input terminals are available, and the SHA1144 can be connected as a follower with unity gain or potentiometric gain, as well as inverter or even a differential amplifier. Since the unity gain follower mode will be the most frequent application, performance data listed in the specification table is based on this operating mode.

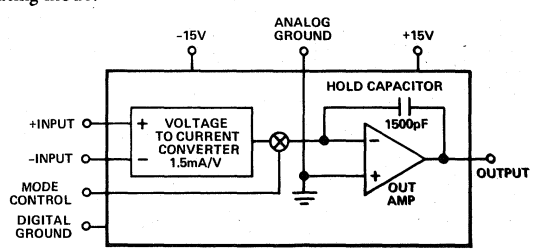


Figure 1. Block Diagram – SHA1144

14

SPECIFICATIONS (typical @ +25°C, gain = +1V/V and nominal supply voltages unless otherwise noted)

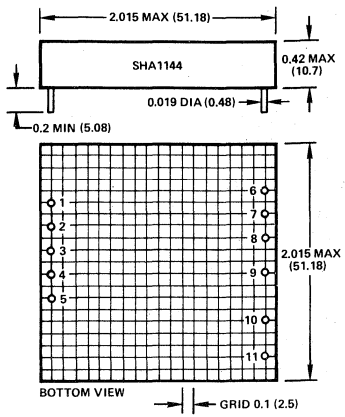
MODEL		SHA1144
ACCURACY		
Gain		+1V/V
Gain Error		±0.005%
Gain Nonlinearity		±0.0005% (±0.001% max)
Gain Temperature Coefficient (0 to +70°C)		±1ppm/°C (±2ppm/°C max)
INPUT CHARACTERISTICS		
Input Voltage Range		±10V
Impedance		$10^{11}\ \Omega \| 10pF$
Bias Current		0.5nA max
Initial Offset Voltage		Adjustable to Zero
Offset vs. Temperature (0 to +70°C)		±30μV/°C max
OUTPUT CHARACTERISTICS		
Voltage		±10V min
Current		±20mA min
Resistance		<1Ω
Capacitive load		350pF
Noise @ 100kHz Bandwidth		70μV p-p
@ 1MHz Bandwidth		175μV p-p
SAMPLE MODE DYNAMICS		
Frequency Response		
Small Signal (-3dB)		1MHz
Full Power		50kHz
Slew Rate		3V/μs
SAMPLE-TO-HOLD SWITCHING		
Aperture Delay Time		50ns
Aperture Uncertainty		0.5ns
Offset Step		1mV
Offset Nonlinearity		160μV
Switching Transient		
Amplitude		50mV
Settling Time to ±0.003%		1μs
HOLD MODE DYNAMICS		
Droop Rate		1μV/μs (2μV/μs max)
Variation with Temperature		double every +10°C
Feedthrough (for 20V p-p Input @ 1kHz)		-80dB
HOLD-TO-SAMPLE SWITCHING		
Acquisition Time to ±0.003%	(20V Step)	6μs (8μs max)
	(10V Step)	5μs
±0.01%	(20V Step)	5μs
	(10V Step)	4μs
DIGITAL INPUT		
Sample Mode (Logic "1")		+2V<Logic "1"<+5.5V @ 15nA max
Hold Mode (Logic "0")		0V<Logic "0"<+0.8V @ 5μA (20μA max)
POWER REQUIRED[1]		+15V ±3% @ 60mA
		-15V ±3% @ 45mA
TEMPERATURE RANGE		
Operating		0 to +70°C
Storage		-55°C to +85°C

[1] Recommended Power Supply ADI Model 902-2, ±15V @ ±100mA output.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

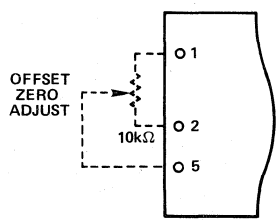
Dimensions shown in inches and (mm).



PIN DESIGNATIONS

1. TRIM
2. TRIM
3. +INPUT
4. -INPUT
5. TRIM
6. +15V
7. ANALOG GROUND
8. -15V
9. ANALOG OUTPUT
10. MODE CONTROL
11. DIGITAL GROUND

OFFSET ZERO ADJUST (OPTIONAL)



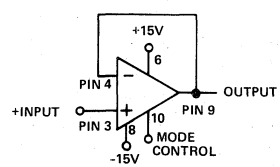


Figure 2. Unity Gain Follower

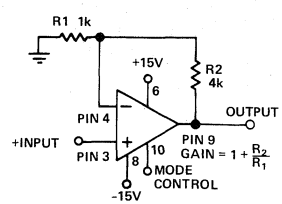


Figure 3. Noninverting Operation

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

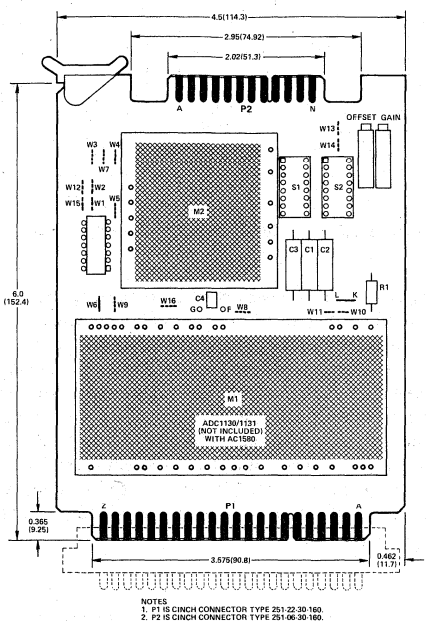


Figure 4. AC1580 Mounting Board

OPTIONAL AC1580 EVALUATION BOARD

The optional AC1580, shown in Figure 4, is available for benchtop-evaluation of the SHA1144.

S1, S2: Harris HI508A multiplexers (optional, not included).

DATA ACQUISITION APPLICATION

Successive-approximation A/D converters can generate substantial linearity errors if the analog input varies during the period of conversion; even the fast 14-bit models available cannot tolerate input signal frequencies of greater than a few Hz. For this reason, sample-and-hold amplifiers like the SHA1144 are connected between the A/D and its signal source to hold the analog input constant during conversion.

When the SHA1144 is connected to an A/D, its aperture time uncertainty, rather than the A/D's conversion time, is the factor which limits the allowable input signal frequency. The SHA1144, with a typical aperture delay time of 50ns and an uncertainty of 0.5ns, will change from the sample mode to the hold mode 50 to 50.5ns after the "1" to "0" transition of the mode control input. If the system timing is so arranged as to initiate the mode control signal 50ns early, then switching will actually occur within 0.5ns of the desired time as shown below.

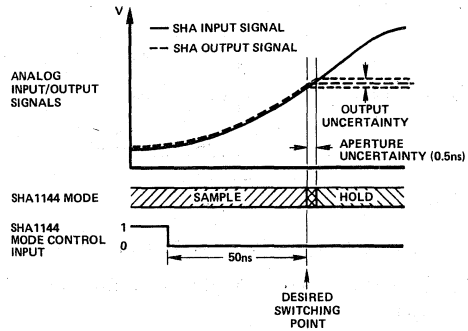


Figure 5. Aperture Uncertainty

The maximum allowable slew rate will thus equal the quotient of the maximum allowable voltage uncertainty and the 0.5ns aperture uncertainty. For sinewave inputs, the corresponding maximum frequency is expressed by:

$$f_{max} = \left(\frac{\Delta E}{E_{FS}}\right)\left(\frac{1}{2\pi\Delta t}\right) \cong 3.18 \times 10^8 \left(\frac{\Delta E}{E_{FS}}\right)$$

where: ΔE = the allowable voltage uncertainty

E_{FS} = the sinewave magnitude

For a system containing a SHA1144 and a 14-bit A/D with ±10V input signals and an allowable input uncertainty of ±1/2LSB (±620μV), the maximum allowable signal frequency will be 19.7kHz.

POWER SUPPLY AND GROUNDING CONNECTIONS

The proper power supply and grounding connections are shown below in Figure 6.

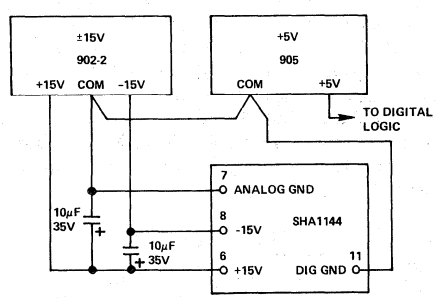


Figure 6. Power Supply and Grounding Connections

The ±15V power supplies must be externally bypassed as shown. The capacitors should be tantalum types and should be installed as close to the module pins as possible. The analog and digital ground lines should be run separately to their respective power supply commons to prevent coupling of digital switching noise to the sensitive analog circuit section.

OPERATION WITH AN A/D CONVERTER

Figure 7 below shows the appropriate connections between the SHA1144 and a successive approximation A/D converter in block diagram form.

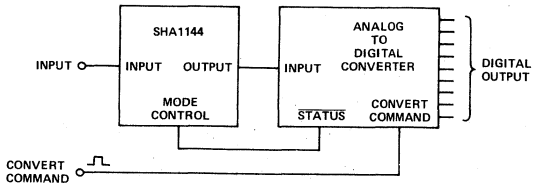


Figure 7. SHA1144 and A/D Connections

The resulting timing sequence at the start of conversion is illustrated in Figure 8.

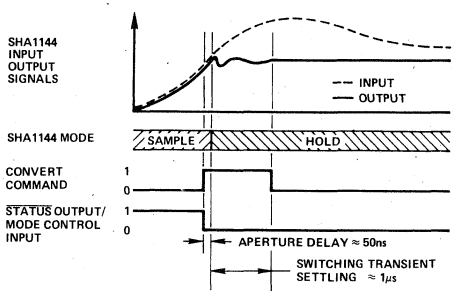


Figure 8. A/D and SHA Timing at Start of Conversion

Note that the leading edge of the convert command pulse causes the converter's STATUS output to go to Logic "0" which in turn switches the SHA1144 from sample to hold. As discussed previously, the typical SHA1144 actually changes modes 50 to 50.5ns after the "1" to "0" transition of the mode control input. This mode switching causes a transient on the output terminal which decays to within 0.003% of the final value in approximately 1μs. Once the transient has settled, the convert command input is returned to Logic "0" and the conversion proceeds. As shown in Figure 9, the STATUS signal returns to Logic "1" and the SHA1144 returns to the sample mode at the end of conversion. Within 6μs, it will have acquired the input signal to 0.003% accuracy and a new conversion cycle may be started.

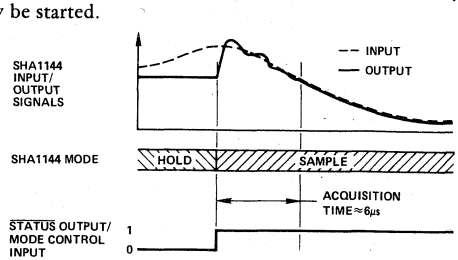


Figure 9. A/D and SHA Timing at End of Conversion

OPERATION WITH AN A/D AND MULTIPLEXER

The subsystem of Figure 10 may also be connected to a multiplexer like the Harris HI508A as shown below.

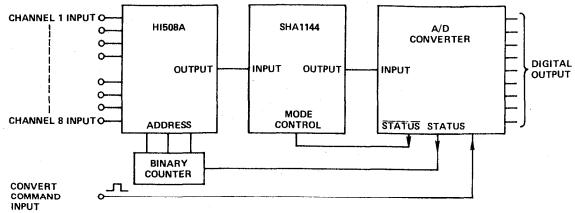


Figure 10. A/D, SHA, and MPX Connections

The leading edge of the convert command pulse sets the STATUS output to Logic "0" thereby switching the SHA1144 to "hold"; the corresponding change to Logic "1" of the STATUS output increments the binary counter and changes the multiplexer address. Since the SHA1144's aperture time is small with respect to the multiplexer switching time, it will have switched to the hold mode before the multiplexer actually changes channels. The multiplexer switching transients will settle out long before the SHA returns to "sample" at the end of conversion. The timing sequence described above is illustrated in Figure 11.

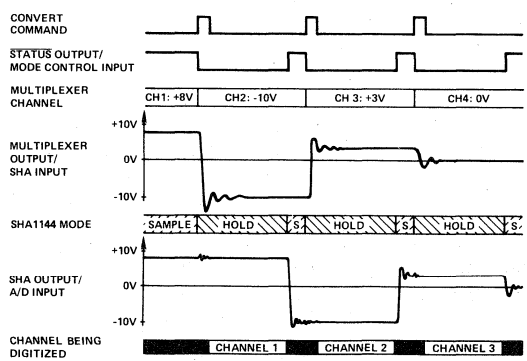


Figure 11. A/D, SHA, and MPX Timing

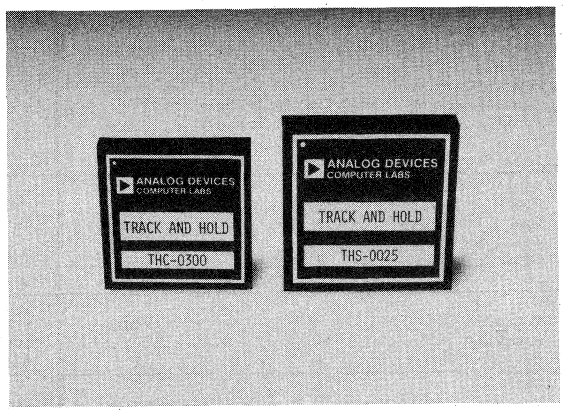
This method of sequencing the multiplexer may be altered to permit random addressing or addressing in a preset pattern. The timing of the multiplexer address changes may also be altered but consideration should be given to the effects of feedthrough in the SHA1144. Feedthrough is the coupling of analog input signals to the output terminal while the SHA is in "hold". Large multiplexer switching transients occuring during A/D conversion may introduce an error.

Ultra High Speed Sample/Track-and-Hold Amplifiers

THS, THC SERIES

FEATURES
- 20ps Aperture Uncertainty (THS)
- 15 to 1000ns Acquisition Times
- 0.01% Linearity
- DC Coupled High Input Z Buffer

APPLICATIONS
- Data Acquisition Systems
- Data Distribution Systems
- Peak Measurement Systems
- Simultaneous Sample & Hold
- Analog Delay & Storage



GENERAL DESCRIPTION

The THS/THC series' modules include the fastest sample/track-and-hold amplifier (SHA) available (THS-0025), as well as general purpose high speed low droop rate, low feedthrough devices such as the THC-1500. The six devices in the series allow a wide range of trade-offs between speed, price, droop rate, output noise levels, gain precision and offset drift. All devices feature high input impedance buffer amplifiers and high output current amplifiers (50mA). The THS units achieve their speed through the use of a dc-coupled Schottky diode sampling bridge while the THC series use MOS FET switches. TTL, or ECL logic can be used on any THC device, and either is available as a no cost option on THS units.

APPLICATIONS

The most common use for a track and hold is to place it ahead of an A/D converter to allow the digitizing of signals with bandwidths higher than the digitizer alone can handle. The use of the THS series track and holds can allow a reduction of system aperture to 20ps while THC units provide 100ps. These track and holds may also be used for peak holding functions, simultaneous sampling A/Ds (with appropriate analog multiplexing), and other high speed analog signal processing applications. These modules have been used to construct 13-bit A/D converters with word rates as high as 10MHz. The THS/THC series is designed to operate in either the track-and-hold or sample-and-hold modes. They perform well with the MAS series' A/D converters.

TRACK-AND-HOLD (T/H) MODE

When a THS/THC unit is operated in the T/H mode, it is allowed to "track" the input signal for a period of time prior to initiating a "hold command". During the track period, the output follows the input, and the device functions like an amplifier. In the THC units a resistor gain programmable op amp provides this function.

When a Logic "1" is input to the "hold command" input of the T/H, its output is frozen. This output level is held until the track mode is reestablished by a Logic "0" at the "hold command" input. This operation is shown graphically in Figure 1. The held output level is the voltage value at the input at the instant the hold command is applied, plus the aperture time.

Variations in the instants of sampling are called aperture uncertainty. It appears as jitter in the sampling point and can cause significant errors when very high dV/dt inputs are sampled.

During the hold period, feedthrough and droop rate can introduce errors at the output. It is important that a track and hold have high feedthrough rejection to prevent input to output leakage during the hold period. The droop rate is the amount the output changes during the hold period, as a result of loading on the internal hold capacitor.

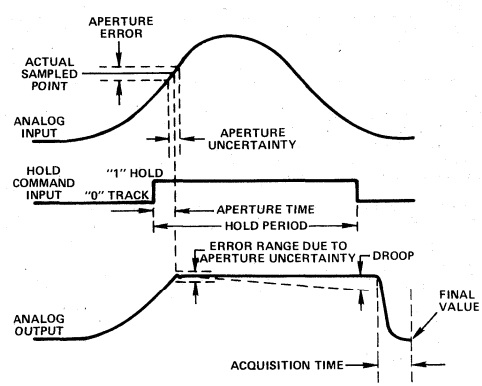


Figure 1. Track-and-Hold Operation

SPECIFICATIONS (typical at 25°C and nominal supply voltages)

MODEL	UNITS	FAST THC SERIES THC-0300	THC-0750	THC-1500	ULTRA FAST THS SERIES THS-0025	THS-0060	THS-0225
DYNAMIC CHARACTERISTICS							
Acquisition Time (to 0.1%)	ns	100	300	1000	25	75	300
Sample Rate (max)[1]	MHz	5	2.5	1	30	15	3.5
Aperture Time TTL	ns	18	*	*	10	**	**
ECL	ns	8	*	*	6	**	**
Settling Time THC to 0.1%, THS to 1% (See Figure 2)	ns	80	250	900	15	50	200
Bandwidth (Small Signal 3dB)	MHz	12	4	1.2	60	20	5
Slew Rate	V/μs	300	100	30	300	100	25
Aperture Uncertainty	ps max	100	*	*	20	**	**
Harmonic Distortion, 500kHz THC, 5MHz THS	dB	68	*	*	*	*	*
Feedthrough Rejection (dc to max Sample Rate/2) (dc to 5MHz THS)	dB	63	70	80	65	75	80
Droop Rate	μV/μs	12	5	2	5000	500	100
ACCURACY/STABILITY DC							
Gain	V/V	−1 ±2% (Pin 6 to Pin 15)			0.975	**	**
Gain vs. Temperature	ppm/°C	10	*	*	5	**	**
Zero Offset Voltage		Adjustable to Zero			Adjustable to Zero		
Offset vs. Temperature	ppm/°C	10	*	*	30	**	**
Linearity	%	±0.01	*	*	*	*	*
INPUT							
Voltage	V max	±10	*	*	±2	**	**
Impedance	Ω	10^{10}	*	*	1M	**	**
Bias Current	nA	0.05	*	*	*	*	*
OUTPUT							
Voltage	V max	±10	*	*	±2 (No Load)	**	**
Current	mA	±50	*	*	*	*	*
Impedance		Less than 0.01Ω @ dc			5Ω (Output 1, Pin 21) 75Ω (Output 2, Pin 22)		
Noise (dc to 15MHz THS) (dc to 2.5MHz THC)	μV rms	100	50	50	200	100	50
HOLD COMMAND (DIGITAL INPUTS)					(TTL or ECL Purchased as no cost Options)		
TTL Single Line Input (2 Std. TTL Loads)							
"0" = Sample/Track		0 to +0.4V	*	*	*	*	*
"1" = Hold		+2.4 to +5V	*	*	*	*	*
ECL		Single Line Input[2]			Two Line Complementary[3]		
"0" = Sample/Track	V	−1.7	*	*	*	*	*
"1" = Hold	V	−0.8	*	*	*	*	*
POWER REQUIREMENTS							
+15V ±5% (THC) +12V to +15V (THS)	mA max	90	*	*	100	**	**
−15V ±5% (THC) −12V to −15V (THS)	mA max	80	*	*	100	**	**
+5V ±5% (THS) TTL Option	mA max	N/A	*	*	20	**	**
−5.2V ±5% (THS)	mA max	N/A	*	*	80	**	**
−5.2V ±5% (THS) ECL Option	mA max	N/A	*	*	24	**	**
Power Supply Rejection Ratio ±15V	mV/V max	10	*	*	20	**	**
TEMPERATURE RANGE							
Operating	°C	0 to +70	*	*	*	*	*
Storage	°C	−55 to +125	*	*	*	*	*
PHYSICAL CHARACTERISTICS							
Case		diallyl phthalate per MIL-M-14 type SDG-F			diallyl phthalate per MIL-M-14 type SDG-F		

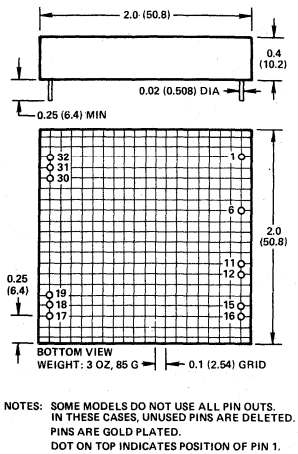
NOTES:
[1] Sample rates shown are a guide only and are based on system acquisition times—not logic speed. These rates can be exceeded with acquisition time trade-offs.
[2] These inputs are unterminated. An external pull down resistor should be used when driven by ECL 10k logic source.
[3] These inputs are each terminated with a 330Ω pull down resistor to −5.2V.

*Specifications same as THC-0300.
**Specifications same as THS-0025.

Specifications subject to change without notice.

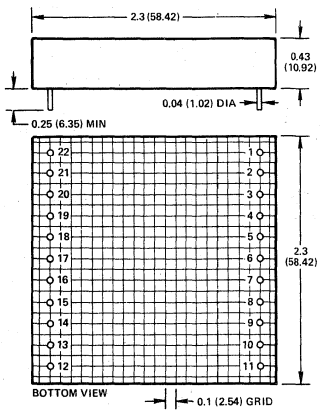
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTES: SOME MODELS DO NOT USE ALL PIN OUTS. IN THESE CASES, UNUSED PINS ARE DELETED. PINS ARE GOLD PLATED. DOT ON TOP INDICATES POSITION OF PIN 1.

THC Series



NOTES: SOME MODELS DO NOT USE ALL PIN OUTS. IN THESE CASES, UNUSED PINS ARE DELETED. PINS ARE GOLD PLATED. DOT ON TOP INDICATES POSITION OF PIN 1.

THS Series

PIN DESIGNATIONS

PIN	THC SERIES' FUNCTION	THS SERIES' FUNCTION
1	ANALOG INPUT	GROUND
4	N/A	+15V
5	N/A	GROUND
6	FEEDBACK	-15V
7	N/A	HOLD COMMAND (ECL)
8	N/A	$\overline{\text{HOLD COMMAND}}$ (ECL)
9	N/A	HOLD COMMAND (TTL)
10	N/A	-5.2V
11	OFFSET ADJUST	+5V
12	OFFSET ADJUST	GROUND
13	N/A	OFFSET ADJUST
14	N/A	ANALOG INPUT 1
15	UNITY GAIN	N/A
16	ANALOG OUTPUT	GROUND
17	GROUND	N/A
18	-15V	N/A
19	+15V	N/A
20	N/A	GROUND
21	N/A	ANALOG OUTPUT 1
22	N/A	ANALOG OUTPUT 2
30	HOLD COMMAND (ECL)	N/A
31	HOLD COMMAND (TTL)	N/A
32	GROUND	N/A

When the hold command input returns to the track condition, the amount of time required for the T/H output to reestablish accurate tracking of the input signal is called the acquisition time. Figure 2 shows settling accuracy versus acquisition time for the THS/THC series. Figure 3 shows superimposed photographs of the input and output waveforms of a THS-0025 operated as a track-and-hold amplifier. Note that the output reacquires the input just 12ns after the end of the hold time.

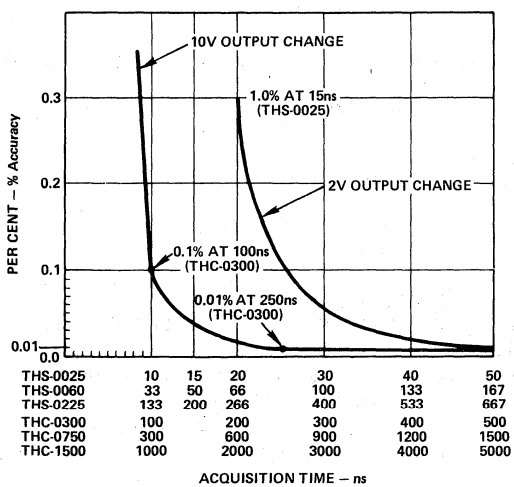


Figure 2. Acquisition Time vs. Settling Accuracy

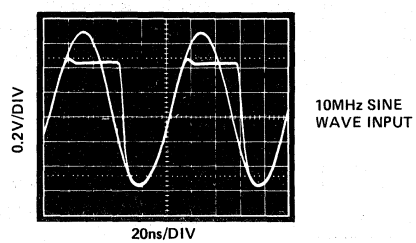


Figure 3. Track-and-Hold Operation (THS-0025)

SAMPLE AND HOLD (S/H) MODE

In the S/H mode of operation, devices are normally left in the hold condition. A very short sample pulse is applied to the hold command input when a new sample needs to be obtained at the output. The sample pulse width is dictated by the acquisition time. For small sample-to-sample variations, a pulse width as narrow as 12ns may be used for THS units and 80ns for THC units. If possible for greater accuracy, sample pulses should be wider (see Figure 2).

In general, however, the pulse width to the THS-0025 should be 15ns to 50ns, depending on required accuracy. Figure 4 shows the input and output waveforms of a THS-0025 used in the S/H mode.

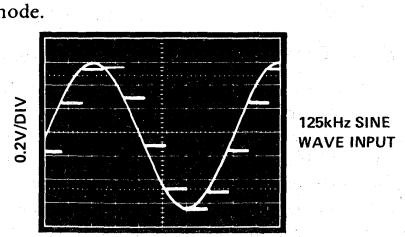


Figure 4. Sample-and-Hold Operation (THS-0025)

APPLICATION NOTES

Figure 5 shows a slope sensitive circuit which is capable of finding the peaks of positive excursions of an input waveform and digitizing the result. The circuit may be implemented without the A/D converter, in which case the output is an analog level held by the T/H module that may be observed or measured in some other manner.

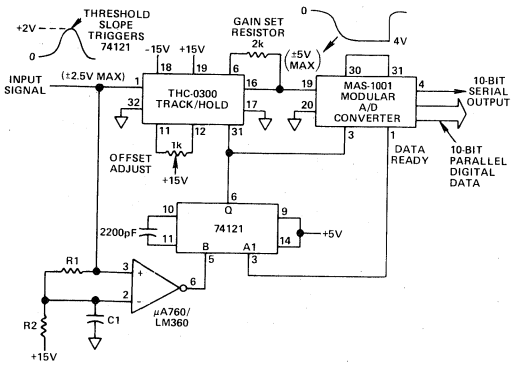


Figure 5. Peak Detector (THC-0300)

The comparator triggers the T/H module when the positive slope of the input signal drops below a threshold slope equal to 15V/R2C1. A minimum positive slope of 15V/R1C1 is required to arm the detector. Resistors R1 and R2 are used to provide a guard band to prevent noise from triggering the circuit. The guardband voltage is equal to 15V X R1/R2 and is generally set to approximately 5 to 20mV.

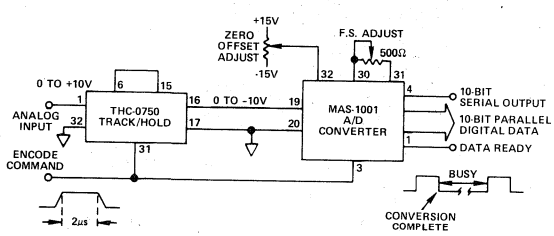


Figure 6. A/D Conversion System (THC)

Throughput Rate	Greater than 400kHz
Overall Accuracy	0.05%
Resolution	One Part in 1024 (10 Bit)
Aperture Uncertainty	100ps

Analog Input	Digital Output
0V	0000000000
+5.000V	1000000000
+9.990V	1111111111

Table 1. Capsule Performance for the A/D System

Analog Devices' THC series track-and-holds are designed to interface directly with the MAS series A/D converters as well as other commercially available modular A/Ds. In the above application, the THC module is used to acquire the analog signal to be converted and hold the sampled output over a much longer time period to permit the A/D module to accurately encode the analog data sample. In this way, the system aperture time is reduced to less than 100ps, and analog bandwidths up to the Nyquist limit may be accurately digitized.

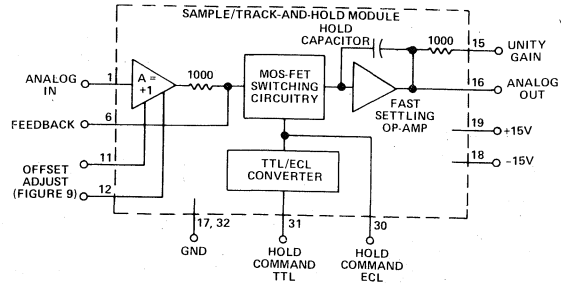


Figure 7. Sample/Track-and-Hold THC Series Block Diagram

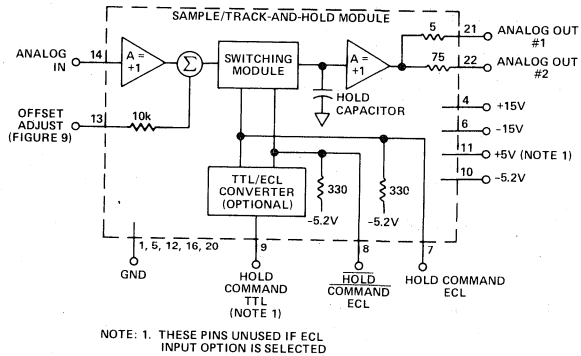


Figure 8. Sample/Track-and-Hold THS Series Block Diagram

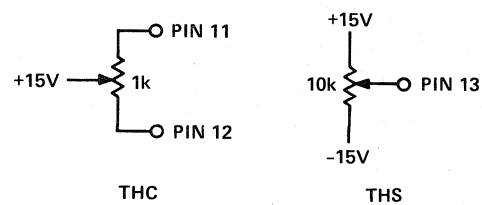


Figure 9. Optional Offset Adjustments

ORDERING INFORMATION

Order THS-0025 TTL, THS-0060 TTL, or THS-0225 TTL for TTL Hold Command Option.

Order THS-0025 ECL, THS-0060 ECL, or THS-0225 ECL for Balanced ECL Hold Command Input.

Order THC-0300, THC-0750, THC-1500 as required. All have available TTL and ECL Logic Inputs.

Data-Acquisition Subsystems

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Selection Guide
Data-Acquisition Subsystems

The products to be found in this section are high-performance modules and hybrid A/D conversion circuits that also provide sample-hold and/or multiplexing. In addition, some types have programmable-gain amplifiers, microprocessor interface logic, and switching for applications involving both differential and single-ended inputs.

In addition to the devices listed in the Selection Guide, there are a number of other devices, to be found in this Volume, which perform data-acquisition functions, including MACSYM, the μMAC-4000 Intelligent Measurement-and-Control Subsystem, Microcomputer Interface Boards, Digital Panel Meters, and A/D Converters (including, for example, the 12-bit 5MHz MOD-1205, with on-board track-hold amplifier).

Of especial note are the AD2036, AD2037, and AD2038 scanning digital panel instruments (to be found in the Digital Panel Instrument Section), which provide complete six-channel data-acquisition (including power supply) for measurement of temperature or voltage and have BCD data outputs for system input. Also of note (and to be found in Volume I) is the monolithic AD7581 data-acquisition-system-on-a-chip, which continuously converts 8 channels of analog information, stores stores them in dual-port RAM, and continuously makes all eight available by direct memory read instructions to the appropriate channel.

The data sheets provide complete descriptions, specifications, and application information. Additional general information pertaining to portions of the subsystems may be found in the appropriate sections of this Databook (e.g., A/D Converters, Sample/Track-Hold Amplifiers). Basic general information can be found in *Analog-Digital Conversion Notes*, a 246-page book published by Analog Devices, Inc. It is available at $5.95 from P.O. Box 796, Norwood, MA 02062.

		SINGLE CHANNEL				MULTI-CHANNEL				
		DAS1152	DAS1153	DAS1155	DAS1156	AD7581	AD363[1,2]	AD364[1,2]	AD362[1,3]	DAS1128[1]
Resolution	8 Bits					•				
	12 Bits						•	•		•
	14 Bits	•		•						
	15 Bits		•		•					
Input Structure	Sample/Hold	•	•	•	•		•	•	•	•
	Single Ended	•	•			•	•	•	•	
	Differential			•	•		•	•	•	•
	Amplifier									
	Differential Amplifier			•	•		•	•	•	•
	Resistor Programmable Gain			•	•					
	Channels									
	One	•	•	•	•					
	Eight					•	•	•	•	•
	Sixteen						•	•	•	•
Internal Reference		•	•	•	•		•	•	•	•
μP Bus Compatible		•	•	•	•	•		•		
Operating Temperature Ranges	0 to +70°C	•	•	•	•	•	•	•	•	•
	−25°C to +85°C	•	•	•	•	•				
	−55°C to +125°C						•	•	•	
Output	Digital	•	•	•	•	•	•	•		•
	Analog								•	
Logic Compatible	TTL	•	•	•	•	•	•	•	•	•
	CMOS					•				
Volume I Page		15-39	15-39	15-41	15-41	11-121	15-13	15-25	15-5	15-37
Volume II Page		15-25	15-25	15-29	15-29	–	15-9	15-13	15-5	15-17

[1] 8 channels differential input, 16 channels single ended.
[2] Two DIP packages.
[3] DAS Analog Input Section.

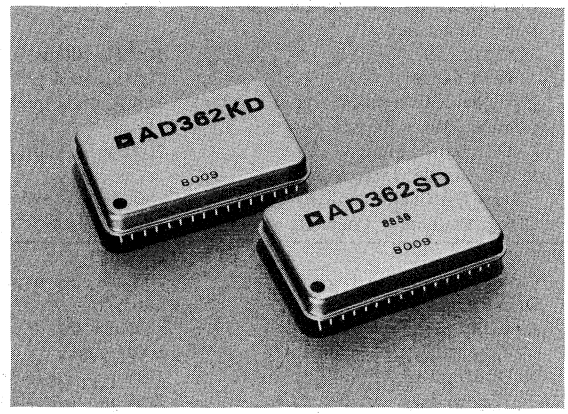
ANALOG DEVICES

Precision Sample-and-Hold with 16-Channel Multiplexer

AD362

FEATURES

- 16 Single-Ended or 8 Differential Channels with Switchable Mode Control
- True 12-Bit Precision: Nonlinearity ≤±0.005%
- High Speed: 10μs Acquisition Time to 0.01%
- Complete and Calibrated: No Additional Parts Required
- Small, Reliable: 32 Pin Hermetic Metal DIP
- Versatile: Simple Interface to Popular Analog to Digital Converters
- High Differential Input Impedance ($10^{10}\Omega$) and Common Mode Rejection (80dB)
- Fully Protected Multiplexer Inputs



PRODUCT DESCRIPTION

The AD362 is a complete, precision 16-channel data acquisition system analog input section in hybrid integrated circuit form. Large-scale linear integrated circuitry, thick- and thin-film technology and active laser trimming gives the AD362 extensive applications versatility along with full 12-bit accuracy.

The AD362 contains two 9-channel multiplexers, a differential amplifier, a sample-and-hold with high-speed output amplifier, a channel address latch and control logic. The multiplexers may be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A unique feature of the AD362 is an internal user-controllable analog switch that connects the multiplexers in either a single-ended or differential mode. This allows a single device to perform in either mode without hard-wire programming and permits a mixture of single-ended and differential sources to be interfaced by dynamically switching the input mode control.

The sample-and-hold mode control is designed to connect directly to the "Status" output of an analog to digital converter so that a convert command to the ADC will automatically put the sample-and-hold into the "Hold" mode. A precision hold capacitor is included with each AD362. The AD362 output amplifier is capable of driving the unbuffered analog input of most high-speed, 12-bit successive-approximation ADCs. Interface is thereby reduced to two simple connections with no additional components required.

When used with a 12-bit, 25-microsecond ADC such as the AD572, AD574 or AD ADC80, system throughput rate is as high as 30kHz at full rated accuracy. The AD362KD is specified for operation over a 0 to +70°C temperature range while the AD362SD operates to specification from −55°C to +125°C. Processing to MIL-STD-883, Class B is available for the AD362SD. Both grades are packaged in a hermetic, electrostatically shielded 32-pin metal dual-in-line package.

This four-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be found in Volume I, page 15-5.

PRODUCT HIGHLIGHTS

1. The AD362, when used with a precision analog to digital converter, forms a complete, accurate, high-speed data acquisition system.
2. The 16-input channels may be configured in single-ended, differential or a mixture of both modes. Mode switching is provided by a user-controllable internal analog switch.
3. Multiplexers, differential amplifier, sample-and-hold and high-speed output buffer provide complete analog interfacing capabilities.
4. Internal channel address latches are provided to facilitate interfacing the AD362 to data, address or control buses.
5. All grades of the AD362 are hermetically sealed in rugged metal DIP packages.
6. A precision hold capacitor is provided with each AD362.
7. The AD362SD is specified over the entire military temperature range, −55°C to +125°C. Processing to MIL-STD-883, Class B is available.

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SPECIFICATIONS (typical @ +25°C, ±15V and +5V with 2000pF hold capacitor as provided unless otherwise noted)

MODEL	AD362KD	AD362SD/AD362SD-883B[1]
ANALOG INPUTS		
Number of Inputs	16 Single-Ended or 8 Differential (Electronically Selectable)	*
Input Voltage Range, Linear		
T_{min} to T_{max}	±10V min	*
Input (Bias) Current, Per Channel	±50nA max	*
Input Impedance		
On Channel	$10^{10}\Omega$, 100pF	*
Off Channel	$10^{10}\Omega$, 10pF	*
Input Fault Current (Power Off or On)	20mA, max, Internally Limited	*
Common Mode Rejection		
Differential Mode	70dB min (80dB typ) @ 1kHz, 20V p-p	*
Mux Crosstalk (Interchannel,		
Any Off Channel to Any On Channel)	-80dB max (-90dB typ) @ 1kHz, 20V p-p	*
Offset, Channel to Channel	±2.5mV max	*
ACCURACY		
Gain Error, T_{min} to T_{max}	±0.02% FSR, max	*
Offset Error, T_{min} to T_{max}	±4mV	*
Linearity Error	±0.005% max	*
T_{min} to T_{max}	±0.01% max	*
Noise Error	1mV p-p, 0.1 to 1MHz, max	*
T_{min} to T_{max}	2mV p-p, 0.1 to 1MHz, max	*
TEMPERATURE COEFFICIENTS		
Gain, T_{min} to T_{max}	±4ppm/°C max	±2ppm/°C max
Offset, ±10V Range, T_{min} to T_{max}	±2ppm/°C max	±1.5ppm/°C max
SAMPLE AND HOLD DYNAMICS		
Aperture Delay	100ns max (50ns typ)	*
Aperture Uncertainty	500ps max (100ps typ)	*
Acquisition Time, for 20V Step to		
±0.01% of Final Value	18μs max (10μs typ)	*
Feedthrough	-70dB max (-80dB typ) @ 1kHz	*
Droop Rate	2mV/ms max (1mV/ms typ)	*
DIGITAL INPUT SIGNALS[2]		
Input Channel Select (Pins 28-31)	4-Bit Binary, Channel Address	*
	1LS TTL Load	*
Channel Select Latch (Pin 32)	"1": Latch Transparent	*
	"0": Latched	*
	8LS TTL Loads	*
Single Ended/Differential	"0": Single-Ended Mode	*
Mode Select (Pin 1)	"1": Differential Mode	*
	3TTL Loads	*
Sample and Hold Command (Pin 13)	"0": Sample Mode	*
	"1": Hold Mode	*
	1TTL Load	*
POWER REQUIREMENTS		
Supply Voltages/Currents	+15V, ±5% @ 30mA max	*
	-15V, ±5% @ 30mA max	*
	+5V, ±5% @ 40mA max	*
Total Power Dissipation	1.1 Watts max	*
TEMPERATURE RANGE		
Specification	0 to +70°C	-55°C to +125°C
Storage	-55°C to +85°C[3]	-55°C to +150°C

NOTES:
[1] The AD362 is available processed and screened to the requirements of MIL-STD-883, Class B. When ordering, specify "AD362SD/883B".
[2] One TTL Load is defined as $I_{IL} = -1.6mA$ max @ $V_{IL} = 0.4V$, $I_{IH} = 40\mu A$ max @ $V_{IH} = 2.4V$. One LS TTL Load is defined as $I_{IL} = -0.36mA$ max @ $V_{IL} = 0.4V$, $I_{IH} = 20\mu A$ max @ $V_{IH} = 2.7V$.
[3] AD362KD External Hold Capacitor is limited to +85°C; AD362 device itself may be stored at up to +150°C.

*Specifications same as AD362KD.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (ALL MODELS)

+V, Digital Supply	+5.5V
+V, Analog Supply	+16V
-V, Analog Supply	-16V
V_{IN}, Signal	±V, Analog Supply
V_{IN}, Digital	0 to +V, Digital Supply
A_{GND} to D_{GND}	±1V

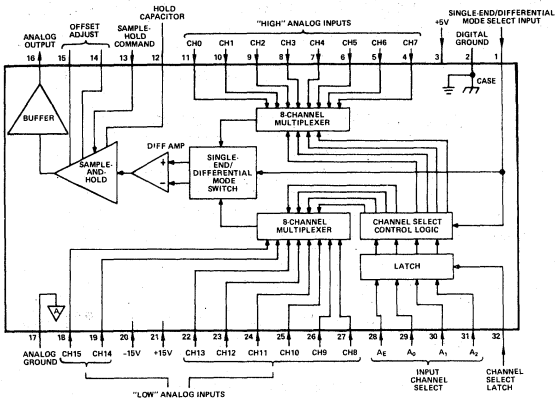


Figure 1. AD362 Analog Input Section Functional Block Diagram and Pinout

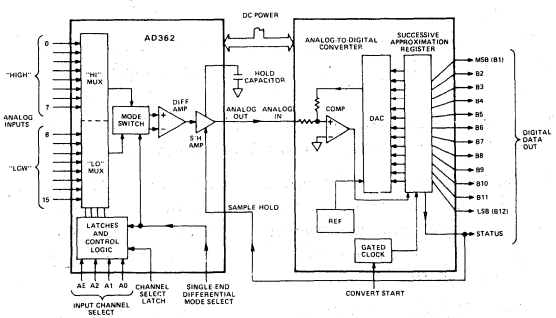


Figure 2. AD362 with ADC as a Complete Data Acquisition System

AD362 PIN FUNCTION DESCRIPTION

Pin Number	Function
1	Single-End/Differential Mode Select "0": Single-Ended Mode "1": Differential Mode
2	Digital Ground
3	Positive Digital Power Supply, +5V
4	"High" Analog Input, Channel 7
5	"High" Analog Input, Channel 6
6	"High" Analog Input, Channel 5
7	"High" Analog Input, Channel 4
8	"High" Analog Input, Channel 3
9	"High" Analog Input, Channel 2
10	"High" Analog Input, Channel 1
11	"High" Analog Input, Channel 0
12	Hold Capacitor (Provided)
13	Sample-Hold Command "0": Sample Mode "1": Hold Mode Normally Connected to ADC Status
14	Offset Adjust (See Figure 5)
15	Offset Adjust (See Figure 5)
16	Analog Output Normally Connected to ADC "Analog In"
17	Analog Ground
18	"High" ("Low") Analog Input, Channel 15 (7)
19	"High" ("Low") Analog Input, Channel 14 (6)
20	Negative Analog Power Supply, -15V
21	Positive Analog Power Supply, +15V
22	"High" ("Low") Analog Input, Channel 13 (5)
23	"High" ("Low") Analog Input, Channel 12 (4)
24	"High" ("Low") Analog Input, Channel 11 (3)
25	"High" ("Low") Analog Input, Channel 10 (2)
26	"High" ("Low") Analog Input, Channel 9 (1)
27	"High" ("Low") Analog Input, Channel 8 (0)
28	Input Channel Select, Address Bit AE
29	Input Channel Select, Address Bit A0
30	Input Channel Select, Address Bit A1
31	Input Channel Select, Address Bit A2
32	Input Channel Select Latch "0": Latched "1": Latch Transparent

AD362 ORDERING GUIDE

Model	Specification Temp Range	Max Gain TC
AD362KD	0 to +70°C	±4ppm/°C
AD362SD	-55°C to +125°C	±2ppm/°C
AD362SD/883B	-55°C to +125°C	±2ppm/°C

NOTE: D Suffix = Dual-In-Line package designator.

AD362 DESIGN

The AD362 consists of two 8-channel multiplexers, a differential amplifier, a sample-and-hold with high-speed output buffer, channel address latches and control logic as shown in Figure 1. The multiplexers can be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A unique feature of the AD362 is an internal analog switch controlled by a digital input that performs switching between single-ended and differential modes. This feature allows a single AD362 to perform in either mode without external hard-wire interconnections. Of more significance is the ability to serve a mixture of both single-ended and differential sources with a single AD362 by dynamically switching the input mode control.

Multiplexer channel address inputs are interfaced through a level-triggered ("transparent") input register. With a Logic "1" at the Channel Select Latch input, the address signals feed through the register to directly select the appropriate input channel. This address information can be held in the register by placing a Logic "0" on the Channel Select Latch input. Internal logic monitors the status of the Single-Ended/Differential Mode input and addresses the multiplexers accordingly.

A differential amplifier buffers the multiplexer outputs while providing high input impedance in both differential and single-ended modes. Amplifier gain and common mode rejection are actively laser-trimmed.

The sample-and-hold is a high speed monolithic device that can also function as a gated operational amplifier. Its uncommitted differential inputs allow it to serve a second role as the output subtractor in the differential amplifier. This eliminates one amplifier and decreases drift, settling time and power consumption. A Logic "1" on the Sample-and-Hold Command input will cause the sample-and-hold to "freeze" the analog signal while the ADC performs the conversion. Normally the Sample-and-Hold Command is connected to the ADC Status output which is at Logic "1" during conversion and Logic "0" between conversions. For slowly-changing inputs, throughput speed may be increased by grounding the Sample-and-Hold Command input instead of connecting it to the ADC status.

A Polystyrene hold capacitor is provided with each commercial temperature range device (AD362KD) while a Teflon capacitor is provided with units intended for operation at temperatures up to 125°C (AD362SD). Use of an external capacitor allows the user to make his own speed/accuracy tradeoff; a smaller capacitor will allow faster sample-and-hold response but will decrease accuracy while a larger capacitor will increase accuracy at slower conversion rates.

The output buffer is a high speed amplifier whose output impedance remains low and constant at high frequencies. Therefore, the AD362 may drive a fast, unbuffered, precision ADC without loss of accuracy.

The AD362 is constructed on a substrate that includes thick-film resistors for non-critical applications such as input protection and biasing. A separately-mounted laser-trimmed thin-film resistor network is used to establish accurate gain and high common-mode rejection. The metal package affords electromagnetic and electrostatic shielding and is hermetically welded at low temperatures. Welding eliminates the possibility of contamination from solder particles or flux while low temperature sealing maintains the accuracy of the laser-trimmed thin-film resistors.

THEORY OF OPERATION

Concept

The AD362 is intended to be used in conjunction with a high-speed precision analog-to-digital converter to form a complete data acquisition system (DAS) in microcircuit form. Figure 2 shows a general AD362-with-ADC DAS application.

By dividing the data acquisition task into two sections, several important advantages are realized. Performance of each design is optimized for its specific function. Production yields are increased thus decreasing costs. Furthermore, the standard configuration packages plug into standard sockets and are easier to handle than larger packages with higher pin counts.

System Timing

Figure 3 is a timing diagram for the AD362 connected as shown in Figure 2 and operating at maximum conversion rate. The ADC is assumed to be a conventional 12 bit type such as the AD572 or AD ADC80.

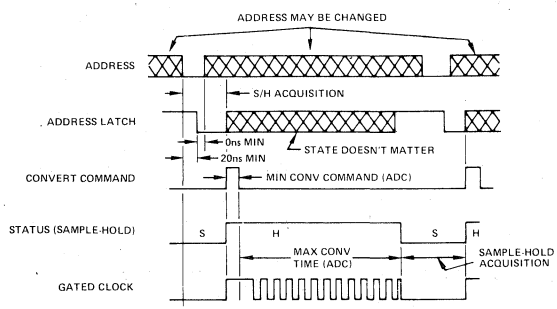


Figure 3. DAS Timing Diagram

The normal sequence of events is as follows:

1. The appropriate Channel Select Address is latched into the address register. Time is allowed for the multiplexers to settle.
2. A Convert Start command is issued to the ADC which, in response, indicates that it is "busy" by placing a Logic "1" on its Status line.
3. The ADC Status controls the sample-and-hold. When the ADC is "busy", the sample-and-hold is in the Hold mode.
4. The ADC goes into its conversion routine. Since the sample-and-hold is holding the proper analog value, the address may be updated during conversion. Thus multiplexer settling time can coincide with conversion and need not affect throughput rate.
5. The ADC indicates completion of its conversion by returning Status to Logic "0". The sample-and-hold returns to the Sample mode.
6. If the input signal has changed full-scale (different channels may have widely-varying data) the sample-and-hold will typically require 10 microseconds to "acquire" the next input to sufficient accuracy for 12-bit conversion.

After allowing a suitable interval for the sample-and-hold to stabilize at its new value, another Convert Start command may be issued to the ADC.

ANALOG DEVICES

Complete 16-Channel 12-Bit Integrated Circuit Data Acquisition System

AD363

FEATURES

Versatility
- **Complete System in Reliable IC Form**
- **Small Size**
- **16 Single-Ended or 8 Differential Channels with Switchable Mode Control**
- **Military/Aerospace Temperature Range: -55°C to +125°C (AD363S) MIL-STD-883B Processing Available**
- **Versatile Input/Output/Control Format**
- **Short-Cycle Capability**

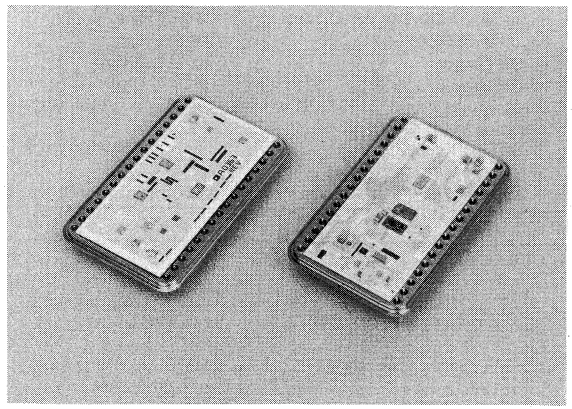
Performance
- **True 12-Bit Operation: Nonlinearity ≤±0.012%**
- **Guaranteed No Missing Codes Over Temperature Range**
- **High Throughput Rate: 30kHz**
- **Low Power: 1.7W**

Value
- **Complete: No Additional Parts Required**
- **Reliable: Hybrid IC Construction, Hermetically Sealed. All Inputs Fully Protected**
- **Precision +10.0 ±0.005 Volt Reference for External Application**
- **Fast Precision Buffer Amplifier for External Application**
- **Low Cost**

PRODUCT DESCRIPTION

The AD363 is a complete 16 channel, 12-bit data acquisition system in integrated circuit form. By applying large-scale linear and digital integrated circuitry, thick and thin film hybrid technology and active laser trimming, the AD363 equals or exceeds the performance and versatility of previous modular designs.

The AD363 consists of two separate functional blocks. Each in hermetically-sealed 32 pin dual-in-line packages. The analog input section contains two eight-channel multiplexers, a differential amplifier, a sample-and-hold, a channel address register and control logic. The multiplexers may be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A unique feature of the AD363 is an internal user-controllable analog switch that connects the multiplexers in either a single-ended or differential mode. This allows a single device to perform in either mode without hard-wire programming and permits a mixture of single-ended and differential sources to be interfaced to an AD363 by dynamically switching the input mode control.



The Analog-to-Digital Converter Section contains a complete 12-bit successive approximation analog-to-digital converter, including internal clock, precision 10 volt reference, comparator, buffer amplifier and a proprietary-design 12-bit D/A converter. Active laser trimming of the reference and D/A converter results in maximum linearity errors of ±0.012% while performing a 12-bit conversion in 25 microseconds.

Analog input voltage ranges of ±2.5, ±5.0, ±10, 0 to +5 and 0 to +10 volts are user-selectable. Adding flexibility and value are the precision 10 volt reference (active-trimmed to a tolerance of ±5mV) and the internal buffer amplifier, both of which may be used for external applications. All digital signals are TTL/DTL compatible and output data is positive-true in parallel and serial form.

System throughput rate is as high as 30kHz at full rated accuracy. The AD363K is specified for operation over a 0 to +70°C temperature range while the AD363S operates to specification from -55°C to +125°C. Processing to MIL-STD-883B is available for the AD363S. Both device grades are guaranteed to have no missing codes over their specified temperature ranges.

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This four-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be found in Volume I, page 15-13.

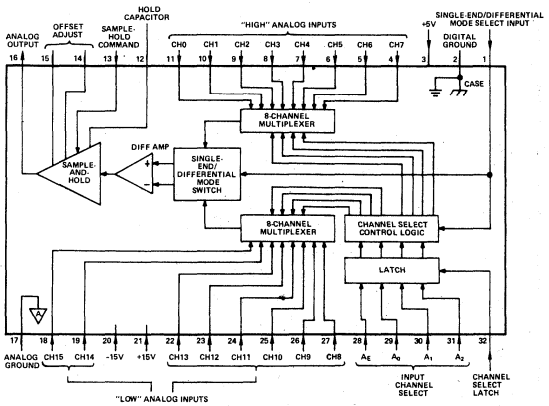
SPECIFICATIONS (typical @ +25°C, ±15V and +5V with 2000pF hold capacitor as provided unless otherwise noted)

MODEL	AD363K	AD363S
ANALOG INPUTS		
Number of Inputs	16 Single-Ended or 8 Differential (Electronically Selectable)	*
Input Voltage Ranges		
Bipolar	±2.5V, ±5.0V, ±10.0V	*
Unipolar	0 to +5V, 0 to +10V	*
Input (Bias) Current, Per Channel	±50nA max	*
Input Impedance		
On Channel	$10^{10}\Omega$, 100pF	*
Off Channel	$10^{10}\Omega$, 10pF	*
Input Fault Current (Power Off or On)	20mA, max, Internally Limited	*
Common Mode Rejection		
Differential Mode	70dB min (80dB typ) @ 1kHz, 20V p-p	*
Mux Crosstalk (Interchannel,		
Any Off Channel to Any On Channel)	-80dB max (-90dB typ) @ 1kHz, 20V p-p	*
RESOLUTION	12 BITS	*
ACCURACY		
Gain Error[1]	±0.05% FSR (Adj. to Zero)	*
Unipolar Offset Error	±10mV (Adj to Zero)	*
Bipolar Offset Error	±20mV (Adj to Zero)	*
Linearity Error	±½LSB max	*
Differential Linearity Error	±1LSB max (±½LSB typ)	*
Relative Accuracy	±0.025% FSR	*
Noise Error	1mV p-p, 0 to 1MHz	*
TEMPERATURE COEFFICIENTS		
Gain	±30ppm/°C max (±10ppm/°C typ)	±25ppm/°C max (±15ppm/°C typ)
Offset, ±10V Range	±10ppm/°C max (±5ppm/°C typ)	±8ppm/°C max (±5ppm/°C typ)
Differential Linearity	No Missing Codes Over Temperature Range	*
SIGNAL DYNAMICS		
Conversion Time[2]	25μs max (22μs typ)	*
Throughput Rate, Full Rated Accuracy	25kHz min (30kHz typ)	*
Sample and Hold		
Aperture Delay	100ns max (50ns typ)	*
Aperture Uncertainty	500ps max (100ps typ)	*
Acquisition Time		
To ±0.01% of Final Value for Full Scale Step	18μs max (10μs, typ)	*
Feedthrough	-70dB max (-80dB typ) @ 1kHz	*
Droop Rate	2mV/ms max (1mV/ms typ)	*
DIGITAL INPUT SIGNALS[3]		
Convert Command (to ADC Section, Pin 21)	Positive Pulse, 200ns min Width. Leading Edge ("0" to "1") Resets Register, Trailing Edge ("1" to "0") Starts Conversion.	*
	1TTL Load	*
Input Channel Select (To Analog Input Section, Pins 28-31)	4 Bit Binary, Channel Address.	*
	1LS TTL Load	*
Channel Select Latch (To Analog Input Section, Pin 32)	"1" Latch Transparent	*
	"0" Latched	*
	4LS TTL Loads	*
Sample-Hold Command (To Analog Input Section Pin 13 Normally Connected To ADC "Status", Pin 20)	"0" Sample Mode	*
	"1" Hold Mode	*
	2LS TTL Loads	*
Short Cycle (To ADC Section Pin 14)	Connect to +5V for 12 Bits Resolution.	*
	Connect to Output Bit n + 1 For n Bits Resolution.	*
	1TTL Load	*
Single Ended/Differential Mode Select (To Analog Input Section, Pin 1)	"0": Single-Ended Mode	*
	"1": Differential Mode	*
	3TTL Loads	*

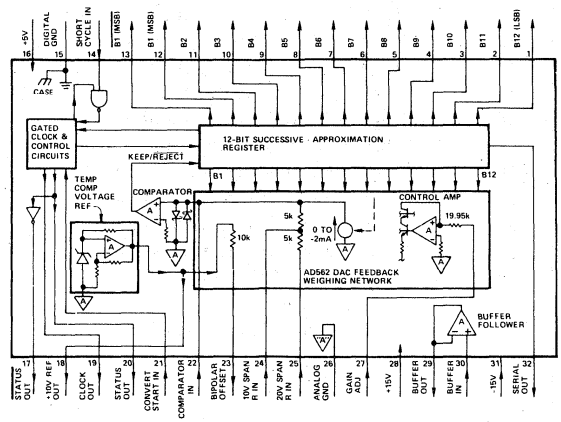
MODEL	AD363K	AD363S
DIGITAL OUTPUT SIGNALS[3]		
(All Codes Positive True)		
Parallel Data		
Unipolar Code	Binary	*
Bipolar Code	Offset Binary/Two's Complement	*
Output Drive	2TTL Loads	*
Serial Data (NRZ Format)		
Unipolar Code	Binary	*
Bipolar Code	Offset Binary	*
Output Drive	2TTL Loads	*
Status ($\overline{\text{Status}}$)	Logic "1" ("0") During Conversion	*
Output Drive	2TTL Loads	*
Internal Clock		
Output Drive	2TTL Loads	*
Frequency	500kHz	*
INTERNAL REFERENCE VOLTAGE	+10.00V, ±10mV	*
Max External Current	±1mA	*
Voltage Temp. Coefficient	±20ppm/°C, max	*
POWER REQUIREMENTS		
Supply Voltages/Currents	+15V, ±5% @ +45mA max (+38mA typ)	*
	-15V, ±5% @ -45mA max (-38mA typ)	*
	+5V, ±5% @ +136mA max (+113mA typ)	*
Total Power Dissipation	2 watts max (1.7 watts typ)	*
TEMPERATURE RANGE		
Specification	0 to +70°C	-55°C to +125°C
Storage	-55°C to +85°C[4]	-55°C to +150°C

NOTES:
[1] With 500Ω, 1% fixed resistor in place of Gain Adjust pot.
[2] Conversion time of ADC Section.
[3] One TTL Load is defined as I_{IL} = -1.6mA max @ V_{IL} = 0.4V, I_{IH} = 40μA max @ V_{IH} = 2.4V.
One LS TTL Load is defined as I_{IL} = -0.36mA max @ V_{IL} = 0.4V, I_{IH} = 20μA max @ V_{IH} = 2.7V.
[4] AD363K External Hold Capacitor is limited to +85°C; Analog Input Section and ADC Section may be stored at up to +150°C.

*Specifications same as AD363K.
Specifications subject to change without notice.



AD363 Analog Input Section Functional Block Diagram and Pinout



AD363 ADC Section (AD572) Functional Diagram and Pinout

PIN FUNCTION DESCRIPTION

ANALOG INPUT SECTION

Pin Number	Function
1	Single-End/Differential Mode Select "0": Single-Ended Mode "1": Differential Mode
2	Digital Ground
3	Positive Digital Power Supply, +5V
4	"High" Analog Input, Channel 7
5	"High" Analog Input, Channel 6
6	"High" Analog Input, Channel 5
7	"High" Analog Input, Channel 4
8	"High" Analog Input, Channel 3
9	"High" Analog Input, Channel 2
10	"High" Analog Input, Channel 1
11	"High" Analog Input, Channel 0
12	**Hold Capacitor (Provided)**
13	**Sample-Hold Command** "0": Sample Mode "1": Hold Mode Normally Connected to ADC Pin 20
14	Offset Adjust (See Figure 6)
15	Offset Adjust (See Figure 6)
16	Analog Output Normally Connected to ADC "Analog In"
17	Analog Ground
18	"High" ("Low") Analog Input, Channel 15 (7)
19	"High" ("Low") Analog Input, Channel 14 (6)
20	Negative Analog Power Supply, -15V
21	Positive Analog Power Supply, +15V
22	"High" ("Low") Analog Input, Channel 13 (5)
23	"High" ("Low") Analog Input, Channel 12 (4)
24	"High" ("Low") Analog Input, Channel 11 (3)
25	"High" ("Low") Analog Input, Channel 10 (2)
26	"High" ("Low") Analog Input, Channel 9 (1)
27	"High" ("Low") Analog Input, Channel 8 (0)
28	Input Channel Select, Address Bit AE
29	Input Channel Select, Address Bit A0
30	Input Channel Select, Address Bit A1
31	Input Channel Select, Address Bit A2
32	Input Channel Select Latch "0": Latched "1": Latch "Transparent"

ANALOG TO DIGITAL CONVERTER SECTION

Pin Number	Function
1	Data Bit 12 (Least Significant Bit) Out
2	Data Bit 11 Out
3	Data Bit 10 Out
4	Data Bit 9 Out
5	Data Bit 8 Out
6	Data Bit 7 Out
7	Data Bit 6 Out
8	Data Bit 5 Out
9	Data Bit 4 Out
10	Data Bit 3 Out
11	Data Bit 2 Out
12	Data Bit 1 (Most Significant Bit) Out
13	$\overline{\text{Data Bit 1}}$ ($\overline{\text{MSB}}$) Out
14	Short Cycle Control Connect to +5V for 12 Bits Connect to Bit (n+1) Out for n Bits
15	Digital Ground
16	Positive Digital Power Supply, +5V
17	$\overline{\text{Status}}$ Out "0": Conversion in Progress (Parallel Data Not Valid) "1": Conversion Complete (Parallel Data Valid)
18	+10Volt Reference Out
19	Clock Out (Runs During Conversion)
20	Status Out "0": Conversion Complete (Parallel Data Valid) "1": Conversion in Progress (Parallel Data Not Valid)
21	Convert Start In Reset Logic : ⎍↑ Start Convert : ↓⎍
22	Comparator In
23	Bipolar Offset Open for Unipolar Inputs Connect to ADC Pin 22 for Bipolar Inputs (See Figure 8)
24	10V Span R In (See Figure 7)
25	20V Span R In (See Figure 8)
26	Analog Ground
27	Gain Adjust (See Figures 7 and 8)
28	Positive Analog Power Supply, +15V
29	Buffer Out (For External Use)
30	Buffer In (For External Use)
31	Negative Analog Power Supply, -15V
32	Serial Data Out Each Bit Valid On Trailing (↓⎍) Edge Clock Out, ADC Pin 19

ANALOG DEVICES

Fast, Complete, 16-Channel µP Compatible 12-Bit Data Acquisition System

AD364

ADVANCED TECHNICAL DATA

FEATURES

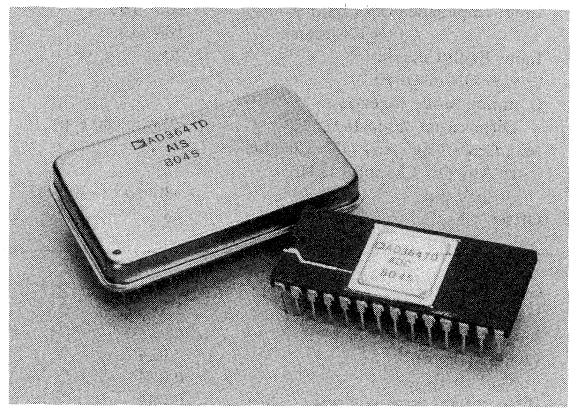
- Complete Data Acquisition System in 2-Package IC Form
- Full 8- or 16-Bit Microprocessor Bus Interface
- 16 Single-Ended or 8 Differential Channels with Switchable Mode Control
- True 12-Bit Operation: Nonlinearity ≤±0.012%
- Guaranteed No Missing Codes Over Specified Temperature Range
- High Throughput Rate: 20kHz
- Fast Successive Approximation Conversion: 25µs
- Buried Zener Reference for Long-Term Stability and Low Gain TC
- Small Size: Requires Only 2.8 Square Inches
- Short-Cycle Capability
- Low Power: 1.4 Watts
- Military/Aerospace Temperature Range: -55°C to +125°C MIL-STD-883 Class B Processing Available

PRODUCT DESCRIPTION

The AD364 is a complete 16 channel, microprocessor compatible, 12-bit data acquisition system in integrated circuit form. The AD364 design is implemented with linear compatible LSI chips, active laser trimming and hybrid technology resulting in maximum performance and flexibility.

The AD364 consists of two separate functional blocks, each in a hermetically sealed dual-in-line package. The analog input section contains two eight-channel multiplexers, a differential amplifier, a sample-and-hold, a channel address register and control logic. The multiplexers may be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A unique feature of the AD364 is an internal user-controllable analog switch that connects the multiplexers in either a single-ended or differential mode. This allows a single device to perform in either mode without hard-wire programming and permits a mixture of single-ended and differential sources to be interfaced to an AD364 by dynamically switching the input mode control.

The ADC section contains a complete 12-bit successive approximation ADC, including internal clock, precision 10 volt reference, comparator and bus interface. The ADC uses the newly-developed LCI (Linear-Compatible Integrated Injection Logic) process to provide the low power logic necessary to make a high speed 12-bit ADC and 3-state output buffer circuitry for direct interface to an 8-, 12- or 16-bit microprocessor bus.



The AD364 is available in 4 different grades. The AD364J and K grades are specified for operation over the 0 to +70°C temperature range. The AD364S, T are specified for the -55°C to +125°C range.

PRODUCT HIGHLIGHTS

1. The precision laser-trimmed scaling and bipolar offset resistors provide three calibrated ranges; 0 to +10 volts unipolar, or -5 to +5 and -10 to +10 volts bipolar. Typical bipolar offset and full scale calibration errors of ±0.05% can be trimmed to zero each with one external component.
2. The internal buried zener reference is trimmed to 10.00 volts with a ±1% maximum error and 15ppm/°C typical TC. The reference is available externally and can drive up to 1.5mA beyond that required for the reference and bipolar offset resistors.
3. The AD364 interfaces to most popular microprocessors with an 8-, 12-, or 16-bit bus without external buffers or peripheral interface controllers. Multiple-mode three-state output buffers connect directly to the data bus while the read and convert commands are taken from the control bus. The 12 bits of output data can be read either as one 12-bit word or as two 8-bit bytes (one with 8 data bits, the other with 4 data bits and 4 trailing zeros).

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This four-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be found in Volume I, page 15-25.

SPECIFICATIONS (typical @ +25°C, ±15V and +5V with 2000pF hold capacitor as provided unless otherwise noted)

PARAMETER	AD364J	AD364K	AD364S	AD364T	UNITS
ANALOG INPUTS					
Number of Inputs	16 Single-Ended or 8 Differential (Electronically Selectable)				
Input Voltage Range					
T_{min} to T_{max}	±10	*	*	*	V
Input (Bias) Current per Channel	±50	*	*	*	nA max
Input Impedance ON Channel	10^{10}/100	*	*	*	Ω/pF
OFF Channel	10^{10}/10	*	*	*	Ω/pF
Input Fault Current	20	*	*	*	mA max
(Power ON or OFF)					(Internally
Common Mode Rejection					Limited)
Differential Mode 1kHz 20Vp-p	70 min (80 typ)	*	*	*	dB
Mux Cross Talk (Any OFF Channel					
to Any ON Channel) 1kHz					
20V p-p	-80 max (-90 typ)	*	*	*	dB
Offset, Channel to Channel	±5	*	*	*	mV max
ACCURACY					
Gain Error[1]	0.3	*	*	*	% of FSR
Unipolar Offset Error[2]	±10	±8	*	**	mV
Bipolar Offset Error[2]	±50	±20	*	**	mV
Linearity Error	0.024	0.012	*	**	% of FSR max
T_{min} to T_{max}	0.024	0.012	*	*	% of FSR max
Differential Linearity Error	0.024	0.012	*	**	% of FSR max
T_{min} to T_{max}	0.024	0.012	*	*	% of FSR max
Noise Error	1mV p-p 0.1Hz to 1MHz	*	*	*	
TEMPERATURE COEFFICIENTS					
Gain	54	31	*	**	ppm/°C
Offset (±10V Range)	12	7	*	**	ppm/°C
Operating Temperature Range	0 to +70°C	*	-55°C to +125°C	***	ppm/°C
SIGNAL DYNAMICS					
Conversion Time	32 max (25 typ)	*	*	*	μs
Throughput Rate, Full Accuracy	20 min (25 typ)	*	*	*	kHz
Sample Hold					
Aperture Delay	100 max (50 typ)	*	*	*	ns
Aperture Uncertainty	500 max (100 typ)	*	*	*	ps
Acquisition Time					
To 0.01% of Final Value					
For Full Scale Step	18 max (10 typ)	*	*	*	μs
Feedthrough at 1kHz	-70 max (-80 typ)	*	*	*	dB
Droop Rate	2 max (1 typ)	*	*	*	mV/ms
DIGITAL INPUT SIGNALS					
Analog Input Section					
Input Channel Select	4 Bit Binary Address	*	*	*	
	1 LS TTL Load	*	*	*	
Channel Select Latch	"1" Latch Transparent	*	*	*	
	"0" Latched	*	*	*	
	4 LS TTL Loads	*	*	*	
Single Ended/Differential	"0" Single Ended	*	*	*	
Mode Select	"1" Differential	*	*	*	
	3TTL Loads	*	*	*	
Sample and Hold Command	"0" Sample Mode	*	*	*	
	"1" Hold Mode	*	*	*	
	1TTL Load	*	*	*	
ADC Section[3] $4.5 \leqslant V_L \leqslant 5.5$					
Logic Input Threshold					
T_{min} to T_{max}					
Logic "1"	2.0	*	*	*	V min
Logic "0"	0.8	*	*	*	V max
Logic Input Current					
T_{min} to T_{max}					
Logic "1"	10	*	*	*	μA max
Logic "0"	10	*	*	*	μA max

PARAMETER	AD364J	AD364K	AD364S	AD364T	UNITS
DIGITAL OUTPUT SIGNALS					
Logic Outputs T_{min} to T_{max}					
Sink Current V_{OUT} = 0.4V	1.6	*	*	*	mA min
Source Current V_{OUT} = 2.4V	0.5	*	*	*	mA min
Output Leakage When In Three State	±40	*	*	*	μA max
Output Coding					
Unipolar	Positive True Binary	*	*	*	
Bipolar	Positive True Offset Binary	*	*	*	
POWER REQUIREMENTS					
Supply Voltages/Currents	+15V, ±5% @ 36mA max	*	*	*	
	−15V, ±5% @ 65mA max	*	*	*	
	+5V, ±5% @ 75mA max	*	*	*	

[1] With 50Ω resistor from REF IN to REF OUT. Adjustable to zero.
[2] Adjustable to zero.
[3] 12/$\overline{8}$ line must be hard wired to V_{LOGIC} or digital common.
*Specifications same as AD364J.
**Specifications same as AD364K.
***Specifications same as AD364S.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (ALL MODELS)

+V, Digital Supply	+5.5V
+V, Analog Supply	+16V
−V, Analog Supply	−16V
V_{IN}, Signal	±V, Analog Supply
V_{IN}, Digital	0 to +V, Digital Supply
A_{GND} to D_{GND}	±1V

PROCESSING TO MIL-STD-883

All models of AD364 ordered to the requirements of MIL-STD-883B, Method 5008 are identified with a /883B suffix and receive the following processing:

PROCESS	CONDITIONS
1) 100% pre-cap Visual Inspection	2017.1
2) Stabilization Bake	1008, 24 hours @ +150°C
3) Temperature Cycle	1010, Test Condition C, 10 cycles, −65°C to +150°C
4) Constant Acceleration	2001, Y1 Plane, 1000G
5) Visual Inspection	Visable Damage
6) Operating Burn-In	1015, Test Condition B 160 hours @ +125°C
7) Seal Test: Fine Leak	1014, Test Condition A, 5 x 10^{-7} std cc/sec
Gross Leak	1014, Condition C
8) Final Electrical Test	Per Data Sheet
9) External Visual Inspection	2009

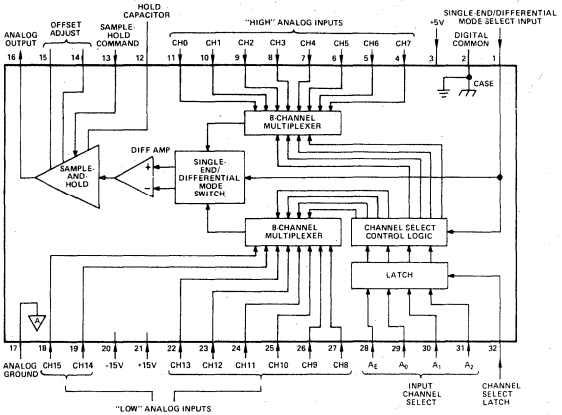


Figure 1. AD364 Analog Input Section Functional Block Diagram and Pinout

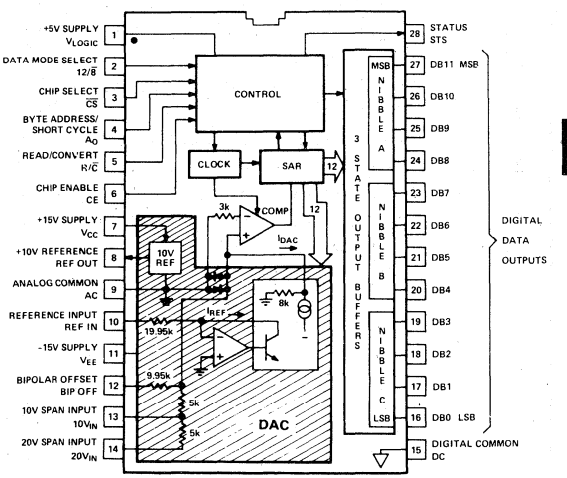


Figure 2. ADC Section Functional Block Diagram and Pinout

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PIN FUNCTION DESCRIPTION

ANALOG INPUT SECTION

Pin Number	Function
1	Single-End/Differential Mode Select "0": Single-Ended Mode "1": Differential Mode
2	Digital Common
3	Positive Digital Power Supply, +5V
4	"High" Analog Input, Channel 7
5	"High" Analog Input, Channel 6
6	"High" Analog Input, Channel 5
7	"High" Analog Input, Channel 4
8	"High" Analog Input, Channel 3
9	"High" Analog Input, Channel 2
10	"High" Analog Input, Channel 1
11	"High" Analog Input, Channel 0
12	Hold Capacitor (Provided, See Figure 3)
13	Sample-Hold Command "0": Sample Mode "1": Hold Mode Normally Connected to ADC Pin 28
14	Offset Adjust (See Figure 7)
15	Offset Adjust (See Figure 7)
16	Analog Output Normally Connected to ADC "Analog In" (See Figure 3)
17	Analog Common
18	"High" ("Low") Analog Input, Channel 15 (7)
19	"High" ("Low") Analog Input, Channel 14 (6)
20	Negative Analog Power Supply, -15V
21	Positive Analog Power Supply, +15V
22	"High" ("Low") Analog Input, Channel 13 (5)
23	"High" ("Low") Analog Input, Channel 12 (4)
24	"High" ("Low") Analog Input, Channel 11 (3)
25	"High" ("Low") Analog Input, Channel 10 (2)
26	"High" ("Low") Analog Input, Channel 9 (1)
27	"High" ("Low") Analog Input, Channel 8 (0)
28	Input Channel Select, Address Bit AE
29	Input Channel Select, Address Bit A0
30	Input Channel Select, Address Bit A1
31	Input Channel Select, Address Bit A2
32	Input Channel Select Latch "0": Latched "1": Latch "Transparent"

ANALOG TO DIGITAL CONVERTER SECTION

Pin Number	Function
1	Logic Power Supply, +5V
2	Data Mode Select (12/$\overline{8}$) "0": 8 Upper Bits or 4 Lower Bits as Selected by Byte Select (A_0)
3	Chip Select ($\overline{CS}$) "0": Device Selected "1": Device Inhibited
4	Byte Address/Short Cycle (A_0) "0": Upper 8 Bits Enabled (12/$\overline{8}$ "0")/ 12 Bit Cycle "1": Lower 4 Bits Enabled (12/$\overline{8}$ "1")/ 8 Bit Cycle
5	Read Convert (R/$\overline{C}$) "0": Convert Start "1": Read Enable
6	Chip Enable (CE) ↓: R/$\overline{C}$ "0", $\overline{CS}$ "0" Initiates Conversion ↓: R/$\overline{C}$ "1", $\overline{CS}$ "0" Initiates Read "0": Device Disabled "1": Device Enabled
7	Analog Power Supply, +15V (V_{CC})
8	Reference Out, +10V
9	Analog Common (AC)
10	Reference In
11	Analog Power Supply, -15V (V_{EE})
12	Bipolar Offset
13	10 Volt Span Input
14	20 Volt Span Input
15	Digital Common (DC)
16	Data Bit 0
17	Data Bit 1
18	Data Bit 2
19	Data Bit 3
20	Data Bit 4
21	Data Bit 5
22	Data Bit 6
23	Data Bit 7
24	Data Bit 8
25	Data Bit 9
26	Data Bit 10
27	Data Bit 11
28	Status Out

ANALOG DEVICES

Low-Cost, High Speed Data Acquisition Module

DAS1128

FEATURES
- **Complete Data Acquisition System**
- **12-Bit Digital Output**
- **16 Single or 8 Differential Analog Inputs**
- **High Throughput Rate**
- **Selectable Analog Input Ranges**
- **Versatile Input/Output/Control Format**
- **Low 3 Watt Power Dissipation**
- **Small 3" x 4.6" x 0.375" Module**



GENERAL DESCRIPTION

The DAS1128 is a complete self-contained miniature high speed data acquisition system. The compact 3" x 4.6" x 0.375" module provides the designer with an easily implemented solution to the data acquisition problem. It contains an analog input signal multiplexer, a sample-and-hold amplifier, a 12-bit A/D converter, and all of the programming, timing and control circuitry needed to perform the complete data acquisition function.

The DAS1128 is a high performance device which can digitize an analog signal to an accuracy of ±½LSB out of 12 bits, relative to full scale. It has ±8ppm/°C gain temperature coefficient, and the maximum throughput rate can be varied from 50,000 conversions/second for a 12 bit conversion from different analog input channels, to 200,000 conversions/second for a successive 4-bit conversion made on a single channel.

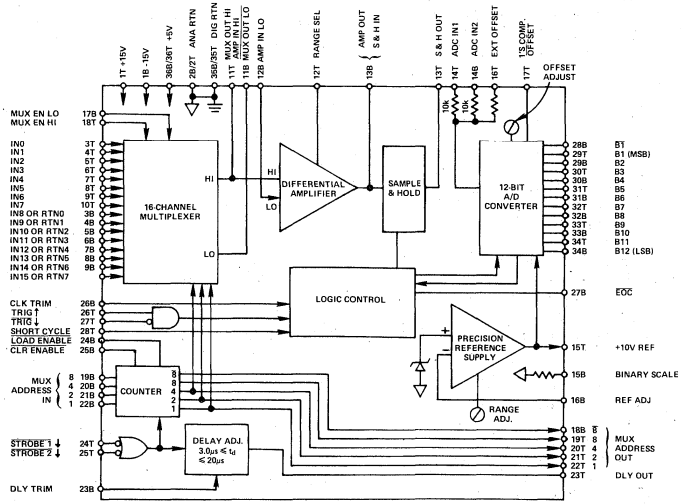


Figure 1. Functional Block Diagram

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SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

ANALOG INPUTS

Number of Inputs to Multiplexer	16 Single Ended, 8 True-Differential, 16 Pseudo-Differential
Input Voltage (Full Scale Range)	-10V to +10V, 0V to +10V, -5V to +5V, 0V to +5V, -10.24V to +10.24V, 0V to +10.24V, -5.12V to +5.12V, or 0V to +5.12V.
Maximum Input Voltage	±15V
Input Current (per channel)	5nA max
Input Impedance	$>10^{10}$ ohms
Input Capacitance	10pF for "OFF" channel 100pF for "ON" channel
Input Fault Current (power off or MUX failure)	Internally limited to 20mA
Direct ADC Input Impedance	10kΩ for each input line

ACCURACY[1]

Resolution	12 Bits
Error Relative to F.S.	±½LSB
Quantization Error	±½LSB
Differential Nonlinearity Error	
@ 33kHz throughput rate	±½LSB, 1LSB max
@ 50kHz throughput rate	±1LSB
Noise Error	±¼LSB
-FS to +FS Error Between Successive Channel Transitions	±1LSB

TEMP. COEFFICIENTS

Gain	8ppm/°C, 20ppm/°C max
Offset	5ppm/°C, 15ppm/°C max
Differential Nonlinearity	2.5ppm/°C, 6ppm/°C max

SIGNAL DYNAMICS

Throughput Rate (12 Bits)	50kHz (max) (includes 5μs for MUX and SHA settling time plus 15μs for ADC)
MUX Crosstalk ("OFF" channels to "ON" channel)	>80dB down @ 1kHz
Differential Amplifier CMRR	70dB to 1kHz
SHA Acquisition Time to 0.01%	4.5μs max
SHA Aperture Uncertainty	10ns
SHA Feedthrough	70dB down @ 1kHz

DIGITAL INPUT SIGNALS

Compatibility	Standard DTL/TTL logic levels, 1 unit load/line
MUX Address Inputs (8, 4, 2, 1; Pins 19B through 22B)	Positive true natural binary coding selects channel for random addressing mode. Must be stable for 100ns after $\overline{\text{STROBE}}$.
MUX ENABLE HI (Pin 18T)	High (Logic "1") input enables MUX "HI" output (for inputs 0 through 7)
MUX ENABLE LO (Pin 17B)	High (Logic "1") input enables MUX "LO" output (for inputs 8 through 15)
$\overline{\text{STROBE}}$ (Pin 24T or 25T)	Negative going transition (Logic "1" to Logic "0") updates MUX address register. $\overline{\text{STROBE}}$ 1 must be a Logic "1" to enable $\overline{\text{STROBE}}$ 2. $\overline{\text{STROBE}}$ 2 must be at Logic "1" to enable $\overline{\text{STROBE}}$ 1.
$\overline{\text{LOAD ENABLE}}$ (Pin 24B)	High (Logic "1") input allows next $\overline{\text{STROBE}}$ command to sequentially advance MUX address register. Low (Logic "0") input allows next $\overline{\text{STROBE}}$ command to update MUX address register according to external address inputs.
$\overline{\text{CLEAR ENABLE}}$ (Pin 25B)	Low (Logic "0") input allows next $\overline{\text{STROBE}}$ command to reset MUX address to channel "0" overriding $\overline{\text{LOAD ENABLE}}$.
TRIGGER (Pin 26T)	Positive going transition (Logic "0" to Logic "1") initiates A/D conversion (even during conversion); $\overline{\text{TRIGGER}}$ (Pin 27T) must be at Logic "0" to allow TRIGGER function.
$\overline{\text{TRIGGER}}$ (Pin 27T)	Negative going transition (Logic "1" to Logic "0") initiates A/D conversion; Pin 26T (TRIGGER) must be at Logic "1" to allow $\overline{\text{TRIGGER}}$ function.

[1] Warmup time to rated accuracy is 5 minutes.
[2] Specification applies only when tracking +15V and -15V supplies are used, and for slowly occuring variations in power supply voltages.

Specifications subject to change without notice.

DIGITAL OUTPUT SIGNALS

Compatibility	Standard DTL/TTL logic levels; 5 unit loads/line.
Parallel Outputs	$\overline{\text{B1}}$, B1 through B12
Coding	Natural binary, two's complement, offset binary, or one's complement. Pin selectable.
MUX Address Outputs ($\overline{8}$, 8, 4, 2, 1; pins 18B, 19T through 22T)	Positive true natural binary coding indicates channel selected.
DELAY OUT (Pin 23T)	Negative going transition (Logic "1" to Logic "0") occurring normally 5μs (adjustable from 3.0μs to 20μs) after $\overline{\text{STROBE}}$ command initiates A/D conversion automatically when connected to the $\overline{\text{TRIGGER}}$.
$\overline{\text{EOC}}$ (Pin 27B)	High (Logic "1") output during A/D conversion.

ADJUSTMENTS & TRIMS

Offset Adjust	
Internal Adjustment (Externally Accessible)	±10LSBs (min)
Remote External Adjustment (Pin 16T)	±10LSBs (min)
Range Adjust	
Internal Adjustment (Externally Accessible)	±10LSBs (min)
Remote External Adjustment (Pin 16B)	±10LSBs (min)
Clock Trim (Pin 26B)	
Factory Setting (Pin 26B "OPEN")	1.25μs/Bit
External Adjustment Range	1.25μs/Bit to 2.08μs/Bit
Delay Trim (Pin 23B)	
Factory Setting (Pin 23B "OPEN")	3.0μs
External Adjustment Range	3.0μs to 20μs

CONTROLS

SHORT CYCLE (Pin 28T)	Connect to ground for full 12 bit resolution. Connect to B_n output for resolution to B_{n-1} bits.
Channel Selection Mode (MUX Address Loading Mode)	Random, sequential continuous, and sequential triggered. Pin selectable.
A-D Conversion/Channel-Select Sequences	Normal (input channel remains selected during its A/D conversion) and overlap (next channel selected during A/D conversion). Pin selectable.
Range Select (Pin 12T)	Differential Amplifier gain control: connect to ANA RTN (Pin 2T) for X1 gain; connect to AMP OUT (Pin 13B) for X2 gain. This control is used in FSR selection procedure.
BINARY SCALE (Pin 15B)	Connect to REF ADJ (Pin 16B) to set reference to 10.24V. This control is used in FSR selection procedure, see Table II.
OUTPUT CODING (Pin 17T)	Ground for 1's complement output code; connect to -15V dc for other available codes.

POWER REQUIREMENTS

+15V ±3%	40mA, 50mA max
-15V ±3%	70mA, 100mA max
+5V ±5%	250mA, 500mA max
Power Supply Sensitivity[2]:	
Gain	±2.0mV/V
Offset	±4.0mV/V
Ref	±0.5mV/V

ENVIRONMENT & PHYSICAL

Operating Temperature	0 to +70°C
Storage Temperature	-25°C to +85°C
Relative Humidity	Up to 95% noncondensing
Electrical Shielding	RFI & EMI 6 sides (except connector area)
Packaging	Insulated steel cased module 3.00" x 4.60" x 0.375"

THEORY OF OPERATION

A block diagram of the DAS1128 is shown in Figure 1. Analog input signals are applied to the various inputs of the 16 channel CMOS multiplexer. This multiplexer in conjunction with the differential amplifier that follows it, can be configured by the user to accept 16 single ended analog inputs, or 8 fully differential analog inputs. It can also be connected as a 16 channel "pseudo-differential" input device, which permits some of the benefits of differential operation while maintaining a 16 channel input capability.

The differential buffer amplifier is gain programmable by the user via jumpers at the module pins. This feature, along with the selectable reference voltages, permits the user to set up the DAS1128 to operate on any of 8 input voltage ranges. The differential amplifier drives a sample-and-hold amplifier, whose function it is to hold the selected analog input signal at a constant level while the A/D converter is making a conversion.

The A/D converter is a high speed 12-bit successive approximation device that has been designed using the Analog Devices' AD562, 12-bit integrated circuit D/A. The reference voltage for the conversion is supplied by an adjustable precision reference circuit that has a temperature coefficient of 5ppm/°C.

In addition to these basic functional blocks, the DAS1128 also contains all of the clock circuitry necessary to perform the complete data acquisition function. The internal clock can be externally adjusted to provide various throughput rates at different accuracies. Input channel addressing logic is provided, as is the capability to short cycle the A/D converter (i.e. perform conversions of less than 12-bits resolution). It is also possible for the user to adjust the time interval between input channel selection and the commencement of a conversion. The user can thus trade off speed vs. accuracy in the settling time of the multiplexer and sample-and-hold amplifier, as well as speed versus accuracy of the A/D converter.

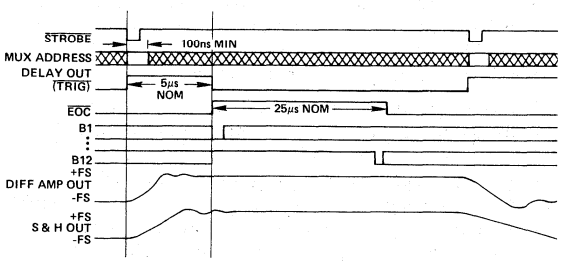


Figure 2. Simplified Timing Diagram, Showing Time-Interval Assignments and Constants

INPUT CONNECTIONS

As shown in Figure 3, three input configurations can be used. 16 single-ended inputs (3a) can be connected to the multiplexer, all referenced to analog gnd. In the second configuration (3b), the inputs are connected individually as 8 true differential pairs. In this case the differential amplifier is connected "Differentially" with the output of the MUX. Finally, a "Quasi-Differential" connection (3c) can be realized under favorable ground path conditions. In this configuration the differential amplifier Lo terminal is used as the ground return for all sensors. In each of these input schemes, it should be noted that the input multiplexer has been designed to protect itself and signal sources from both overvoltage failure and from fault currents due to power-off loading or MUX failure.

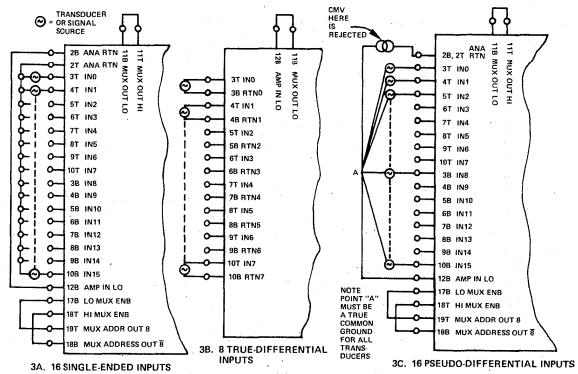


Figure 3. Signal Input Connections for Three Different Configurations

Full scale range of the DAS1128 may be set by appropriate jumper connections for 8 different ranges: 0 to +10V; 0 to +5V; 0 to +10.24V; 0 to +5.12V; -10 to +10V; -5 to +5V; -10.24 to +10.24V; -5.12 to +5.12V.

Note that 10.24 and 5.12 ranges are commonly used since conversion increments become 5mV/bit, 2.5mV/bit, and 1.25mV/bit.

MUX AND S/H DYNAMICS – OVERLAP MODE

The overlap mode is defined as the ability of MUX to accept a new channel address thereby selecting the next channel to be sampled while the previously acquired sample is being held by the S/H for conversion. The dynamic characteristics of the S/H circuit are shown in Figure 4. Maximum throughput rates are obtainable when a single channel is held at a single address and the channel is sampled repeatedly. In a dynamic condition, data-throughput rates obtainable are shown in Figure 5.

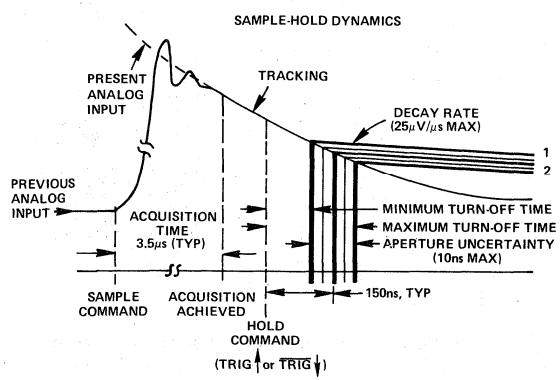


Figure 4. Sample-Hold Parameters Defined and Specified

SHORT CYCLE

It is possible to short cycle the DAC1128, i.e., stop the conversion after less than 12 bits. This can be done by connecting an external jumper between short cycle terminal and one of the output terminals. With shorter cycles the attainable throughput rate increases, see Figure 5. In short cycle operation the $\overline{EOC}$ will decrease proportionately to the number of bits selected. Note the short cycle terminal *must* be grounded for full 12-bit operation.

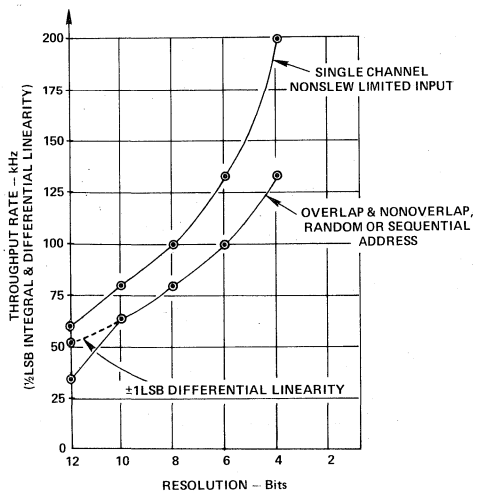
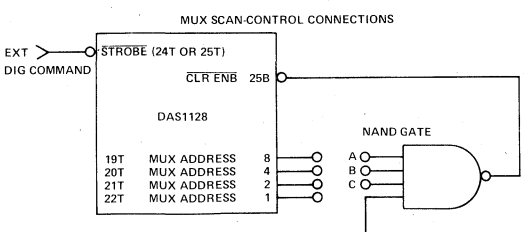


Figure 5. DAS1128 Throughput Rates

MUX ADDRESSING

External terminals have been provided for the address counter. Thus the address counter can be configured to produce the following modes: Continuous sequential scanning (free running), sequential scanning with external step command, abbreviated scan continuously, random channel selection. See Figure 6 and set up procedure for details.



LAST CHANNEL	MUX ADDRESS 8	4	2	1	DIG. GROUND
1	X	X	X	A	X
2	X	X	B	X	X
3	X	X	B	A	X
4	X	C	X	X	X
5	X	C	X	A	X
6	X	C	B	X	X
7	X	C	B	A	X
8	C	X	X	X	X
9	C	X	X	A	X
10	C	X	B	X	X
11	C	X	B	A	X
12	B	C	X	X	X
13	B	C	X	A	X
14	A	C	B	X	X
15	X	X	X	X	A

X = NO CONNECTION

IF $\overline{LOAD\ ENB}$ IS ALSO USED, CONNECT THIS INPUT TO IT (TO 24B). THIS GIVES LOADING PREFERENCE OVER CLEARING.

NOTE: FOR INITIAL CHANNEL = M, CONNECT GATE OUTPUT TO $\overline{LOAD\ ENB}$ (24B) AND CODE CHANNEL IN 8, 4, 2, 1 TO ADDRESS M. HOWEVER, THIS PRECLUDES RANDOM ADDRESSING.

Figure 6. To shorten scanning sequency of multiplexer channels, make the appropriate connections, (as shown in the chart) between an external NAND gate and MUX ADDRESS terminals 19T to 21T

GROUNDING CONSIDERATIONS

Attention should be given to the methods of connection for electrical returns and voltage reference points. Analog return (ANA RTN) and digital return (DIG RTN) are provided. The following rules should be applied when integrating the DAS1128 into the system.

1. If the ±15V power supply is floating (for optimum analog accuracy), connect its return to ANA RTN (Pin 2B or 2T). If the ±15V power supply is *not* floating, connect its return to DIG RTN (Pin 35T or 35B).
2. Connect the +5V supply return to DIG RTN (Pin 35T or 35B). If this supply also powers additional equipment, run separate, parallel returns to the equipment ground and to DIG RTN (Pin 35T or 35B).
3. To minimize signal grounding problems, single-ended input signals should only be returned to ANA RTN (Pin 2B or 2T). If this is not possible, then connect the input signals in either the "true differential" or "pseudo-differential" configurations (see Figure 3).
4. Connect computer ground to DIG RTN (Pin 35T or 35B). Use heavy wire or ground planes.
5. The computer chassis should be connected to the computer and power supply grounds at only one point.
6. Connect the third-wire ground from main ac power input to the computer power supply return.

GAIN AND OFFSET ADJUSTMENTS

The DAS1128 is calibrated with external gain and offset adjustment potentiometers connected as shown in Figure 7 and 8. The offset adjustment potentiometer has an adjustment range of at least ±10LSBs, and the gain range adjustment potentiometer has an adjustment range of at least ±10LSBs.

Offset calibration is not affected by changes in gain calibration, and should therefore be performed prior to gain calibration. Proper gain and offset calibration requires great care and the use of extremely sensitive and accurate reference instruments. The voltage standard used as a signal source must be very stable. It should be capable of being set to within ±1/10LSB of the desired value at any point within its range.

These adjustments are not made with zero and full scale input signals, and it may be helpful to understand why. An A/D converter will produce a given digital word output for a small range of input signals, the nominal width of the range being one LSB. If the input test signal is set to a value which should cause the converter to be on the verge of switching between two adjacent digital outputs, the unit can be calibrated so that it does switch at just that point. With a high speed convert command rate and a visual display, these adjustments can be performed in a very accurate and sensitive way. Analog Devices *Analog-Digital Conversion Notes* gives more detailed information on testing and calibrating A/D converters.

OFFSET CALIBRATION

For unipolar +10V operation set the input voltage precisely to +0.0012V and adjust the offset potentiometer until the converter is just on the verge of switching from 000000000000 to 000000000001.

For ±5V bipolar operation set the input voltage precisely to -4.9988V; for ±10V units set it to -9.9976V. Adjust the offset

potentiometer, Figure 7, until Offset Binary coded units are just on the verge of switching from 000000000000 to 000000000001 and Two's Complement coded units are just on the verge of switching 100000000000 to 100000000001.

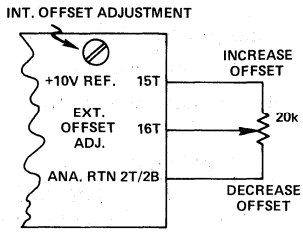


Figure 7. Ext. Offset Adjustment

GAIN CALIBRATION

Set the input voltage precisely to +9.9963V for unipolar operation, +4.9963V for inputs of ±5V or +9.9926V for inputs of ±10V. Note that these values are 1½LSBs less than nominal full scale. Adjust the 20k variable gain resistor, Figure 8, until Binary and Offset Binary coded units are just on the verge of switching from 111111111110 to 111111111111 and Two's Complement coded units are just on the verge of switching from 011111111110 to 011111111111.

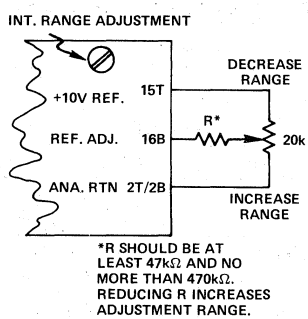


Figure 8. Ext. Ref. Adjustment

CLOCK RATE ADJUSTMENT

The clock rate may be adjusted for best conversion time/accuracy trade-off. The conversion time is varied by means of the external circuitry shown in Figure 9. An open CLK TRIM terminal (Pin 26B) results in 1.25μs/bit nominal conversion time. A grounded CLK TRIM terminal (for highest accuracy) results in 2.08μs/bit conversion.

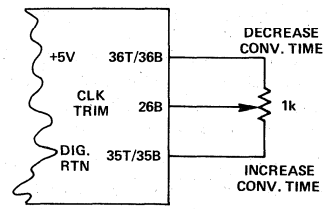


Figure 9. Clock Trim

DELAY TIME ADJUSTMENT

The DLY OUT signal may be adjusted to vary the A/D converter triggering time by means of the external circuitry shown in Figure 10. An open DLY TRIM terminal (Pin 23B) results in a nominal delay time of 3.0μs. A grounded DLY TRIM terminal (for highest-accuracy) results in 20μs delay time nominal.

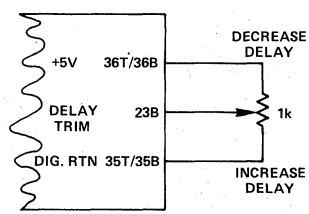


Figure 10. Delay Trim

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TABLE I

INPUT CONFIGURATION	ANALOG INPUT CONNECTIONS	ANALOG INPUT RETURN	JUMPER CONNECTIONS
16 Single-Ended Inputs (Figure 3a)	3T thru 10T and 3B thru 10B	All input returns to 2B or 2T	11B to 11T 12B to 2B or 2T 17B to 19T 18T to 18B
8 Differential Inputs (Figure 3b)	3T thru 10T	3B thru 10B	11B to 12B 17B to 18T to "1"
16 Pseudo-Differential Inputs (Figure 3c)	3T thru 10T and 3B thru 10B	Common Input return to 12B	11B to 11T 17B to 19T 18T to 18B

RECOMMENDED SET-UP PROCEDURE

1. Select input configuration, see Table I.
2. Select MUX address mode.
   The method of addressing the multiplexer can be selected by connecting the unit as follows:

   RANDOM. Set Pin 24B ($\overline{\text{LOAD ENB}}$) to Logic "0". The next falling edge of $\overline{\text{STROBE}}$ will load the address presented to Pins 19B through 22B (8, 4, 2, 1). The code on these lines must be stable during the falling edge of $\overline{\text{STROBE}}$ plus 100ns.

   SEQUENTIAL FREE RUNNING. Set to Logic "1", Pin 24B ($\overline{\text{LOAD ENB}}$) and 25B ($\overline{\text{CLR ENB}}$). Connect Pin 27B ($\overline{\text{EOC}}$) to Pin 24T ($\overline{\text{STROBE 1}}$). Connect Pin 23T (DLY OUT) to Pin 27T ($\overline{\text{TRIG}}$). Use Pin 26T ($\overline{\text{TRIG}}$) as a run/stop control (i.e., A/D conversion will continue while TRIG is high and will stop while TRIG is low).

   SEQUENTIAL TRIGGERED. Set to Logic "1", Pins 24B ($\overline{\text{LOAD ENB}}$) and 25B ($\overline{\text{CLR ENB}}$). Connect Pin 24T ($\overline{\text{STROBE}}$) to external triggering source. The multiplexer address register will automatically advance by one channel whenever a $\overline{\text{STROBE}}$ command is received. The initial channel can be selected by setting Pin 24B ($\overline{\text{LOAD ENB}}$) to Logic "0" during only one $\overline{\text{STROBE}}$ command. The multiplexer address will then be determined by the logic levels on Pins 19B through 22B (the external MUX address lines). Channel "0" can be selected as the initial channel by setting Pin 25B ($\overline{\text{CLR ENB}}$) to Logic "0" during only one $\overline{\text{STROBE}}$ command. The final channel can be selected by following the procedure presented in Figure 6.
3. Select A-D conversion/channel select sequence (see Figure 5).
   (1) NORMAL (input channel remains selected during its A/D conversion). Connect Pin 23T (DLY OUT) to Pin 27T ($\overline{\text{TRIG}}$).
   (2) OVERLAP (next channel is selected during A/D conversion). Connect Pin 27B ($\overline{\text{EOC}}$) to TTL compatible inverter input. Connect inverter output to Pin 24T ($\overline{\text{STROBE}}$). Connect Pin 23T (DLY OUT) to Pin 27T ($\overline{\text{TRIG}}$). Adjust the delay to at least 4μs greater than $\overline{\text{EOC}}$, 20μs max (see Figure 10). The signal on Pin 26T (TRIG) serves as RUN/STOP control.
   (3) REPETITIVE SINGLE CHANNEL. After selecting the input channel to be repetitively sampled (see MUX ADDRESS MODE, above), set Pin 27T ($\overline{\text{TRIG}}$) to Logic "0". Connect Pin 26T (TRIG) to a triggering source. Conversion process is initiated by positive edge of TRIG command.
4. Select output resolution.
   a. Full 12-bit resolution: connect Pin 28T (SHT CYC) to Pin 35B (DIG RTN).
   b. Bn (Bn $<$ 12) bit resolution: connect Pin 28T to the output pin for Bn + 1.
5. Select optimum throughput rate.
   The system clock frequency and the STROBE to TRIG delay (if used) can be trimmed to optimize the accuracy/throughput rate trade-off. See Figures 9 and 10.
6. Select input voltage full scale range. See Table II.
7. Select output digital coding. See Table III.

TABLE II

FOR FULL SCALE RANGE OF:	MAKE THE FOLLOWING CONNECTIONS
0 to +10V	12T to 2T; 14T to 14B to ADC Source*.
0 to +10.24V	same as 0 to +10V, *plus* 15B to 16B.
0 to +5V	12T to 13B; 14T and 14B to ADC Source*
0 to +5.12V	same as 0 to +5V, *plus* 15B to 16B
-10V to +10V	12T to 2T; 14T to 15T; and 14B to ADC Source*.
-10.24V to +10.24V	same as -10V to +10V, *plus* 15B to 16B
-5V to +5V	12T to 13B; 14T to 15T and 14B to ADC Source*.
-5.12V to +5.12V	same as -5V to +5V, *plus* 15B to 16B.

*ADC Source is usually Sample and Hold Output (13T), but may be any signal source including Diff. Amp. Output (13B) if Sample and Hold is not desired.

TABLE III

OUTPUT CODE	CONNECTIONS
Unipolar Binary	Connect 17T to -15V Use 29T (B1) for MSB
2's Complement	Connect 17T to -15V Use 28B ($\overline{\text{B1}}$) for MSB
Offset Binary	Connect 17T to -15V Use 29T (B1) for MSB
1's Complement	Connect 17T to 2B Use 28B ($\overline{\text{B1}}$) for MSB

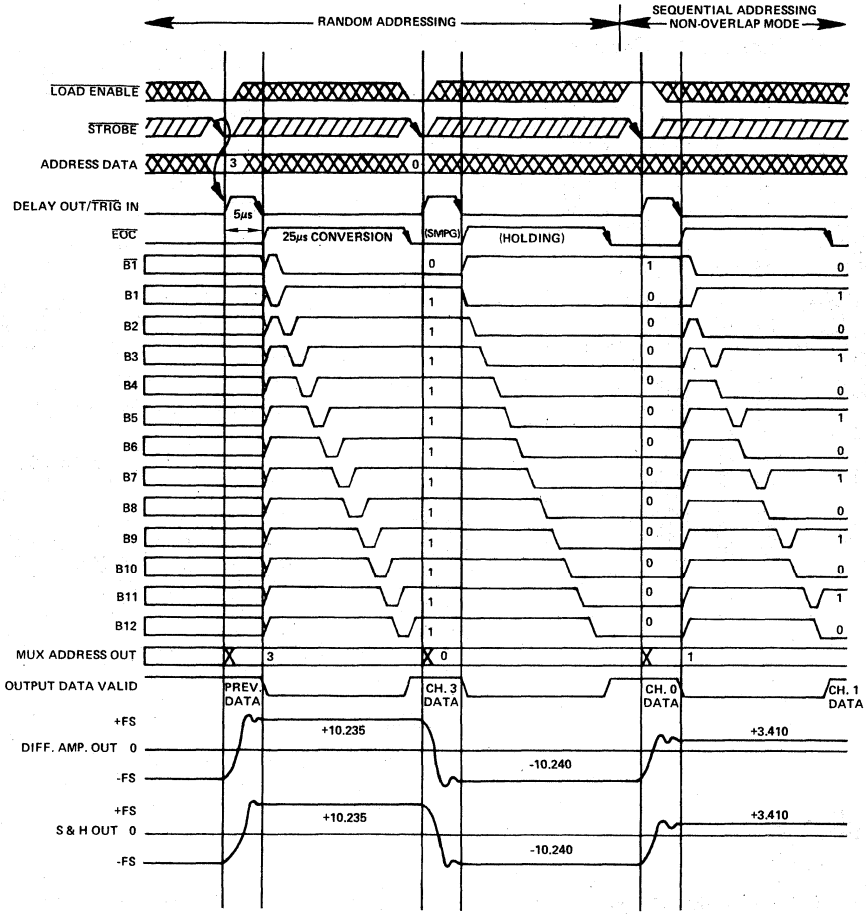


Figure 11. Timing for Non-Overlap Operation in Both Random and Sequential Addressing Modes. For Status Keys and Signal Condition Data, Refer to Box Below.

SIGNAL CONDITIONS AND STATUS KEYS FOR FIGURES 11 AND 12.

CH. 2 = -3.415V CODE 010 101 010 101
CH. 3 = +10.235V CODE 111 111 111 111
CH. 0 = -10.240V CODE 000 000 000 000
CH. 1 = +3.410V CODE 101 010 101 010

ADC SET UP FOR ±10.24V. INPUT, OFFSET BINARY. (FOR TWO'S COMPLEMENT, USE $\overline{B1}$ FOR MSB.)

KEY	INPUTS	OUTPUTS
XXX	May change	Don't know
///	May change 0 to 1	Changes 0 to 1
\\\	May change 1 to 0	Changes 1 to 0
OR	Must be stable	Will be stable

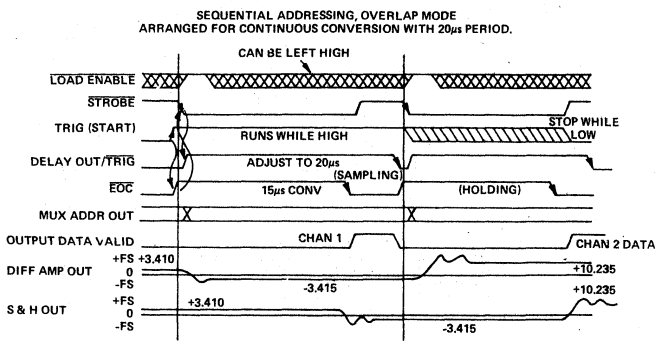


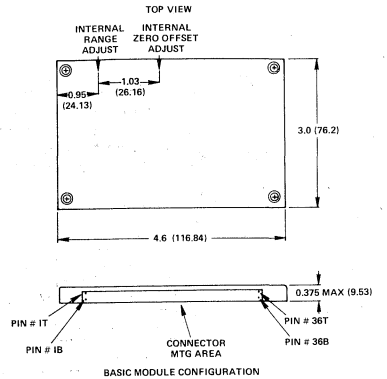
Figure 12. Timing Diagram for Overlap Operation in the Sequential Addressing Mode. For Status Keys and Signal Condition Data, See Box at Right.

Outline Drawings and Pin Designations

DAS1128 Connector Pin Diagram

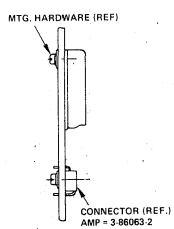
+15V	1T	1B	-15V	
ANA RTN	2T	2B	ANA RTN	
CH 0 IN	3T	3B	CH 8 IN	(CH 0 RTN)
CH 1 IN	4T	4B	CH 9 IN	(CH 1 RTN)
CH 2 IN	5T	5B	CH 10 IN	(CH 2 RTN)
CH 3 IN	6T	6B	CH 11 IN	(CH 3 RTN)
CH 4 IN	7T	7B	CH 12 IN	(CH 4 RTN)
CH 5 IN	8T	8B	CH 13 IN	(CH 5 RTN)
CH 6 IN	9T	9B	CH 14 IN	(CH 6 RTN)
CH 7 IN	10T	10B	CH 15 IN	(CH 7 RTN)
MUX HI OUT	11T	11B	MUX LO OUT	
RANGE SEL	12T	12B	AMP IN LO	
S & H OUT	13T	13B	AMP OUT	
ADC IN 1	14T	14B	ADC IN 2	
+10V REF	15T	15B	BINARY SCALE	
EXT OFFSET	16T	16B	REF ADJ	
OUTPUT CODING	17T	17B	ENABLE LO	
ENABLE HI	18T	18B	$\overline{8}$ OUT	
8 OUT / 4 OUT / 2 OUT / 1 OUT — MUX ADDRESS LINES	19T–22T	19B–22B	8 IN / 4 IN / 2 IN / 1 IN — MUX ADDRESS LINES	
DLY OUT	23T	23B	DLY TRIM	
$\overline{\text{STROBE 1}}$	24T	24B	$\overline{\text{LOAD ENB}}$	
$\overline{\text{STROBE 2}}$	25T	25B	CLR ENB	
TRIG	26T	26B	CLK TRIM	
$\overline{\text{TRIG}}$	27T	27B	$\overline{\text{EOC}}$	
SHT CYC	28T	28B	$\overline{\text{BT}}$ OUT	
B1 OUT	29T	29B	B2 OUT	
B3 OUT	30T	30B	B4 OUT	
B5 OUT	31T	31B	B6 OUT	
B7 OUT	32T	32B	B8 OUT	
B9 OUT	33T	33B	B10 OUT	
B11 OUT	34T	34B	B12 LSB OUT	
DIG RTN	35T	35B	DIG RTN	
+5V	36T	36B	+5V	

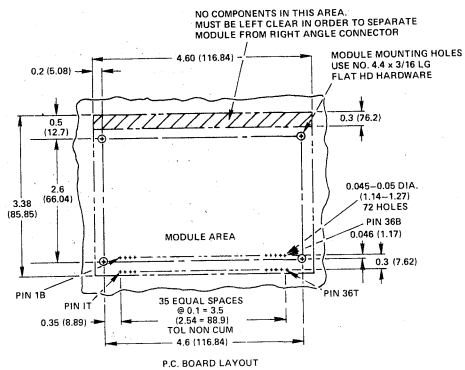
TOP VIEW



BASIC MODULE CONFIGURATION

Dimensions shown in inches and (mm).

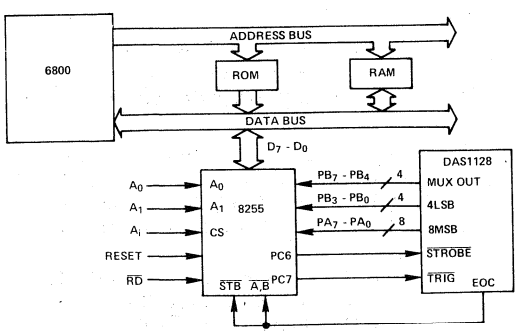




P.C. BOARD LAYOUT

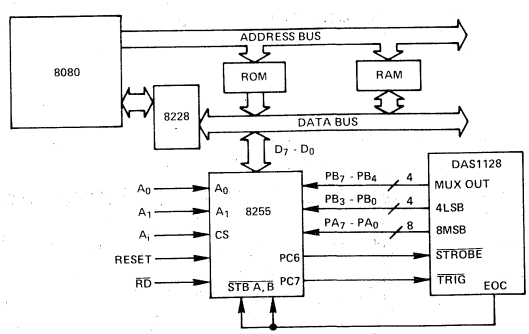
Typical Applications

DAS1128 WITH MOTOROLA 6800



NOTE:
1. 8255 USED IN MODE 1 (STROBED I/O)
2. PC6 INDEXES MUX TO DESIRED CHANNEL
3. CS TO A_i (WHERE, A_i IS AN ADDRESS BIT OTHER THAN A_0 OR A_1)
4. PC7 INITIATES CONVERSION
5. EOC STROBES IN DATA AND MUX INFO
6. 8255 SHOWN, HOWEVER 6820 CAN ALSO BE USED

DAS1128 WITH INTEL 8080



NOTE:
1. 8255 USED IN MODE 1 (STROBED I/O)
2. CS TO A_i (WHERE, A_i IS AN ADDRESS BIT OTHER THAN A_0 OR A_1)
3. PC6 INDEXES MUX TO DESIRED CHANNEL
4. PC7 INITIATES CONVERSION
5. EOC STROBES IN DATA AND MUX INFO

14-Bit & 15-Bit Sampling Analog To Digital Converter

DAS1152/DAS1153

FEATURES

- **Complete with High Accuracy Sample/Hold and A/D Converter**
- **Differential Nonlinearity: ±0.002% FSR max (DAS1153)**
- **Nonlinearity: DAS1152: ±0.005% FSR max**
  DAS1153: ±0.003% FSR max
- **Low Differential Nonlinearity T.C.: ±2ppm/°C max**
- **High Throughput Rate: 25kHz max (DAS1152)**
- **High Feedthrough Rejection: −96dB**
- **Byte-Selectable Tri-State Buffered Outputs**
- **Internal Gain & Offset Potentiometers**
- **Improved Second Source to A/D/A/M 824 and A/D/A/M 825 Modules**
- **Low Cost (100s)**

APPLICATIONS

- **Process Control Data Acquisition**
- **Automated Test Equipment**
- **Seismic Data Acquisition**
- **Nuclear Instrumentation**
- **Medical Instrumentation**
- **Robotics**

GENERAL DESCRIPTION

The DAS1152/DAS1153 are 14-/15-bit sampling analog-to-digital converters having a maximum throughput rate of 25kHz/20kHz. They provide high accuracy, high stability, and functional completeness all in a 2″ × 4″ × 0.44″ metal case.

Guaranteed high accuracy system performance such as nonlinearity of ±0.005% FSR (DAS1152)/±0.003% FSR (DAS1153) and differential nonlinearity of ±0.003% FSR (DAS1152)/±0.002% FSR (DAS1153) are provided. Guaranteed stability such as differential nonlinearity T.C. of ±2ppm/°C (DAS1153) maximum, zero T.C. of ±80μV/°C maximum, gain T. C. of ±8ppm/°C maximum and power supply sensitivity of ±0.001% FSR/% V_S are also provided by the DAS1152/DAS1153.

The DAS1152/DAS1153 make extensive use of both integrated circuit and thin film components to obtain their excellent performance, small size, and low cost. The devices contain a precision sample/hold amplifier, high accuracy 14-/15-bit analog-to-digital converter, tri-state output buffers, internal gain and offset trim potentiometers, and power supply bypass capacitors (as shown in Figure 1).



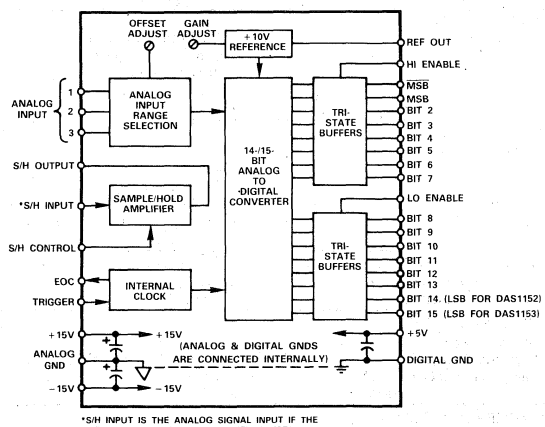


Figure 1. DAS1152/DAS1153 Block Diagram

Four analog input voltage ranges are selectable via user pin programming: 0 to +5V, 0 to +10V, ±5V, and ±10V. Unipolar coding is provided in true binary format with bipolar coding displayed in offset binary and two's complement. Tri-state buffers provide easy interface to bus structured applications.

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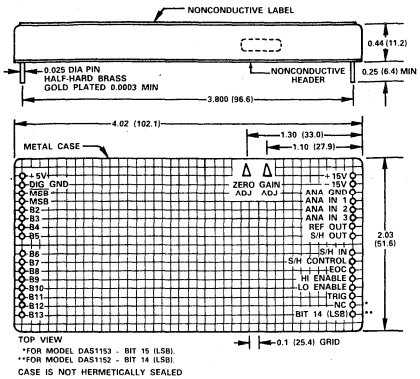
SPECIFICATIONS (typical @ +25°C unless otherwise specified)

MODEL	DAS1152	DAS1153
RESOLUTION	14 Bits	15 Bits
DYNAMIC PERFORMANCE		
Throughput Rate	25kHz min	20kHz min
Conversion Time	35µs max	44µs max
S/H Acquisition Time	4µs max	5µs max
S/H Aperture Delay	50ns	*
S/H Aperture Uncertainty	1ns	*
Feedthrough Rejection[1]	−96dB	*
Droop Rate	0.05µV/µs (0.1µV/µs max)	*
Dielectric Absorption Error	±0.005% of Input Voltage Change	*
ACCURACY		
Integral Nonlinearity[2]	±0.005% FSR[3] max	±0.003% FSR[3] max
Differential Nonlinearity	±0.003% FSR[3] max	±0.002% FSR[3] max
No Missing Codes	Guaranteed	*
±3σ Noise (S/H plus A/D)	75µV rms	*
±3σ Noise (A/D)	50µV rms	*
STABILITY		
Differential Nonlinearity T.C.	±2ppm/°C max	*
Gain T.C.	±8ppm/°C max	*
Zero T.C.	±30µV/°C typ, ±80µV/°C max	*
Power Supply Sensitivity	±0.001% FSR[3]/% V_s	*
ANALOG INPUT		
Voltage Range		
Bipolar	±5V, ±10V	*
Unipolar	0 to +5V, 0 to +10V	*
ADC Input Impedance 0 to +5V	2.5kΩ	*
0 to +10V, ±5V	5kΩ	*
±10V	10.0kΩ	*
S/H Input Impedance	100MΩ|5pF	*
DIGITAL INPUTS		
Convert Command[4]	1TTL Load, Positive Pulse	*
	Negative Edge Triggered	*
S/H Control	HOLD = Logic 0	*
	SAMPLE = Logic 1	*
Low Enable, High Enable	ENABLE = Logic 0	*
DIGITAL OUTPUTS		
Parallel Data Outputs		
Unipolar	Binary	*
Bipolar	Offset Binary, 2's Complement	*
Output Drive	2TTL Loads	*
Status	Logic "1" During Conversion	*
Output Drive	2TTL Loads	*
INTERNAL REFERENCE VOLTAGE	+10V, ±0.3%	*
External Load Current (Rated Performance)	2mA max	*
Temperature Stability	±5ppm/°C max	*
POWER REQUIREMENTS		
Rated Voltages	±15V (±3%), +5V (±5%)	*
Operating Voltages[5]	±12V to +17V, +4.75V to +5.25V	*
Supply Current Drain ±15V	±37mA	*
+5V	80mA	*
TEMPERATURE RANGE		
Specified	0 to +70°C	*
Operating	−25°C to +85°C	*
Storage	−25°C to +85°C	*
Relative Humidity	Meets MIL-STD-202E, Method 103B	*
Shielding	Electrostatic (RFI) 6 Sides,	*
	Electromagnetic (EMI) 5 Sides	*
SIZE	2" × 4" × 0.44" Metal Package	*

NOTES
*Specifications same as DAS1152
[1]Measured in hold mode, input 20V pk-pk @ 10kHz.
[2]Worst-case summation of S/H and A/D nonlinearity errors.
[3]FSR means Full Scale Range.
[4]When connecting the Convert Command and the S/H control terminals together, the pulse width must be long enough for the S/H amplifier to acquire the input signal to the required accuracy 4µs (max, DAS1152)/5µs (max, DAS1153). If the A/D converter is only used, the Convert Command pulse width should be 100ns min (see Figure 2).
[5]If only the ADC portion is used, the operating power supply voltage can be maintained at ±12V to ±17V. But if the S/H section is required, the operating voltage must be maintained at ±15V (±3%) or the S/H input voltage must be limited to −7V to +10V for a ±12V supply voltage.
[6]Recommended Power Supply: Analog Devices Model 923.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



OPERATION

The DAS1152/DAS1153 are functionally complete data acquisition subsystems being fully characterized as such. All the necessary data acquisition and microprocessor interface elements are provided internal to these devices. Accuracy and performance criteria are tested and specified for the entire system. Thus, design time and associated high accuracy problems are minimized because layout and component optimization have already been performed.

For operation, the only connections necessary to the DAS1152/DAS1153 are the ±15V and +5V power supplies, analog input signal, trigger pulse, and the HI-ENABLE/LO-ENABLE tri-state controls. Analog input and digital output programming are user selectable via external jumper connections.

ANALOG INPUT SECTION

The analog input can be applied to just the A/D converter or to the internal sample/hold amplifier ahead of the A/D converter. When using just the A/D converter, apply the analog input per the voltage range pin programming shown in Table 1. When using the sample/hold amplifier in conjunction with A/D converter, apply the analog input to the S/H INPUT terminal and connect the S/H OUTPUT terminal to the appropriate A/D converter analog input.

Analog Voltage Input Range	Connect V_{IN} or S/H Out To	Connect Analog Common To	Connect Ref Out To
0 to +5V	ANA IN 1, ANA IN 2, ANA IN 3	Ground	NC*
0 to +10V	ANA IN 2 ANA IN 3	Ground ANA IN 1	NC*
±5V	ANA IN 1	Ground, ANA IN 3	ANA IN 2
±10V	ANA IN 3	Ground, ANA IN 1	ANA IN 2

*No Connection

Table 1. Analog Input Pin Programming

Errors due to source loading are eliminated since the sample/hold amplifier is a high-impedance unity-gain amplifier. High feedthrough rejection is provided for either single-channel or multichannel applications. Feedthrough rejection can be optimized, in multichannel applications, by changing channels at the rising or falling edge of the S/H control pulse.

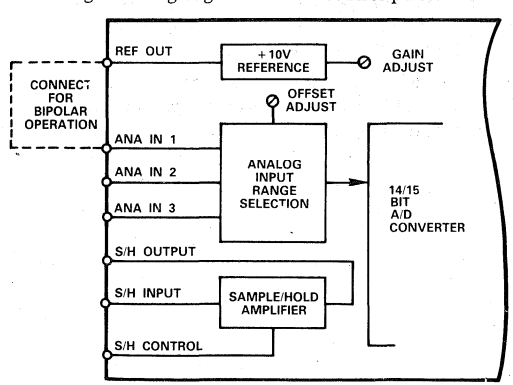


Figure 2. Analog Input Block Diagram

TIMING DIAGRAM

The timing diagram for the DAS1152/DAS1153 is illustrated in Figure 3. This figure also includes the sample/hold amplifier acquisition time.

If the sample/hold amplifier is required, the TRIGGER input and S/H CONTROL terminal can be tied together providing only one conversion control signal. When the trigger pulse goes high, it places the sample/hold amplifier in the sample mode allowing it to acquire the present input signal. The trigger pulse must remain high for a minimum of 4μs (DAS1152)/5μs (DAS1153) to insure accuracy is attained. If the sample/hold amplifier is not used, the trigger pulse needs to be only 100ns (min) in length to satisfy the A/D converter trigger requirements. At the falling edge of the trigger pulse, the sample/hold amplifier is placed in the hold mode, the A/D conversion begins, and all internal logic is reset. Once the conversion process is initiated, it cannot be retriggered until after the end of conversion.

With this negative edge of the trigger pulse the MSB is set low with the remaining digital outputs set to logic high state, and the status line is set high and remains high through the full conversion cycle. During conversion each bit, starting with the MSB, is sequentially switched low at the rising edge of the internal clock. The DAC output is then compared to the analog input and the bit decision is made. Each comparison lasts one clock cycle with the complete 14-/15-bit conversion taking 35μs/44μs maximum for the DAS1152/DAS1153 respectively. At this time, the STATUS line goes low signifying that the conversion is complete. For microprocessor bus applications, the digital output can now be applied to the data bus by enabling the tri-state buffers. For maximum data throughput, the digital output data should be read while the sample/hold amplifier is acquiring the new analog input signal.

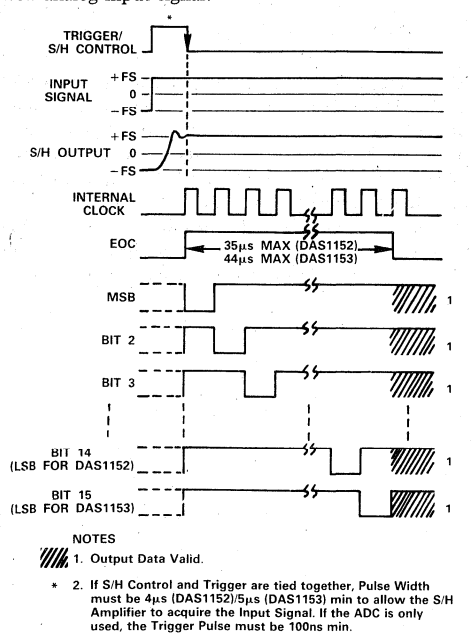


Figure 3. DAS1152/DAS1153 Timing Diagram

GAIN AND OFFSET ADJUSTMENT

The DAS1152/DAS1153 contain internal gain and offset adjustment potentiometers. Each potentiometer has ample adjustment range so that gain and offset errors can be trimmed to zero.

Since offset calibration is not affected by changes in gain calibration, it should be performed prior to gain calibration. Proper gain and offset calibration requires great care and the use of extremely sensitive and accurate reference instruments. The voltage standard used as a signal source must be very stable and be capable of being set to within ±1/10LSB of the desired value at any point within its range.

OFFSET CALIBRATION

For a 0 to +10V unipolar range set the input voltage precisely to +305μV for the DAS1152 and +153μV for the DAS1153. For a 0 to +5V unipolar range set the input to +153μV for the DAS1152 and +76μV for the DAS1153. Then adjust the zero potentiometer until the converter is just on the verge of switching from 000.....000 to 000.....001.

For the ±5V bipolar range set the input voltage precisely to +305μV for the DAS1152 and +153μV for the DAS1153. For a ±10V bipolar range set the input voltage precisely to +610μV for the DAS1152 and +305μV for the DAS1153. Adjust the zero potentiometer until the offset binary coded units are just on the verge of switching from 000.....000 to 000.....001 and the two's complement coded units are just on the verge of switching from 100.....000 to 100.....001.

GAIN CALIBRATION

Set the input voltage precisely to +9.99909V (DAS1152)/ +9.99954V (DAS1153) for the 0 to +10V units, +4.99954V (DAS1152)/+4.99977V (DAS1153) for 0 to +5V units, +9.99817V (DAS1152)/+9.99909V (DAS1153) for ±10V units, or +4.99909V (DAS1152)/+4.99954V (DAS1153) for ±5V units. Note that these values are 1 1/2LSBs less than nominal full scale. Adjust the gain potentiometer until binary and offset binary coded units are just on the verge of switching from 11.....10 to 11.....11 and two's complement coded units are just on the verge of switching from 011.....10 to 011.....11.

DAS1152/DAS1153 INPUT/OUTPUT RELATIONSHIPS

The DAS1152/DAS1153 produces a true binary coded output when configured as a unipolar device. Configured as a bipolar device, it can produce either offset binary or two's complement output codes. The most significant bit ($\overline{MSB}$) is used to obtain the binary and offset binary codes while ($\overline{MSB}$) is used to obtain two's complement coding. Table 2 shows the DAS1152/DAS1153 unipolar analog input/digital output relationships. Tables 3 and 4 show the DAS1152/DAS1153 bipolar analog input/digital output relationships.

NOMINAL BIPOLAR INPUT-OUTPUT RELATIONSHIPS

ANALOG INPUT			
0 to +5V Range		0 to +10V Range	
DAS1152	DAS1153	DAS1152	DAS1153
+4.99969V	+4.99984V	+9.99939V	+9.99969V
+2.50000V	+2.50000V	+5.0000V	+5.00000V
+0.62500V	+0.62500V	+1.25000V	+1.25000V
+0.0003V	+0.00015V	+0.0006V	+0.0003V
+0.0000V	+0.0000V	+0.0000V	+0.0000V

DIGITAL OUTPUT	
Binary Code	
DAS1152	DAS1153
11 111 111 111 111	111 111 111 111 111
10 000 000 000 000	100 000 000 000 000
00 100 000 000 000	001 000 000 000 000
00 000 000 000 001	000 000 000 000 001
00 000 000 000 000	000 000 000 000 000

Table 2. Unipolar Input-Output Relationships

Analog Input		Digital Output	
±5V Range	±10V Range	Offset Binary Code	Two's Complement Code
+4.99939V	+9.99878V	11 111 111 111 111	01 111 111 111 111
+2.50000V	+5.0000V	11 000 000 000 000	01 000 000 000 000
+0.00061V	+0.00122V	10 000 000 000 001	00 000 000 000 001
+0.00000V	+0.00000V	10 000 000 000 000	00 000 000 000 000
−5.00000V	−10.00000V	00 000 000 000 000	10 000 000 000 000

Table 3. DAS1152 Bipolar Input/Output Relationships

Analog Input		Digital Output	
±5V Range	±10V Range	Offset Binary Code	Two's Complement Code
+4.99969V	+9.99939V	111 111 111 111 111	011 111 111 111 111
+2.50000V	+5.0000V	110 000 000 000 000	010 000 000 000 000
+0.0003V	+0.00061V	100 000 000 000 001	000 000 000 000 001
+0.00000V	+0.00000V	100 000 000 000 000	000 000 000 000 000
−5.00000V	−10.00000V	000 000 000 000 000	100 000 000 000 000

Table 4. DAS1153 Bipolar Input/Output Relationships

TRI-STATE DIGITAL OUTPUT

The ADC digital outputs are provided in parallel format to the output tri-state buffers. The output information can be applied to a data bus in either a one-byte or a two-byte format by using the HIGH BYTE ENABLE and LOW BYTE ENABLE terminals. If the tri-state feature is not required, normal digital outputs can be obtained by connecting the enable pins to ground.

POWER SUPPLY AND GROUNDING CONNECTIONS

Although the analog power ground and the digital ground are connected in the DAS1152/DAS1153, care must still be taken to provide proper grounding due to the high accuracy nature of these devices. Though only general guidelines can be given, grounding should be arranged in such a manner as to avoid ground loops and to minimize the coupling of voltage drops (on the high current carrying logic supply ground) to the sensitive analog circuit sections. Analog and digital grounds should remain separated on the PC board and terminated at the respective DAS1152/DAS1153 terminals.

No power supply decoupling is required since, the DAS1152/ DAS1153, contain high quality tantalum capacitors on each of the power supply inputs to ground.

14-Bit & 15-Bit Low Level Data Acquisition Systems

DAS1155/DAS1156



FEATURES

Functionally Complete:
Includes Instrumentation Amplifier, Sample/Hold Amplifier, and Analog to Digital Converter
Differential Nonlinearity: ±0.002% FSR max (DAS1156)
Guaranteed Nonlinearity: ±0.005% FSR (DAS1155)
±0.003% FSR (DAS1156)
High Common Mode Rejection: −80dB (up to 500Hz)
High Feedthrough Rejection: −96dB
Resistor Programmable Gain: 1V/V to 1000V/V
Byte Selectable Tri-State Buffer Outputs
Internal Gain and Offset Potentiometers

APPLICATIONS

Low Level High Accuracy Data Acquisition Systems
Process Control
Nuclear Instrumentation
Automated Test Equipment
Medical Instrumentation

GENERAL DESCRIPTION

The DAS1155/DAS1156 are 14-/15-bit low level data acquisition systems having a minimum throughput rate of 25kHz/20kHz. These data acquisition systems provide high accuracy, high stability, and functional completeness all in a 2″ × 4″ × 0.44″ metal case.

Guaranteed high accuracy system performance such as nonlinearity of ±0.005% FSR (DAS1155)/±0.003% FSR (DAS1156) and differential nonlinearity of ±0.003% FSR (DAS1155)/±0.002% FSR (DAS1156) are provided. Guaranteed stability such as differential nonlinearity T.C. of ±2ppm/°C maximum, offset T.C. of ±(1 + 50/G) µV/°C (RTI) and gain T.C. (RTI) of ±16ppm/°C are also provided by the DAS1155/DAS1156.

Each DAS1155/DAS1156 makes extensive use of both integrated circuit and thin-film components to obtain its excellent performance and small size. Incorporated in these devices are a gain programmable instrumentation amplifier, precision sample/hold amplifier, high accuracy 14-/15-bit analog to digital converter, tri-state output buffers, gain and offset trim potentiometers, and power supply bypass capacitors (as shown in Figure 1).

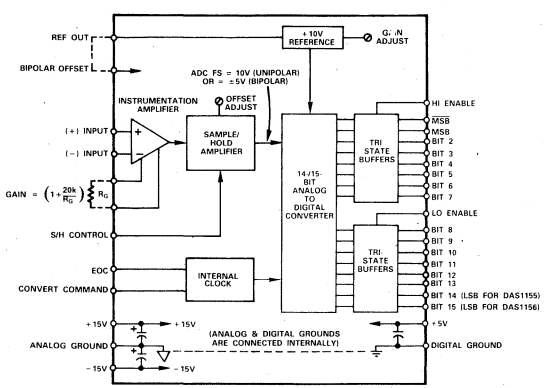


Figure 1. DAS1155/DAS1156 Block Diagram

Unipolar coding is provided for true binary format with bipolar coding displayed in offset binary or two's complement. Tri-state buffers are available for easy interface to bus structured applications.

OPERATION

The DAS1155/DAS1156 are designed, built, and tested to meet system data acquisition requirements. These units can significantly reduce design and debug time by providing, in one package, all of the circuitry necessary for low level data acquisition and microprocessor bus interface.

For operation, the only connections necessary to the DAS1155/DAS1156 are the ±15V and +5V power supplies, analog input signal, trigger pulse, and the HI-ENABLE/LO-ENABLE tri-state controls. Digital output programming is user selectable via external jumper connections.

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ANALOG INPUT SECTION

The analog input section consists of a true differential instrumentation amplifier used to obtain high accuracy measurements in the presence of noise (as shown in Figure 2). It also provides input impedance of (100MΩ) and high common mode rejection of (−80dB). User selectable gain of 1V/V to 1000V/V via an external resistor enables either low level or high level full scale ranges to be applied to the input (+10mV to +10V unipolar, ±5mV to ±5V bipolar) with gain determined by the following formula:

$$\text{GAIN} = 1 + \left(\frac{20k}{R_G}\right)$$

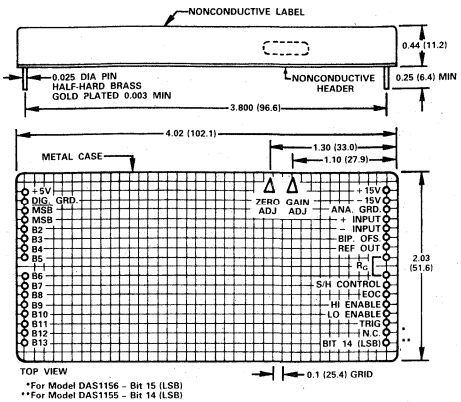
SPECIFICATIONS (typical @ +25°C and rated supplies unless otherwise noted)

MODEL	DAS1155	DAS1156
RESOLUTION	14 Bits	15 Bits
DYNAMIC CHARACTERISTICS		
ADC Conversion Time	35µs max	44µs max
IA Settling Time, (10V Output Swing)		
to 0.003% FSR @ G = 1	15µs max	*
to 0.003% FSR @ G = 10	15µs max	*
to 0.01% FSR @ G = 1000	50µs	*
Throughput Rate @ G = 1, 10	25kHz min	20kHz min
SAMPLE HOLD		
Acquisition Time	4µs max	5µs max
Aperature Delay Time	50ns	*
Aperture Uncertainty Time	1ns	*
Feedthrough Rejection [1]	−96dB	*
Droop Rate	0.05µV/µs	*
ACCURACY		
Differential Nonlinearity (FSR)[2]	±0.003% max	±0.002% max
Integral Nonlinearity (FSR)[3]	±0.005% max	±0.003% max
No Missing Codes	Guaranteed	*
Offset Error	Adjustable to Zero	*
Gain Error	Adjustable to Zero	*
STABILITY		
Offset (RTI) T.C.	$\pm\left(1+\frac{50}{G}\right)$ µV/°C	*
Gain (RTI) T.C.	±16ppm/°C	*
Differential Nonlinearity T.C.	±2ppm/°C max	*
Power Supply Sensitivity	±0.0015% FSR/% V_S	*
ANALOG INPUTS		
Voltage Input Range $\left(\frac{\text{ADC FSR}}{\text{Gain}}\right)$	+10mV to +10V (Unipolar)	*
	±5mV to ±5V (Bipolar)	*
Instrumentation Amplifier		
Gain	Resistor Programmable	*
Gain Range	1 to 1000	*
Gain Equation	$G=1+\left(\frac{20k\Omega}{R_G}\right)$	*
Input Impedance	$10^8\Omega$	*
Bias Current	50nA	*
Offset Current	2nA	*
CMR (up to 500Hz)	−80dB	*
CMV	±10V	*
DIGITAL INPUTS		
ADC Convert Command[4]	1TTL Load, Positive Pulse Negative Edge Triggered	
SHA Control	HOLD = Logic 0 SAMPLE = Logic 1	
Low Enable, High Enable	ENABLE = Logic 0	
DIGITAL OUTPUTS		
Parallel Data Outputs	Tri-State	
Unipolar	Binary	
Bipolar	Offset Binary, 2's Complement	
Output Drive	2TTL Loads	
Status	Logic "1" During Conversion	
Output Drive	2TTL Loads	
INTERNAL REFERENCE VOLTAGE	+10V, ±0.3%	
External Load Current (Rated Performance)	2mA (max)	
Temperature Stability	±8.5ppm/°C (max)	
POWER REQUIREMENTS		
Rated Voltages	±15V ±5%, +5V ±5%	
Operating Voltages[5]	±12V to ±17V, +4.75V to +5.25V	
Supply Current Drain ±15V	±40mA	
+5V	80mA	
TEMPERATURE RANGE		
Specified	0 to +70°C	
Operating	−25°C to +85°C	
Storage	−25°C to +85°C	
Relative Humidity	(Meets MIL-STD-202E, Method 103B)	
SHIELDING	Electrostatic (RFI) 6 sides, Electromagnet (EMI) 5 sides	
SIZE	2" × 4" × 0.44" metal package	

NOTES
[1]Measured in hold mode, input 20V pk-pk @ 10kHz.
[2]FSR means Full Scale Range.
[3]Worst-case summation of IA, S/H and A/D nonlinearity errors.
[4]When connecting the Convert Command the S/H control terminals together, the pulse width must be long enough for the S/H amplifier to acquire the input signal to the required accuracy 4µs (min, DAS1155) 5µs (min, DAS1156).
[5]If a ±12V operating power supply is used, the analog input must be limited to ±7V.
[6]Recommended Power Supply: Analog Devices Model 923.
*Same specifications as for DAS1155.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



INTERCONNECTION AND SHIELDING TECHNIQUES

To preserve the high CMR characteristics of the DAS1155/DAS1156, care must be taken to minimize noise wherever possible. For best performance use twisted shielded cable, for the sensitive input signal, to reduce inductive and capacitive pickup. The cable should be connected as close as possible to the input common mode signal source. Place the gain setting resistor as close as possible to its respective terminal connections to avoid pick-up.

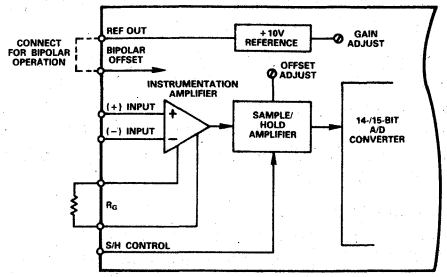


Figure 2. Analog Input Block Diagram

The gain T.C., of the DAS1155/1156, will be directly affected by the resistor used for R_G. Using a high quality metal film resistor is recommended. Bipolar operation is obtained by connecting the REF OUT and the BIPOLAR OFFSET terminals together.

The output of the instrumentation amplifier drives the sample/hold amplifier which has a gain of 1V/V. The sample/hold amplifier holds the input signal at a constant level during the A/D conversion. Acquisition times of 4μs and 5μs maximum are provided respectively by the DAS1155 and DAS1156. Full scale A/D converter input range is programmed for +10V (unipolar) or ±5V (bipolar). Therefore, the instrumentation amplifier gain must be set accordingly to obtain maximum usable resolution.

COMMON MODE REJECTION

CMR is dependent on source impedance imbalance, signal frequency, and amplifier gain. CMR is specified having a ±10V CMV and 1kΩ source imbalance over a frequency range of dc to 500Hz. Figure 3 illustrates the typical CMR vs. source impedance

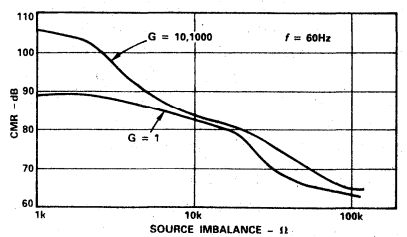


Figure 3. CMR vs Gain and Source Imbalance DAS1155/1156

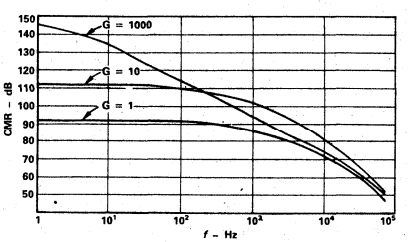


Figure 4. CMR vs Frequency DAS1155/1156

imbalance for the DAS1155/1156. Increasing the input gain of the instrumentation amplifier increases the CMR. At Gain = 1V/V, CMR is maintained greater than 80dB for source impedance imbalance up to 10kΩ. Figure 4 illustrates the CMR vs. gain and frequency.

SETTLING TIME VS. GAIN

Illustrated in Figure 5 is the typical settling time vs. gain of the instrumentation amplifier in the DAS1155/DAS1156. Settling times are specified to 0.003% FSR for gains 1 and 10, and to 0.01% FSR for gain to 1000 having an output step voltage of 10 volts. Settling time to 0.003% FSR for gains greater than 10 are not shown because of the effects of voltage noise at the higher gains.

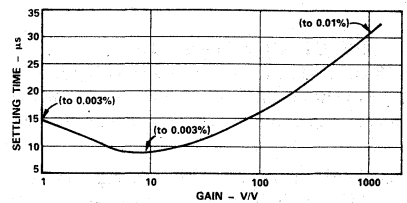
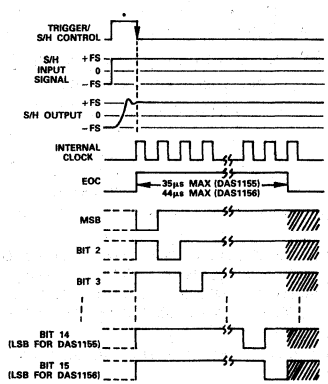


Figure 5. Typical Settling Time vs Gain

TIMING DIAGRAM

The timing diagram for the DAS1155/DAS1156 is illustrated in Figure 6. This figure includes the sample/hold amplifier characteristics and assumes that the instrumentation amplifier is allowed to settle during the previous conversion.



NOTES

1. **Output Data Valid.**
2. **This Diagram assumes that the Instrumentation Amplifier is allowed sufficient time to settle before the Sample/Hold Amplifier is placed in the Sample Mode. Instrumentation Amplifier settling can take place during the A/D Conversion process for the next conversion (see throughput rate).**
3. **The S/H Control and Trigger are tied together, Pulse Width must be 4μs (min)/5μs (min) to allow the S/H Amplifier to acquire the Input Signal.**

Figure 6. DAS1155/DAS1156 Timing Diagram

The TRIGGER input and S/H CONTROL terminal can be tied together requiring only one conversion control signal. When the trigger pulse goes high, it places the sample/hold amplifier in the sample mode allowing it to acquire the present input signal. The trigger pulse must remain high for a minimum of 4μs/5μs, for the DAS1155/DAS1156 respectively, to insure accuracy is attained. At the falling edge of the TRIGGER pulse, the sample/hold amplifier is placed in the hold mode, the A/D conversion

begins, and all internal logic is reset. Once the conversion process is initiated, it cannot be retriggered until after the end of conversion.

With this negative edge of the trigger pulse the MSB is set low with the remaining digital outputs set to logic high state, and the status line is set high and remains high thru the full conversion cycle. During conversion each bit, starting with the MSB, is sequentially switched low at the rising edge of the internal clock. The internal DAC output is then compared to the analog input and the bit decision is made. Each comparison lasts one clock cycle with the complete 14-/15-bit conversion taking 35μs/44μs maximum respectively for the DAS1155/DAS1156.

At this time, the STATUS line goes low signifying that the conversion is complete. For bus applications, the digital output can now be applied to the selected data bus by enabling the tri-state buffers with the HI-ENABLE and LO-ENABLE terminals.

GAIN AND OFFSET ADJUSTMENTS

The DAS1155/DAS1156 each are provided with internal gain and offset adjustment potentiometers. Each potentiometer has ample adjustment range so that gain and offset errors can be trimmed to zero.

Since offset calibration is not affected by changes in gain calibration, it should be performed first. Proper gain and offset calibration require great care and the use of extremely sensitive and accurate reference instruments. The voltage standard used as a signal source must be very stable and be capable of being set to within ±1/10LSB of the desired value at any point within its range.

The analog input values given in Tables 1, 2, 3 and in the following Offset & Gain Calibration Section, are values that should be present at the input to the internal ADC. The value of the analog input will be affected by the gain of the input instrumentation amplifier.(Example: For a full scale input of 0 to +5V, divide the 0 to +10V range input values by 2 and set input gain to 2.

Analog Input 0 to +10V Range		Digital Output Binary Code	
DAS1155	DAS1156	DAS1155	DAS1156
+9.99939V	+9.99969V	11 111 111 111 111	111 111 111 111 111
+5.00000V	+5.00000V	10 000 000 000 000	100 000 000 000 000
+1.25000V	+1.25000V	00 100 000 000 000	001 000 000 000 000
+0.0006V	+0.0003V	00 000 000 000 001	000 000 000 000 001
+0.0000V	+0.0000V	00 000 000 000 000	000 000 000 000 000

Table 1. Nominal Unipolar Input/Output Relationships

Analog Input ±5V Range	Digital Output Offset Binary Code	Two's Complement Code
+4.99939V	11 111 111 111 111	01 111 111 111 111
+2.50000V	11 000 000 000 000	01 000 000 000 000
+0.00061V	10 000 000 000 001	00 000 000 000 001
+0.00000V	10 000 000 000 000	00 000 000 000 000
−5.00000V	00 000 000 000 000	10 000 000 000 000

Table 2. DAS1155 Bipolar Input/Output Relationships

Analog Input ±5V Range	Digital Output Offset Binary Code	Two's Complement Code
+4.99969V	111 111 111 111 111	011 111 111 111 111
+2.50000V	110 000 000 000 000	010 000 000 000 000
+0.00030V	100 000 000 000 001	000 000 000 000 001
+0.00000V	100 000 000 000 000	000 000 000 000 000
−5.00000V	000 000 000 000 000	100 000 000 000 000

Table 3. DAS1156 Bipolar Input/Output Relationships

OFFSET CALIBRATION

For 0 to +10V unipolar range set the input voltage precisely to +305μV for the DAS1155 and +153μV for the DAS1156. Then adjust the zero potentiometer until the converter is just on the verge of switching from 00-----00 to 00-----01.

For the ±5V bipolar range set the input voltage precisely to +305μV for the DAS1155 and +153μV for the DAS1156. Adjust the zero potentiometer until the offset binary coded units are just on the verge of switching from 00-----00 to 00-----01 and the two's complement coded units are just on the verge of switching from 10-----00 to 10-----01.

GAIN CALIBRATION

Set the input voltage precisely to +9.99909 (DAS1155)/+9.99954V (DAS1156) for the 0 to +10V units, or +4.99909V (DAS1155)/+4.99954V (DAS1156) for ±5V units. Note that these values are 1 1/2LSB less than nominal full scale. Adjust the gain potentiometer until binary and offset binary coded units are just on the verge of switching from 11-----10 to 11-----11 and two's complement coded units are just on the verge of switching from 011-----10 to 011-----11.

THROUGHPUT RATE

Throughput rates for the DAS1155/DAS1156 can be increased by the use of the OVERLAP MODE, i.e. updating the input while the ADC is making a conversion.

The guaranteed throughput rates are 25kHz @ G = 1, 20kHz @ G = 1000 for the DAS1155 and 20kHz @ G = 1 and 1000 for the DAS1156. When the IA settling time is less than or equal to the sum of SHA acquisition time and ADC conversion time, 39μs, the DAS throughput rate equals 1/39μs or 25.6kHz. When IA settling time is greater than 39μs (see Figure 5), the DAS throughput rate becomes dependent upon the IA settling time and equals its reciprocal.

DAS1155/DAS1156 INPUT/OUTPUT RELATIONSHIPS

The DAS1155/DAS1156 produces a true binary coded output when configured as a unipolar device. Configured as a bipolar device, it can produce either offset binary or two's complement output codes. The most significant bit (MSB) is used to obtain the binary and offset binary code while the ($\overline{\text{MSB}}$) is used to obtain the two's complement code. Table 1 shows the unipolar analog input/digital output DAS1155/DAS1156 relationships. Tables 2 and 3 show the DAS1155/DAS1156 bipolar analog input/digital output relationships respectively.

TRI-STATE DIGITAL OUTPUT

The digital outputs are provided in parallel format to the output tri-state buffers. The output information can be applied to a data buss in either a one-byte or a two-byte format by using the HI-ENABLE and LO-ENABLE terminals. If the tri-state feature is not required, normal digital outputs can be obtained by connecting the enable pins to ground.

POWER SUPPLY AND GROUNDING CONNECTIONS

Although the analog power ground and the digital ground are connected in the DAS1155/DAS1156, care must still be taken to provide proper grounding due to the high accuracy nature of the devices. Though only general guidelines can be given, grounding should be arranged in such a manner as to avoid ground loops and to minimize the coupling of voltage drops (on the high current carrying logic supply ground) to the sensitive analog circuit sections. Analog and digital grounds should remain separated on the PC board and terminated at the respective DAS1155/DAS1156 terminals.

No power supply decoupling is required since, both the DAS1155 and DAS1156, contain high quality tantalum capacitors on each of the power supply inputs to ground.

Digital Panel Instruments

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•New product since the *1980 Data-Acquisition Components and Subsystems Catalog.*

16

Selection Guide
Digital Panel Instruments

For the purpose of selection, the instruments in this section are divided into three classes, each having its own Selection Guide:

1. 3- to 4 3/4-digit panel meters for general applications, powered by dc voltage furnished by the user's instrumentation-system +5V logic supply
2. 3- to 4 3/4-digit panel meters for general applications, powered by ac line voltage, and including multi-channel scanning and true-rms types
3. Single- and scanning multi-channel digital temperature meters for measurements with thermocouples, RTDs, thermistors, and AD590 semiconductor temperature sensors

The Selection Guides permit all the devices in each class to be compared in terms of their salient features, to narrow the field of choice to one or two devices, for which page locations are given. The data sheets in this Volume have technical

		LOGIC (+5V) POWERED DIGITAL PANEL METERS						
		AD2026-1	AD2006D	AD2010	AD2021	AD2004	AD2027	AD2028
Digits; F.S. Range	3; -99 to +999mV	•						
	3½; ±199.9mV			•	•			
	±1.999V		•		•			
	±19.99V				•			
	4½; ±1.9999V					•	•	
	±19.999V						•	
	4¾; ±3.9999V							•
	±39.999V							•
Input Type	Ltd. Differential	•		•	•		•	•
	Differential		•					
	Floating					•		
Data Outputs		N/A						
	Character Serial				•		•	•
	Parallel BCD		•				•	•
	Parallel BCD Latched			•		•		
Display Type	LED	•		•	•	•	•	•
	Beckman		•					
Display Size		0.5/13	0.55/14	0.27/7	0.5/13	0.27/7	0.43/11	0.43/11
Case Depth[1] in/mm		0.65/17	4.08/104	0.84/21	1.31/33	2.52/64	4.08/104	4.08/104
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[1] All logic powered DPMs use industry standard case with 3.175" X 1.810" (80.65 X 45.97mm) cutout. All ac-powered DPMs except AD2006 use industry standard case with 3.930" X 1.682" (99.82 X 42.72mm) cutout. AD2006 uses same case as logic powered DPMS.

descriptions, specifications, and in many cases, applications information. Complete data sheets for most of these instruments, with further information on application and use of the products, are available upon request. General information on digital panel instruments can be found in the pages that follow the Selection Guides.

For temperature instrumentation, there are a number of other products dedicated to temperature measurement, included in this Databook, that may be of interest. They are to be found in these sections: Transducers & Signal Conditioners, μMAC-4000 Intelligent Measurement-and-Control Subsystems, and MACSYM. Power supplies for excitation of system-powered panel instruments may be found in the Power Supply section.

Finally, in the Synchro & Resolver Conversion section, there are the benchtop API1620 and API1718 Angle Position Indicators, which accept synchro or resolver input, convert to digital, and provide a 5-digit numerical LED display of the angle, and a 5-decade BCD or 16-bit binary data output.

		AC-POWERED DIGITAL PANEL METERS							
		AD2026-2	AD2006	AD2009	AD2016	AD2033[1]	AD2024	AD2025	AD2037
6-Channel Scanning									●
Digits; F.S. Range	3; -99 to +999mV	●							
	3½; ±199.9mV			●	●	●[1]			●
	±1.999V		●	●	●	●[1]			●
	±19.99V			●	●	●[1]			
	199.9V					●[1]			
	600V					●[1]			
	4½; ±1.9999V						●		
	±19.999V						●		
	4¾; ±3.9999V							●	
	±39.999V							●	
Input Type	Single Ended			●					
	Ltd. Differential				●		●	●	
	Differential		●						●
	Floating	●				●			●
	True RMS					●			
Data Outputs		N/A							
	Character Serial				●	●	●	●	
	Parallel BCD		●	●	●	●	●	●	
	Parallel BCD Latched								●
Display Type	LED	●			●	●	●	●	●
	Beckman		●	●					
Display Size		0.5/13	0.55/14	0.55/14	0.5/13	0.5/13	0.43/11	0.43/11	0.5/13
Case Depth[2] in/mm		2.44/63	4.08/104	4.15/105	4.15/112	4.48/114	4.48/114	4.48/114	5.80/147
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[1] Full scale inputs when reading out in dB are 500mV, 5V, 50V, 500V and 625V rms.
[2] All logic powered DPMs use industry standard case with 3.175" X 1.810" (80.65 X 45.97mm) cutout. All ac-powered DPMs except AD2006 use industry standard case with 3.930" X 1.682" (99.82 X 42.72mm) cutout. AD2006 uses same case as logic powered DPMs.

		DIGITAL TEMPERATURE METERS					
		AD2036	AD2037	AD2038	AD2040	AD2050	AD2051
Input	Number of Channels: 1				●	●	●
	Number of Channels: 6	●	●	●			
Sensor (Determines Temperature Range)	Thermocouple Type: Switch Selected						●
	Thermocouple Type: User Specified	●				●	
	Thermocouple Type: J, K, T	●				●	●
	Thermocouple Type: E, R, S					●	●
	AD590 (−55°C to +150°C)			●	●		
	RTD		●				
	Thermistor		●				
Features	Self-Calibration					●	●
	Cold-Junction Compensation	●				●	●
	Linearization	●				●	●
	Isolation	●	●	●		●[1]	●[1]
Readout	Digits: 3+, 2−				●		
	Digits: 3½	●	●	●		●	●
	LED Display Height: 0.5″, 13mm	●	●	●	●		
	LED Display Height: 0.56″, 14.3mm					●	●
Digital Data Output	Isolated Parallel BCD	●	●	●			
	7-Bit Character-Serial ASCII					●	●
Analog Output	Voltage	●	●	●		●	●
	4-to-20mA Current Loop					●	●
Power Supply	AC Line	●	●	●		●	●
	DC +7V to +15V					●	●
	DC +5V				●		
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[1] AC line-operated versions.

UNDERSTANDING DPMS

Introduction

A DPM is basically an analog to digital converter with a visual readout. The DPM samples the input voltage periodically, converts that voltage to digital outputs, and displays the corresponding reading visually. A digital panel meter, then, consists of four basic functional sections: the input section, including signal conditioning and analog to digital conversion circuitry; the display; the data outputs; and the power supply.

Processing The Input Signal

The primary function of the input section is to convert an analog voltage input into a digital signal for display. Besides this basic function, the input section also buffers the input to provide a high input impedance, prevent circuit damage in overvoltage conditions, reject both normal mode and common mode noise on the input signal, compensate for large variations in operating temperature, and sometimes even measure the ratio of two separate input voltages.

The analog to digital conversion scheme used on most DPMs is the dual-slope type, due to its inherent stability and normal mode noise rejection. The dual slope converter can also be used to measure the ratio of two input voltages, in some DPM designs. Lower-resolution DPMs sometimes use staircase or single slope converters, which require RC filtering of the input signal for normal mode noise rejection.

The input of the DPM may be single-ended, differential or floating. Single-ended inputs measure the input voltage with respect to input common and may require some care in application to avoid ground loop problems. To prevent ground loops, some of Analog Devices' DPMs use a "limited differential input", where a resistor separates analog and digital grounds, allowing up to 200mV of common mode voltage and providing up to 60dB of common-mode rejection.

True differential input DPMs accommodate common mode voltages of up to ±5V, adequate for most bridge transducer type applications. For very high common mode voltages, the opto-isolation technique, used in several Analog Devices DPMs, allows common mode voltages of up to ±300V and provides 100 to 120dB of common mode rejection, even when BCD data outputs are being used. Any ac powered DPM can be floated on the power supply transformer to provide isolation and CMR, similarly to the opto-isolated DPM, if no BCD outputs or control signals are being used (i.e., in readout-only operation). Further information on DPM input configurations can be found in the Applications section.

Although most DPMs measure dc input voltages only, and a few measure the rectified average value of ac inputs, the AD2033 measures either the true-rms value of ac+dc signals or the dB value of the ac+dc inputs. The AD2033 uses an implicit computing technique to make accurate and rapid measurements of ac inputs regardless of waveform. Five separate, calibrated inputs are provided for full scale ranges of 200mV to 600V rms. Even with digital and control lines connected, the floating opto-isolated analog input withstands high common mode voltages, such as those encountered when making rms *current* measurements.

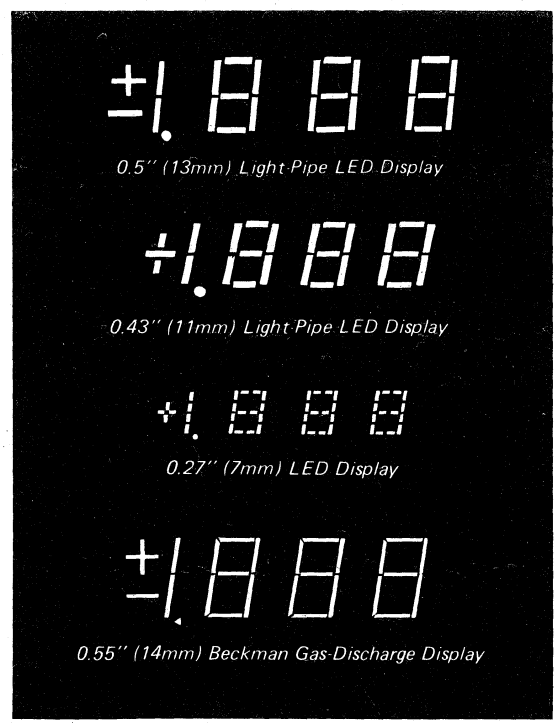
Displaying the Data

Once the input signal is digitized, it is decoded and displayed on a digital readout. Numerous types of displays are available today, but Analog Devices' DPMs use large LED (light emitting diode) displays on all of the latest models. Seven-segment LED displays are large as 0.56 (14.3mm) offer the ultimate in ruggedness, reliability and aesthetic appeal, and challenge Beckman gas discharge displays for size.

Beckman displays and smaller 0.27" (6mm) solid state LEDs are also used by Analog Devices. The large shaped characters of the Beckman display easily read at up to 30 feet (9 meters) away. The neon orange digits can be filtered to provide either an amber or a red display. The smaller LEDs, packaged with counting and decoding logic circuitry, permit the extremely small packaging of the AD2010 and the AD2004. Numitron tube displays, still available in some older designs, offer easy viewing in direct sunlight and can be filtered to provide red, green or amber readouts.

Producing Digital Outputs

Since the visual display of a DPM must be in a decimal format, the counters used in DPM conversion circuitry are always binary-coded decimal (BCD) counters. The data-output format



depends on the circuit design of the meter: most designs using TTL integrated circuits have parallel BCD data outputs, with all BCD bits available simultaneously. Parallel data is easiest to interface to, since most data peripherals, such as printers and comparators, require parallel data. Parallel data can be latched, and therefore valid, except for the period of several microseconds after each conversion, when it is updated, or unlatched, where the data is valid only between conversions. In either case, a STATUS or DATA READY signal is available to indicate when the data outputs are valid.

DPMs using MOS-LSI (metal-oxide semiconductor, large scale integrated circuits) usually have character serial outputs, where each BCD digit is gated onto a single set of parallel output lines in sequence. This technique is used to reduce the number of pins used on the LSI chip and to simplify data interfacing to the display. Although some data peripherals, such as microprocessors, require character-serial data inputs, for many applications it is necessary to use latches or shift registers to convert the data into a parallel format for interfacing. Most DPMs using LSI have an extra cost option available that provides parallel data outputs.

Digital data outputs from DPMs are generally compatible with DTL or TTL logic systems, but some of the newer DPMs using LSI are only compatible with CMOS logic. The parallel output option with these LSI DPM designs, however, is generally TTL compatible for ease in interfacing.

Powering the DPM

Logic power or line power? The +5V dc logic powered DPM can share the power supply designed into most instruments and systems for powering standard logic circuits. When the DPM is operated from the +5V power supply, no ac transformer is required, and the size and weight of the DPM are greatly reduced and internal temperature rise is minimized. This reduction in size, weight and power has allowed DPMs to be used in instruments that could not accommodate bulky ac line-powered DPMs.

The logic-powered DPM has a greater isolation from line variations, noise and transients, since it is operated on regulated power and no ac power lines need to be routed to the front panel of the instrument or system. Logic powered DPMs are safer also, since no high voltages are required, making operational testing safer and UL or CSA approval simpler.

The logic power concept was originally based on the widespread usage of TTL logic circuits. However, MOS (metallic-oxide semiconductor) integrated circuits that use the same power supplies but require less power have greatly increased the benefits of the logic powered DPM. Not only is MOS logic used in the DPMs themselves, to reduce power consumption and size, but its widespread usage in external circuitry to provide instrument control and signal conditioning have made the logic powered DPM concept even more valid today than when it was conceived. Using MOS circuits and logic powered DPMs, today's instruments are becoming smaller; and their lower power consumption makes portability, even with battery power, highly feasible for many designs.

If sufficient logic power cannot be made available in the instrument or system design, or if compatibility with current designs using ac powered DPMs is desired, the line powered DPM will be a better choice. And, in those cases where line powered DPMs make available external power supplies, the DPM may be used to power the entire measurement system.

Analog Devices offers a full line of both logic powered and line powered DPMs, with choices of display types, digits of resolution and grades of performance to allow the user to select the proper DPM for a wide range of applications.

SELECTING DPMs

Which Meter For The Application – Digital Or Analog?

The decision whether to use an analog or digital meter is generally based on three considerations: performance, cost and aesthetics. The DPM offers tremendously greater performance in readability, accuracy, and the availability of special features.

Since the digital display is completely free of ambiguity or interpolation errors, it is an ideal choice for instruments that must be accurately read by relatively unskilled personnel, for example, medical instruments used in operating rooms or process control instruments used in factories. And, the large, bright displays used on DPMs allow the displays to be read from great distances in almost any lighting conditions.

DPMs are basically analog-to-digital converters with displays, and the DPM offers data outputs that can be interfaced with printers, teletypewriters or computers for data logging or processing, or to digital comparators for making go/no go decisions.

Analog meters are principally useful for those applications in which a skilled operator can derive much useful information from the acceleration and fluctuations of a moving element. For example, anticipating adjustment and control often hinges on estimating rate and acceleration, making an analog display mandatory.

The trend in today's instrumentation is toward digital readouts. This is not just because of the performance advantages of DPMs, but because of the superior appearance and customer appeal of digital readouts.

Now DPMs are easier to justify than ever before. For example, the Analog Devices AD2026 became the first real alternative to the measurement grade analog panel meter.

The "Make or Buy" Decision

Several integrated circuit manufacturers now offer DPM LSI chips. Often it is implied that with the DPM chip(s) and a few external components, one can build his own DPM. Although this may seem attractive to some users, the manufacture of a complete DPM is not as easy as it may sound.

Considerable circuit design experience is required to design a DPM of adequate performance using a chip or chip set. Then,

printed circuit boards must be laid out, packaging hardware must be designed, and production line facilities, test equipment and burn-in racks must be designed and built. Parts must be purchased, tested and stocked for each DPM design needed.

Analog Devices, of course, goes through all these procedures and many more, for each and every DPM model we sell. We use our volume buying power to cut parts costs, and our experience in building DPMs to streamline the DPM manufacturing process while still maintaining high standards of DPM quality. And, being a large company with a large export market, we can provide our customers with worldwide sales and service backup.

For most companies that use DPMs, buying a complete DPM from an established vendor turns out to be more cost effective and less troublesome than building their own. By purchasing DPMs, one can obtain quality, reliability, service and low cost without investment of resources, risk and the problems of acquiring DPM design competence.

Understanding Performance Specifications

Currently, there are no industry standards on DPM specifications, and comparing specifications of DPM's from different manufacturers may require some analysis. A section of DPM specification definitions has been included, but an elaboration on several of these is included below to help in understanding fully how specifications relate to performance requirements.

Resolution, Accuracy, and Stability—these three specs are very important in the selection of a DPM. Although more digits may mean more resolution, the digits themselves are useless unless the accuracy is sufficient for the digits to have real meaning. Therefore, accuracy and resolution should be comparable.

Besides temperature variations, there are three components of DPM inaccuracy: *zero offset error, gain error,* and *quantization error.* In any device using a counter and clock to determine a digital output, there is always a potential ±1 count error in the output. This is caused by the timing of the input gate of the counter; when the gate closes asynchronously with the clock, a clock pulse that occurs just as the gate closes may or may not be counted, hence the fixed ±1 digit inaccuracy.

Zero level offsets in the analog circuitry cause errors specified as a percentage of full scale reading. These errors can be corrected by a zero calibration potentiometer requiring periodic resetting, or by internal calibration circuits that set the zero level automatically between each reading, assuring no zero level contribution to the error.

Gain variations occur as a function of signal level in the analog circuitry and produce errors which are specified as a percentage of the reading. These are the hardest errors to design out of a DPM circuit, but they can be minimized by component specification and selection. A range potentiometer is used for periodic adjustment of the gain. Gain errors may also be calibrated out in "smart" instruments having an automatic internal calibration facility (e.g. AD2050).

Since all the electronic components used in the design of a DPM have some temperature dependence, one can expect the accuracy of the DPM to be affected by changes in operating temperature. If automatic zero correction circuitry is not used, the zero level may drift with temperature. Variations in the reference voltage circuitry and its associated switches will cause changes in the gain of the DPM, but careful selection and matching of components can minimize this error.

To illustrate these specifications, consider a 3½ digit DPM (1999 counts full scale). The resolution of the unit is the value of one digit, 1 part in 2000 or 0.05% of full scale. If the accuracy is comparable to the resolution (exclusive of digital indecision), the DPM should have a maximum error of ±0.05% ±1 digit.

Temperature coefficient specifications for a DPM should be very good to maintain the accuracy. A tempco of only 50ppm/°C (0.005%/°C) will produce an additional error of ±0.05% over a range of only ±10°C.

Since each manufacturer tends to use a different method of specifying accuracy and temperature coefficients, specifications must be expressed in common terms to be comparable. For example, one may find specifications for 3½ digit DPMs in the formats shown below ("R" = "of reading"):

Unit 1: max error: ±0.05% R ±1 digit, tempco: ±50ppm(R)/°C

Unit 2: max error: ±0.02% R ±0.03% F.S. ±1 digit, tempco: ±0.004%R ±0.001% F.S./°C

Unit 3: max error: ±0.05% R ±0.05% F.S. ±1 digit, for temperature +15°C to +35°C

To compare the three units, one must establish a common ground: full scale reading, temp range +15°C to +35°C (±10°C). The specification then becomes:

Unit 1: ±0.05% F.S. ±1 digit ±(50ppm(F.S.)/°C x ±10°C)
= ±0.05% F.S. ±1 digit ±0.05% F.S.
= 0.1% F.S. ±1 digit

Unit 2: ±(0.02% F.S. ±0.03% F.S.) ±1 digit (0.004% F.S. ±0.001% F.S.)/°C x ±10°C
= 0.05% F.S. ±1 digit ±0.05% F.S.
= 0.1% F.S. ±1 digit

Unit 3: ±0.05% F.S. ±0.05% F.S. ±1 digit
= 0.1% F.S. ±1 digit

Even though all units are specified differently, they have equivalent performance.

Selecting A DPM

To select the proper DPM for an application, one must thoroughly review the design requirements. This review should include a characterization of the input signal: dc, ac or ac+dc, full scale range, unipolar or bipolar, whether any common mode voltage is present, or if noise pickup may be a problem. What accuracy and resolution are required? Is other than LED display required? Is viewing at large distances or

color coding the displays necessary? Will the DPM be powered by +5V dc or ac line? Are data outputs necessary for data logging or feedback control? Are special features, like ratiometric operation, or the availability of power supply outputs from ac powered DPMs needed?

Once the application is fully characterized, a DPM must be selected with the proper specifications. The following checklist can be used as a guide to help in the selection process:

Selection Checklist

☑ What inputs are to be measured?

- DC, AC or AC+DC
- Unipolar, or bipolar
- Full scale range
- Common mode voltage

☑ Performance

- Resolution: 2½, 3, 3½, 4, 4½, 4¾ digits
- Accuracy
- Temperature operating range and temperature coefficients
- Noise rejection

☑ Display

- LED
- Gas discharge (Beckman)
- Incandescent (Numitron)

☑ Power supply input

- AC line
- +5VDC

☑ Interface signals

- Trigger/Hold – conversion speed
- Data outputs – parallel BCD, character serial or pulse train
- Logic compatibility

☑ Special features

- Ratiometric operation
- Power supply outputs from AC powered DPMs
- Display blanking controls

☑ Physical requirements

- Size – panel cutout and depth
- Mounting requirements

☑ Quality control and reliability

- Burn-in before shipment
- Warranty

☑ Environmental specifications

- Temperature range, operating and storage
- Special requirements – humidity, vibration, etc.

DEFINITIONS – TERMS & SPECIFICATIONS

Accuracy (absolute): DPMs are calibrated with respect to a reference voltage which is in turn calibrated to a recognized voltage standard. The absolute accuracy error of the DPM is the tolerance of the full-scale set point referred to the absolute voltage standard.

Accuracy (relative): Relative accuracy error is the difference between the nominal and actual ratios to full scale of the digital output corresponding to a given analog input. See also: linearity.

Automatic Zero: To achieve zero stability, a time interval during each conversion is provided to allow the circuitry to compensate for drift errors, thereby, providing virtually no zero drift error.

Bias Current: The current required from the source at zero signal input by the input circuit of the DPM. Bias current is normally specified at typical and maximum values. Analog Devices' DPMs using transistor input circuitry are bias current sinks.

Binary Coded Decimal (BCD): Data coding where each decimal digit is represented by a group of 4 binary coded digits (called "quads"). Each quad has bits corresponding to 8, 4, 2, 1 and 10 permissible levels with weights 0-9. BCD is normally used where a decimal display is needed.

Bipolar: A bipolar DPM measures inputs which may be of either positive or negative polarity and automatically displays the polarity as well as the magnitude of the input voltage on the readout.

Character Serial BCD: Multiplexed BCD data outputs, where each digit is gated sequentially onto four common output lines.

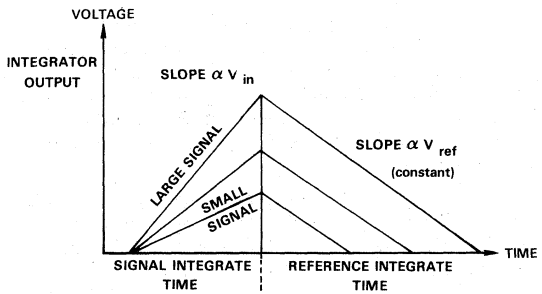
Common-Mode Rejection: A differential-input DPM will reject any input signals present at both input terminals simultaneously if they are within the common mode voltage range. Common mode rejection is expressed as a ratio and usually given in dB. (CMR = 20 log CMRR). 120dB of common-mode rejection (CMRR = 10^6) means that a 10V common-mode voltage is processed as though it were an additive-differential input signal of 10μV magnitude.

Common Mode Voltage: A voltage that appears in common at both input terminals of a device, with respect to its ground.

Conversion Rate: The frequency at which readings may be processed by the DPM. Specifications are typically given for internally clocked rates and maximum permissible externally-triggered rates.

Conversion Time: The maximum time required for a DPM to complete a reading cycle, specified for the full scale reading.

Dual-Slope Conversion: An integrating A/D conversion technique in which the unknown signal is converted to a proportional time interval, which is then measured digitally. This is done by integrating the unknown for a predetermined time.

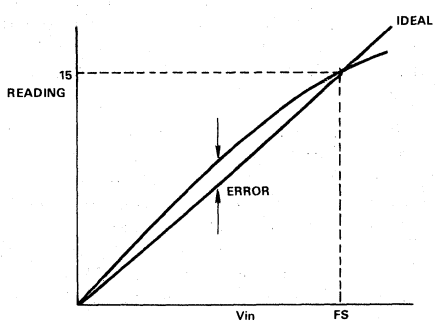


Dual Slope Conversion

Then a reference input is switched to the integrator, and integrates "down" from the level determined by the unknown, until a "zero" level is reached. The time for the second integration process is proportional to the average of the unknown signal level over the predetermined integrating period.

Input Impedance: The complex ratio of signal voltage to signal current at the input terminals. For dc measuring DPMs, the input is measured at dc. For ac measuring DPMs, it is expressed as a dc resistance shunted by a specified capacitance.

Linearity: The conventional definition for nonlinearity of a DPM is the deviation from a "best" straight line which has been fitted to a calibration curve. Analog Devices defines nonlinearity as the deviation from a straight line drawn between the zero and full scale end points. Not only is this an easier method for customer calibration, it is also a more conservative method of specifying nonlinearity.



Linearity

Normal Mode Rejection: Filtering or integrating the input signal improves noise rejection of undesired signals present at the analog *high* input. Normal mode rejection is expressed as the ratio of the actual value of the undersired signal to its measured value over a specified frequency range. (NMR (dB) = 20 log NMRR, e.g. NMR = 40dB means an attenuation of 100:1).

Overload: An input voltage exceeding the full scale range of the DPM produces an overload condition. An overload condition is usually indicated by conspicuous manipulation of the display such as all dashes, flashing zeros, etc. On a 3½ digit DPM with a range of 199.9mV, a ⩾200mV signal will produce an overload condition.

Overrange: As input signal that exceeds all-nines on a DPM, but is less than an overload. On a 3½ digit DPM with a full scale range of 199.9mV, the all-nines range is 0–99.9mV, and signals from 100–199.9mV are said to fall in the 100% overrange region. Some DPMs have higher overrange capability. A 3¾ digit DPM has a full scale range of 3.999 or 300% overrange.

Overvoltage Protection: The input section of the DPM must provide protection from large overloads. Specifications are given for sustained dc voltages that can be tolerated.

Parallel BCD: A data output format where all digital outputs are present simultaneously.

Range (Temperature Operating): The range of temperatures over which the DPM will meet or exceed its performance specifications.

Range (Full Scale): The range of input signals that can be measured by a DPM before reaching an overload condition. A 3½ digit DPM's full-scale range consists of three digits (all-nines range) and 100 percent overrange capability.

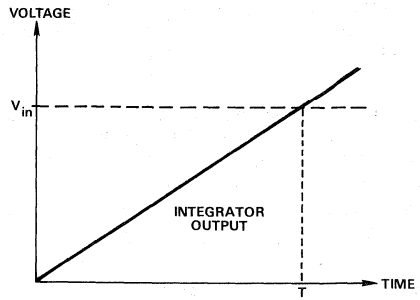
Ratiometric: Dual Slope DPMs compare voltage inputs to a stable internal reference voltage. In some systems, the voltage being measured is a function of another voltage, and accurate measurements should be made as the ratio of the two voltages. Some DPMs provide inputs for external reference voltages for ratiometric measurements.

Resolution: The smallest voltage increment that can be measured by a DPM. It is a function of the full scale range and number of digits of a DPM. For example, if a 3½ digit DPM has a resolution of 1 part in 2000 (0.05%) over a full scale range of 199.9mV, the DPM can resolve 0.1mV.

16

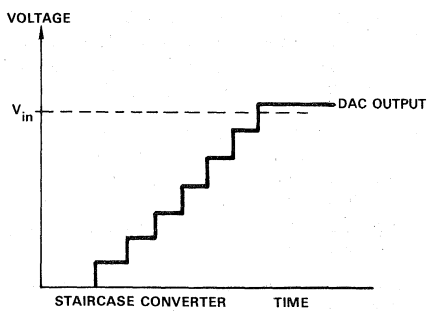
Digits	Counts (F.S.)	Resolution (% F.S.)
2½	199	0.5%
3	999	0.1%
3½	1999	0.05%
3¾	3999	0.025%
4	9999	0.01%
4½	19999	0.005%
4¾	39999	0.0025%

Single Slope Conversion: In the single slope converter, a reference voltage is integrated until the output of the integrator is equal to the input voltage. The time period required for the integrator to go from zero to the level of the input is proportional to the magnitude of the input voltage and is measured by an internal clock.



Single Slope Converter

Staircase Conversion: A simple analog-to-digital conversion technique in which a clock and counter drives a digital-to-analog converter which produces an output voltage waveform resembling a staircase. A comparator stops the counter when the voltage exceeds the input voltage; the count achieved by the counter is the digitized output.



Staircase Converter

Temperature Coefficient: The additive error term (ppm/°C or % Reading/°C) caused by effects of variations in operating temperature on the electronic characteristics of the DPM.

Unipolar Input DPM: A DPM designed to measure input voltages of only one polarity.

APPLYING DPMs

The unique features of the DPM has lead to its widespread usage in many types of test and measurement instrumentation or systems. In fact, the popularity of the DPM as an instrument readout has greatly accelerated the trend to digital readouts in many other applications. Few instrument designs are now initiated without plans for a digital readout.

Some of the applications for DPMs include:

Medical Instruments: Doctors and nurses need precise information – FAST! They rely on digital readouts of blood pressure, heart rate, pulmonary functions, and blood analyses to make life or death decisions.

Analytical and Scientific Instrumentation: Scientists or researchers need accurate information in their experiments, and along with the widespread usage of computers, they interface their equipment for direct data acquisition. They measure pH, temperature, light intensity and virtually any other physical parameter, and the DPM readout gives their instruments the accuracy and interfacibility they need.

Process Control: To measure the thickness of a plastic film, the temperature of metals during processing or even the effluents in their waste water, a DPM provides the accuracy needed for cost conscious production engineers.

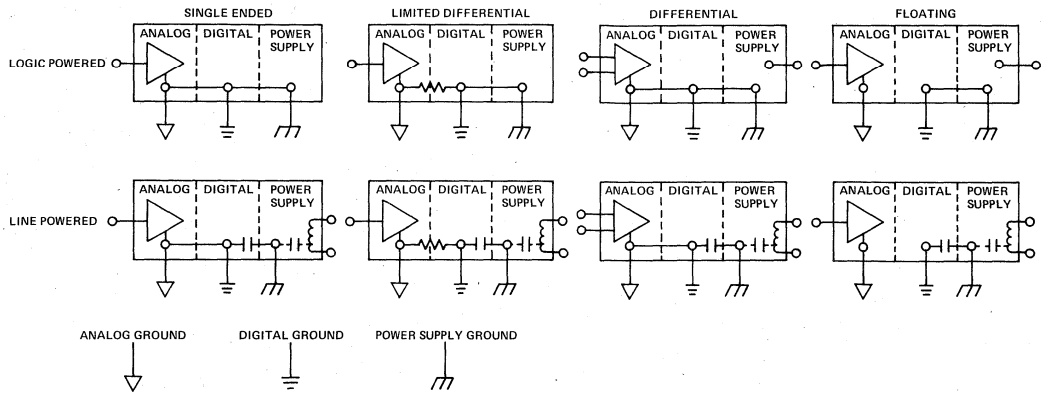
In-House Test Equipment: In order to test electrical and electronic components, instruments or systems, companies need accurate tests in a minimum of time. The DPM provides fast, accurate measurements, and the BCD outputs can be interfaced to digital comparators to provide GO/NO GO or GOOD/BAD decisions without relying on operator decision.

DPM Input Types And Their Applications

The four different input configurations used on DPMs (single-ended, limited differential, differential, and floating) are made available to solve various applications problems. In OEM applications where the DPM is a dedicated readout for an instrument or system, a single-ended DPM is usually desired for its low cost. But single-ended DPMs require care in application to prevent ground loops from interfering with measurements. The "limited differential" input pioneered by Analog Devices, however, uses a single resistor to isolate analog and digital (and, in logic powered DPMs, the power supply) grounds to effectively eliminate ground loops. This limited differential input allows up to approximately 200 millivolts of common mode voltage and 60dB of common mode rejection without imposing the cost penalties of a true differential or floating input. Thus the majority of DPM applications require only a single-ended or limited differential input DPM.

But if the DPM is measuring the output of a bridge transducer, higher common mode voltages must be accommodated, and differential input DPMs which allow a CMV up to ±5V are usually necessary. Where extremely high common mode voltages are required, such as current measurements, a floating (usually opto-isolated) input DPM can provide for up to ±300V CMV. Either the differential or floating input DPM will also provide greater common mode noise rejection, if necessary.

If digital control signals and BCD data outputs are not needed, any ac line powered DPM can be floated on the power supply transformer to provide high CMV and CMR. But care must be exercised when applied in this fashion at high CMV, since all connections may be floating at dangerously high voltages. All line powered DPMs have a connection for "earth ground" which may be connected to a transformer shield or guard track on the printed circuit board, but this earth ground is usually capacitively coupled to the digital ground for noise rejection. Always insure that the earth ground is not directly connected to digital ground when "floating" a line powered DPM in this manner.



Grounding Configurations of DPMs

The diagrams above indicate the internal grounding connections typically used in DPMs with these various types of input configurations. In DPM circuit applications, they can be used to help understand and trace input connections during design and troubleshooting.

ANALOG DEVICES AS DPI SUPPLIER

In 1972, Analog Devices entered the Digital Panel Meter market with a totally new concept: a DPM that operates from the +5V dc power supply commonly used for logic circuitry. Since that time, the user and application benefits of the "logic powered" DPM have been well proven and widely copied. In addition, input circuits have been devised that sense and correct offset drifts between each reading, providing more accurate DPM performance and allowing longer periods between calibration. The "limited differential" input used in some ADI DPMs provides protection from ground loop problems in single ended DPMs at a lower cost than true differential inputs. The AD2033 combines a DPM with input conditioning circuitry to measure the true rms value of any input signal – ac, dc or ac+dc. Introducing the third generation of DPMs, the AD2026 was specifically designed to provide a digital alternative to analog panel meters. Both analog and digital circuitry are implemented on a single I^2L LSI chip.

The products here comprise a wide choice of models with features to fit most every application. One can choose logic power or line power, 3, 3½, 4½ or 4¾ digits of resolution, with LED or Beckman displays. A wide variety of input configurations, data outputs and special features (such as ratiometric operation or the ability to measure true rms values) simplify the application of an Analog Devices' DPM in any application.

In addition to the complete line of traditional DPMs, Analog Devices offers a line of multi-channel digital scanning instruments, including the AD2036 and AD2038 6-channel digital scanning thermometers and the AD2037 6-channel digital scanning voltmeter. They are versatile building blocks for a broad range of data acquisition, data logging, or control applications.

Complementing these products are the AD2040, the industry's lowest cost temperature indicator, and the AD2050 smart temperature indicator for thermocouples.

INDUSTRY STANDARD CASE DESIGNS

Many manufacturers have chosen to use the Analog Devices logic powered case size for their +5V logic powered DPMs, and Analog Devices offers ac line powered DPMs in a case size compatible with the majority of the ac line powered DPMs available. The AD2050 and AD2051 temperature meters meet DIN/NEMA dimension specifications.

QUALITY ASSURANCE

From design to shipment, Analog Devices works hard at quality control. DPM designs are evaluated with regard to electronic and environmental criteria that insure reliable operation in actual applications. Components are bought only from qualified vendors and are pre-tested before assembly. Quality control inspections throughout the manufacturing process insure good workmanship. Extensive automatic testing allows more thorough testing with less chance for errors. Each Analog Devices' DPM receives a one week failure-free burn-in before shipment.

FULL SUPPORT FOR THE OEM CUSTOMER

Analog Devices has anticipated the needs of the OEM user of DPMs. Besides offering attractive large quantity price discounts, Analog Devices stands behind its customers with worldwide sales and service facilities. Application assistance and technical information are available when needed to aid in the selection of the most economical DPM for each application.

High Performance 4½ Digit DPM For System Applications

AD2004

FEATURES
Floating Optically Isolated Analog Section
Excellent Common Mode Rejection: 120dB at ±300V
High Normal Mode Rejection: 60dB
5V dc Powered
Automatic Zero with Maximum Error: 0.01% ±1 Digit
LED Display with Latched Digital Outputs
Small Size: 1.8"H x 3"W x 2.5"D

APPLICATIONS
Industrial Weighing Systems
Process Control Monitoring
Precision Differential Measurement
Ground Loop Elimination
Off Ground Signal Measurements
Analytical and Scientific Instrumentation



GENERAL DESCRIPTION

Analog Devices' model AD2004 is a 4½ Digit, 5V dc powered digital panel meter offering 0.01% ±1 digit accuracy, resolution of 0.1mV, common mode voltage (CMV) of ±300V with a common mode rejection ratio (CMRR) of 120dB.

Using optically coupled isolation techniques for the signal channel, this new design is capable of performing precision measurements of floating differential voltages in noisy environments or under widely varying common mode voltage levels of up to ±300V. The optically isolated design assures ground loop elimination and permits critical measurement of off ground signals such as those found in the nuclear and process control industries.

The AD2004 features a 4½ digit light-emitting-diode (LED) display with a full scale range of 0 to ±1.9999 volts and latched digital data outputs and control interface signals. Automatic-zero correction circuitry measures and compensates for offset and offset drift errors thereby providing virtually no zero error.

The conversion rate of the AD2004 is normally 4 readings per second. However, an external trigger may be applied to vary the sampling rates from a maximum of 8 readings per second down to an indefinite hold rate. During conversion, the previous reading is held by the latched logic. The numeric readout is available as BCD data. Application of the metering system in a computer or data logging system is made easy with the availability of the "overrange," "polarity," "overload," and "status" signals.

The AD2004 can operate from the users 5V dc system supply, thereby, eliminating the shielding and decoupling needed for line powered units when the ac line must be routed near signal leads.

TYPICAL APPLICATIONS INCLUDE:

- Ground loop elimination between input transducer and output circuit functions.
- High resolution monitoring of small signals impressed on high off-ground voltages of up to ±300V.
- Electronic indicating weighing systems for industrial applications. Numerical output may be interfaced with a digital computer or data logging system.
- Digitally controlled industrial process where analog and digital signal isolation is required.
- Balanced strain gage bridge output measurement for industrial requirements.
- Digital indicating micrometer using a linear variable differential transformer (LVDT). Due to the high normal mode rejection ratio of the AD2004, the ac excitation of the LVDT does not induce errors into the system.
- Analytic and Scientific Instrument displays with isolated numeric readout.

FLOATING DIFFERENTIAL INPUT OFFERS HIGH CMV AND CMR

Figure 1 illustrates the isolation technique used to achieve high CMV and CMR.

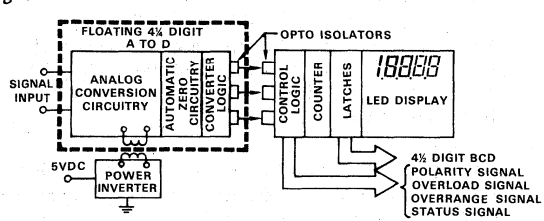


Figure 1. Simplified Block Diagram

For detailed information, contact factory.

SPECIFICATIONS (typical @ +25°C and +5V dc unless otherwise noted)

DISPLAY OUTPUT
- Display consists of five LEDs for data digits plus 100% overrange.
- Overload – Four data digits display zeros and flashes when reading exceeds the input range (>1.9999 volts).
- Decimal Points – Selectable at input connector.

INPUT
- Full Scale Range – 0 to ±1.9999 volts
- Automatic Zero
- Automatic Polarity
- Floating
- Bias Current – <1nA max
- Impedance – >100MΩ
- Overvoltage Protection – ±50V sustained without damage.
- Decimal Points (4) – Selectable by Logic "1" or by leaving open. Grounding the input turns decimal points off.

ACCURACY (30 Minute Warm-Up)
- 0.01% of Reading ±1 Digit
- Resolution – 0.1mV
- Temperature Range – 0 to +50°C operating
- Temperature Coefficient – ±15ppm/°C max

NORMAL MODE REJECTION
- 60dB without filter @ 50-60Hz minimum

COMMON MODE REJECTION
- 120dB typical dc-1kHz with 1kΩ unbalance

COMMON MODE VOLTAGE (with digital interface signals connected)
- ±300V dc (600V peak to peak)

DATA PROCESSING SIGNALS

	IN	OUT
• DTL/TTL Compatible Logic "0"	<0.8V	<0.4V
Logic "1"	>2.0V	>2.4V

- Inputs

  External Trigger – Operation in the External Trigger mode requires the External Hold input be held at Logic "0" or grounded. A negative going external trigger pulse (Logic "1" or Logic "0" and return) is required to start each conversion. The DPM is reset on the negative transition and a new conversion is triggered on the positive transition. The pulse width must be greater than 100ns. The STATUS signal is set at the negative transition and the actual conversion begins 0–3.3μs (maximum of 1 clock pulse) after the positive transition to allow synchronizing conversion with the internal clock.

  External Hold – When this input is grounded or held at 0.8V max, the last conversion is held and displayed. For a new conversion under internal control, this input must be open or at Logic "1".

- Output

  4BCD Digits (8421 Positive True) - Latched - 3TTL loads

  Overrange – Logic "1" indicates an overrange – Latched – 9TTL loads

  Overload – Logic "1" indicates the input has exceeded the input range – Latched – 9TTL loads

  Status Signal – Logic "0" indicates conversion is complete – 9TTL loads

  Polarity – Logic "1" with positive polarity input – Latched – 7TTL loads

CONVERSION TIME
- 125ms for *Full Scale* Input (145ms for AD2004/E)

SPEED
- External Trigger – 8 conversions per second (6 conversions per second for AD2004/E)
- Internal Conversion – 4 conversions per second
- Hold and Read on Command

SIZE AND WEIGHT
- 3"W x 1.8"H x 2.5"D (7.62 x 4.57 x 6.35cm) (overall depth for case and connector is 3.3" (8.38cm)). Weight, 8 oz. (227 gm).

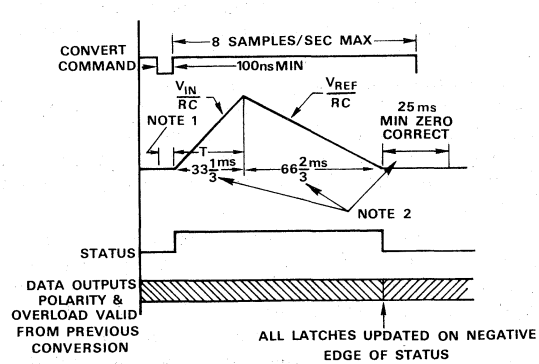
POWER
- 5V dc ±5% @ 800mA typ, 900mA max

ORDERING GUIDE
- AD2004 – Standard AD2004 as described above – tuned for peak normal mode rejection at 60Hz and its harmonics.
- AD2004/E – Standard AD2004 as described above – tuned for peak normal mode rejection at 50Hz and its harmonics.

CONNECTOR
- AC1600 6 feet of decade coded wire mated with "3M" Connector (Part No. 3414)

  AC1601 "3M" mating connector (Part No. 3414) only

Specifications subject to change without notice.



NOTE:
1. **Maximum Delay of One Clock Pulse 3.3μs to Synchronize with Clock.**
2. **AD2004E (50Hz Model) Timing.**
   Ramp up 40ms
   Ramp down 80ms
   Zero correct 25ms

   Maximum Trigger Rate 6ms

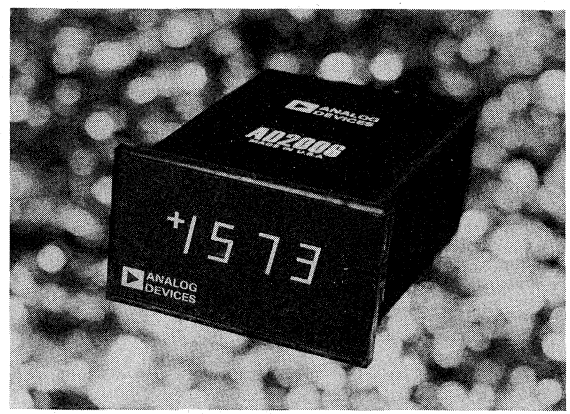
Figure 2. AD2004 Timing Diagram

AC Powered 3½ Digit DPM with Sperry Display

AD2006

FEATURES
AC Line Powered (+5V dc Powered Optional)
0.55" Sperry Display
Differential Input
Maximum Error: ±0.05%±1 Digit
AC Terminal Strip for Safety
Ratiometric Operation
Power Outputs for External Circuitry

APPLICATIONS
Analytical, Medical and Scientific Instrumentation
Industrial Test Equipment
Process Control Instrumentation



GENERAL DESCRIPTION

Analog Devices' model AD2006 is an ac line-powered, 3½ digit panel meter with Sperry displays for high visibility. The design of the AD2006 includes ratiometric operation and external power outputs to increase its application versatility.

The AD2006 provides high accuracy measurements of bipolar, differential input signals over a full scale range of ±1.999V, with a maximum error of ±0.05% (reading) ±1 digit. For most applications, the differential input section provides greater than 70dB of common mode rejection (CMRR) at common mode voltages (CMV) up to ±5V. In addition, the AD2006 can be floated on the ac power supply in the single-ended mode, allowing common mode voltages up to ±300V to be accommodated with common mode rejection exceeding 100dB. To insure the safety of operational personnel and interconnected equipment, especially at high CMV, a terminal strip is provided for connection of ac power.

For best visual readout, the AD2006 is internally programmed to make 5 readings per second. For data acquisition applications, up to 90 conversions per second can be externally triggered. DTL/TTL compatible parallel BCD data outputs and control signals are provided for interfacing to other digital data systems. To extend its versatility, external power outputs suitable for powering op amps and IC circuits are available to facilitate scaling or buffering inputs and driving external logic. Standard ratiometric operation allows normalizing inputs to an external reference voltage for making compensated measurements with bridge and potentiometric transducers.

In addition to ac line powered versions, the AD2006/D is available for operation from +5V dc power supplies commonly used for digital logic circuitry. The AD2006/D has identical performance specifications to all other AD2006 versions, except that it cannot be floated on the power supply for measurements at high common mode voltages and, of course, the +5V dc output is not available.

LARGE CLEAR DISPLAY ENHANCES READABILITY

The AD2006 uses large (0.55") Sperry, seven-segment, planar gas-discharge displays which appear as continuous solid digits. The display size, brightness and contrast ratio makes the AD2006 readable at distances up to 40 feet or more and in any ambient lighting condition including bright sunlight. The display is filtered to provide bright red digits and is readable without distortion over a 130° viewing angle. Overload conditions are indicated by displaying all dashes with the polarity sign remaining valid. The polarity sign can be blanked for display in engineering units where polarity indication is unnecessary.

For detailed information, contact factory.

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

DISPLAY OUTPUT
- Sperry Gas Discharge displays (seven segment, 0.55" (1.4cm)H), for 3 data digits, 100% overrange and polarity indication.
- Overload: Center segment dashes, polarity remains valid.
- Decimal Points: Selectable at input connector (contact closure).
- Polarity Sign may be blanked for display in engineering units.

INPUT
- Full Scale Range: 0 – ±1.999V
- Automatic Polarity
- Differential
- Bias Current: High Input – 3nA typ. (7nA maximum)
  Low Input – 200nA typ. (500nA maximum)
- Impedance: >100MΩ
- Overvoltage Protection: Analog Hi = ±50V sustained
  Analog Low = ±30V sustained

EXTERNAL REFERENCE INPUT
- Range: +5.8 to +6.8 Volts
- Input Impedance: >0.5MΩ
- Not protected against overvoltage
- Absolute Value Measurements: Internal +6.4V reference must be externally connected to the reference input.

ACCURACY
- Maximum Error: 0.05% of reading ±1 digit
- Resolution: 1mV
- Temperature Range: 0 to +50°C operating, -55°C to +85°C storage.
- Temperature Coefficient: Gain: <50ppm/°C
  Zero: <±50μV/°C

COMMON MODE REJECTION
- Differential Mode: 70dB, dc to 1kHz, with 1kΩ unbalance
- Floated on power supply transformer: >100dB[1]

COMMON MODE VOLTAGE
- Differential Mode: ±5V
- Floating Mode: ±300V dc (600V p-p ac)[1]

SPEED
- External Trigger: Up to 90 conversions per second (without display)
- Internal Trigger: 5 conversions per second
- Hold and Read on Command

CONVERSION TIME
- Normal Conversion: 9ms maximum
- Overload Conversion: 11ms maximum

INTERFACE SIGNALS
- DTL/TTL Compatible

	IN	OUT
logic "0"	<0.8V	<0.4V
logic "1"	>2.0V	>2.4V

- Inputs
  Polarity Sign Blanking: Logic "0" or grounding blanks the polarity sign being displayed.
  External Hold: Logic "0" or grounding this input disables the internal trigger, and the last conversion is held and displayed. External triggering can only be done when the AD2006 is in "HOLD".
  External Trigger: A negative trigger pulse applied to the external trigger input will initiate conversion.
- Outputs
  Status: All digital outputs are valid when status is low (logic "0"), logic "1" indicates conversion is in process.
  3BCD Digits (8421 positive true), unlatched, 6TTL loads.
  Overrange: Logic "1", unlatched, 6TTL loads, indicates overrange (>1.000V).
  Overload: Logic "1" unlatched, 6TTL loads, indicates overload (>1.999V), logic "0" indicates data is valid.
  Polarity: Logic "1", latched, 6TTL loads, indicates positive polarity.
  Polarity: Logic "1", latched, 6TTL loads indicates negative polarity.[2]

POWER
- AC line power (see option table), 7 Watts at nominal line voltage.
- AD2006/D: +5V dc @ 850mA

WARMUP
- 20 minutes to specified accuracy.

ADJUSTMENTS
(recommended calibration period: 6 months)
- Gain
- Zero Offset

EXTERNALLY AVAILABLE POWER OUTPUTS
- +5V ±5% @ 50mA (continuous short circuit protection)[1]
- ±15V ±10% @ 10mA (No short circuit protection; may require filtering for power supply-sensitive components)

SIZE
- 3"W x 1.8"H x 4"D (7.62 x 4.57 x 10.16cm) (4.95" (12.57cm) max to rear of mating connector, 4.80(12.19cm) max on AD2006/C)

WEIGHT
- 19 oz. (540gm) with ac power
- 10½ oz. (300gm) on AD2006/D

OPTIONAL FEATURES & ORDERING GUIDE
(All options on any AD2006 are listed on the label affixed to the bottom of the unit.)
- Power Supply Inputs (only one may be specified)

AD2006	115V ac ±10%	(50 – 60Hz)
AD2006/E	220V ac ±10%	(50 – 60Hz)
AD2006/H	240V ac ±10%	(50 – 60Hz)
AD2006/F	100V ac ±10%	(50 – 60Hz)
AD2006/D	+5V dc ±5%	

- Card Edge Connector: AD2006/C
- Any combination of the above options – excluding power inputs – can be specified. When ordering, specify power supply option first, then the other option desired. For example, an AD2006/E/C operates on 220V ac, and has the connector card edge.
- Display Lenses (only one may be specified):
  Lens-5 will be supplied if none is specified)
  Lens-5 Red w/ADI Logo
  Lens-6 Red no ADI Logo
  Lens-9 Amber w/ADI Logo
  Lens-10 Amber no ADI Logo

CONNECTOR
- 3M connector #3414, (optional) AC1600–34 pin connector and 6 ft. (1.83m) of color-coded, 34 way, 28 AWG flat woven cable.
- AC1601-connector only.
- AD2006/C requires 30 pin, 0.156 spacing, Viking No. 2VK 15D/1-2 or Cinch type 251 No. 5030A30.
- AD2006/C optional – Order AC1501.
- AC Power Line Cords are not supplied by ADI.

NOTES
[1] Not applicable to AD2006/D.
[2] Not applicable to AD2006/C.
Specifications subject to change without notice.

RATIOMETRIC OPERATION EXTENDS APPLICATIONS

The AD2006 has provision for making measurements normalized to an external reference voltage. This feature allows compensation for transducer outputs sensitive to excitation voltage variations, by making all measurements with reference to the excitation voltage. Figure 1 shows the AD2006 used with a bridge transducer which may be measuring temperature, pressure or any other physical parameter. The excitation voltage of the transducer is used as the reference input of the DPM. When used in the ratiometric mode, reference inputs in the range of +5.8 to 6.8 volts must be presented to the REFERENCE INPUT. The reference input must be relatively stable since the

DPM measures $\frac{\int_t E_{in}dt}{\int_t E_{ref}dt}$ not $\int_t \frac{E_{in}}{E_{ref}}dt$, and any variations

in the reference voltage during conversion may produce erroneous readings.

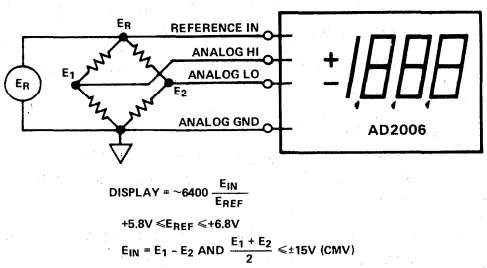


Figure 1. Bridge Transducer Measurements Using the AD2006's Ratiometric Input

The REFERENCE OUTPUT can be used for driving transducers if it is properly buffered using an external op amp. Figure 2 shows a thermistor temperature measuring circuit using the AD2006 to power the entire measurement system. The REFERENCE INPUT is a high impedence input which will not load any reference source, but this input is not protected from overload damage. If normal operation of a AD2006 is required, connection of the Reference Output to the Reference Input will allow operation using the internal +6.4V reference source.

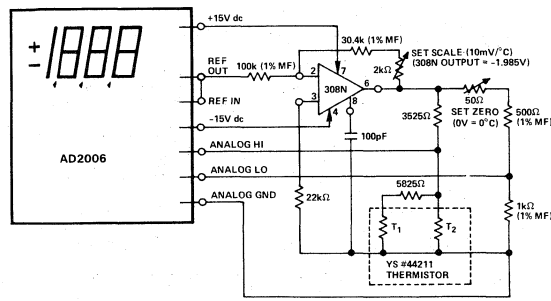


Figure 2. AD2006 Thermistor Temperature Measurement System

DC OUTPUTS CAN POWER EXTERNAL CIRCUITRY

Since the circuitry of the AD2006 requires ±15V and +5V to be generated internally, these voltages are made available to allow operation of external circuitry used in conjunction with the DPM. Sufficient power is available to drive op amps to scale inputs or even buffer the reference output to drive transducers such as in the thermistor application shown in Figure 2. The +5V output (not available on AD2006/D models) can be used for external logic. In many measurement systems, these power outputs will be sufficient to power all the circuitry external to the DPM. Although the regulation and ripple are adequate for the sensitive analog and digital circuitry of the AD2006, further filtering may be necessary for components that are extremely power supply sensitive.

AD2006 THEORY OF OPERATION

Figures 3 and 4 are the block diagram and timing diagram for the AD2006. The AD2006 uses a standard dual slope conversion technique with an absolute value voltage to current converter on the input. The absolute value of the analog input voltage produces a proportional current. When the convert command pulse initiates conversion, this current is integrated "up" for a fixed time period (1000 clock periods). The con-

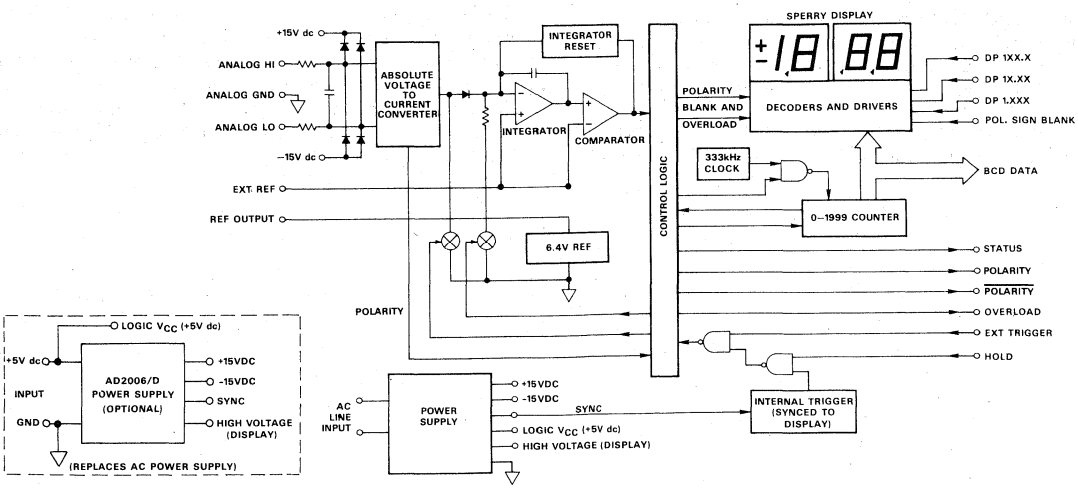


Figure 3. AD2006 Block Diagram

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verter then integrates "down" using a reference current of opposite polarity until the comparator senses that the integrator output voltage has returned to the original baseline. During the ramp-down period, the counters count clock pulses, and the number stored at the end of ramp-down is proportional to the analog input voltage.

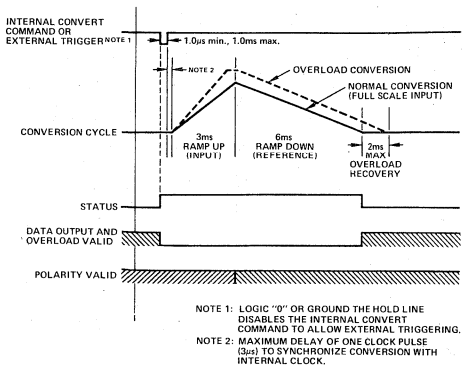


Figure 4. AD2006 Timing Diagram

INTERFACING THE AD2006

AC POWER CONNECTIONS: Connect ac power lines to the terminal strip on the rear of the AD2006. The ground line is internally connected to the case of the DPM. To assure safe operation, always use three-wire ac only, and cover the terminal strip with the protective cover provided. AD2006/D versions use the +5V dc Output and the Digital Ground as power supply INPUTS.

INPUT CONNECTIONS: Differential input signals should be connected between the ANALOG HI and the ANALOG LOW. The ANALOG GROUND must be connected to the system ground. For single-ended operation, connect the ANALOG LOW to the ANALOG GROUND. To allow operation at high common mode voltage, the AD2006 may be floated on the ac power supply transformer in the single-ended mode, without the digital interface signals connected. (See note on decimal points. AD2006/D versions can only be operated in the differential mode.) For absolute value measurements, the REFERENCE OUTPUT must be connected to the REFERENCE INPUT.

DECIMAL POINTS: Grounding the appropriate pin will illuminate the desired decimal point. (Note: Decimal points can be used in the "floating" mode if and only if the appropriate pin is grounded only to the AD2006 digital ground.

DIGITAL DATA OUTPUTS: The digital data outputs are unlatched, positive true, parallel BCD, at DTL/TTL logic levels. All data outputs are valid when the STATUS line is low (logic "0"). Erroneous data will be present when the conversion is in process and the STATUS line is high.

EXTERNAL CONTROL SIGNALS:

EXTERNAL HOLD: Logic "0" or grounding the HOLD input disables the internal trigger, and the last conversion is held and displayed. If a HOLD input is applied during conversion, the conversion will be completed and displayed. No further conversions will be made unless the HOLD input is removed or an EXTERNAL TRIGGER pulse is applied.

EXTERNAL TRIGGER: Operating in the EXTERNAL TRIGGER mode requires that the HOLD line be held at logic "0" or grounded. A negative going trigger pulse (logic "1" to logic "0" and return) of 1μs minimum and 1ms maximum width applied to the trigger input will initiate a conversion. The external trigger input must be a pulse since the STATUS is set on the negative-going edge of the pulse and the conversion is initiated on the positive-going edge of the pulse. Triggering at high rates asynchronously with line frequency may cause modulation of the display brightness, since the display is blanked both during conversion and during the negative half of the line cycle. *Care should be taken to insure that triggering does not occur during conversion, as this will cause an erroneous conversion.*

POLARITY SIGN: A logic "0" or ground blanks the polarity sign being displayed.

CALIBRATION PROCEDURES

WARNING: For the safety of personnel and interconnected equipment, all calibration should be done using a PLASTIC TRIMMING TOOL ONLY.

The accuracy of the AD2006 should be checked approximately every six months. A precision voltage reference or a calibrated DVM or DMM and a stable voltage source are required. The location of the adjustment potentiometers are shown on the mechanical layout drawings. Under most circumstances, only the gain will need adjustment. Should zero adjustment be necessary, adjust the zero before adjusting the gain.

ZERO OFFSET: Apply an input of 0V or short the analog inputs. If the meter does not read zero, adjust the zero offset pot until the meter reads zero and the polarity sign periodically changes. (Turning the pot clockwise, viewed from the back, makes the reading more negative.)

GAIN: Set the input of the panel meter to 1.900V. The input can be from a precision reference source, or from a stable voltage source set using a calibrated DVM or DMM. If the meter does not read 1900, adjust the gain pot to set the proper reading. (Turning the pot clockwise will increase the reading.) This is a bipolar adjustment, when correctly adjusted, the meter will read correctly for both polarities.

ANALOG DEVICES

3½ Digit AC Line Powered DPM

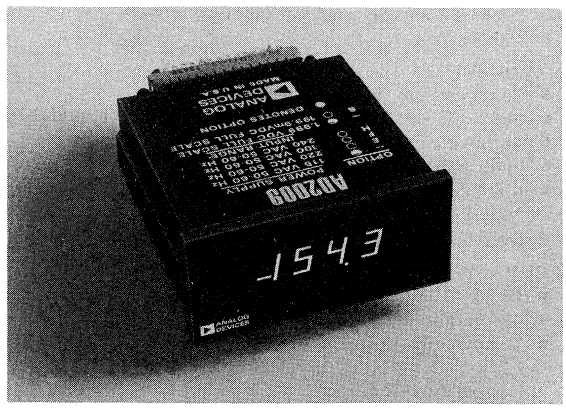
AD2009

FEATURES

- ac Line Powered
- Bright, Seven Segment Gas Discharge Display
- BCD Data Outputs Standard
- Hold and Trigger Control Signals
- Full Scale Ranges of ±1.999V or ±199.9mV
- Display Blanking Control
- Industry Standard Panel Cutout

APPLICATIONS

- General Purpose DPM Applications Requiring AC Power and a High Visibility Display
- Data Logging and Digital Feedback Control Systems



GENERAL DESCRIPTION

The AD2009 is a low cost 3½ digit, ac line powered DPM designed for general purpose DPM applications. The AD2009 measures bipolar input voltages over full scale ranges of either ±1.999V or ±199.9mV, with an accuracy of ±0.1% reading ±1 digit and displays the readings on large, bright 0.55″ (14mm) Beckman gas discharge displays.

LARGE, BRIGHT DISPLAY

For display only applications, the Beckman display offers excellent appearance and visibility. The AD2009 display is easily read up to 50 feet (15m) away and over all ambient lighting conditions. The non-glare lens allows a choice of either red or amber display colors, and is easily silk-screened with company logo or measurement units. External control of decimal points and display blanking is provided.

SIMPLE DATA INTERFACING

Since the AD2009 is designed around TTL logic circuits, parallel BCD data, TTL/DTL compatible, is a standard feature, allowing easy interfacing to a variety of data peripherals, such as digital comparators and line printers. Under internal control, the AD2009 converts at a nominal rate of six conversions per second. Using the Hold and Trigger controls, up to 100 conversions per second can be externally triggered.

INDUSTRY STANDARD CASE DESIGN

In response to industry's urgent need for DPM standardization, Analog Devices has adopted the most popular ac powered DPM panel cutout size for the AD2009 and all future ac line powered DPMs. Since this 3.924″ x 1.682″ (99.67 x 42.72mm) panel cutout is used by so many ac powered panel meters, the potential DPM customers can be assured that second-sources will be available and future new products will be usable without mechanical changes to their instruments or systems.

DESIGNED AND BUILT FOR RELIABILITY

Design and manufacturing techniques are chosen to insure reliability in the AD2009. Conservative design techniques and thorough component evaluation are only the beginning. Manufacturing processes are monitored by continuous quality assurance inspections to insure proper workmanship and testing. Like every other Analog Devices' DPM, each AD2009 is fully tested for electrical specifications, calibrated, and given one full week of failure free burn-in before shipment.

THEORY OF OPERATION

The AD2009 uses a dual slope conversion technique with an absolute value voltage to current converter input. The entire conversion cycle takes less than 10 milliseconds, allowing a complete conversion to be done during the negative half cycle of the ac line, and the resulting reading is displayed during the positive half cycle of the ac line. This scheme not only insures a flicker free display, but also allows externally triggered conversions at rates up to 100/second for data interfacing applications. In order to insure a bright display even during operation at low line voltages and to help insure the reliability of the Beckman displays, a separate power supply is provided to continually illuminate two "keep-alives" in the Beckman display.

SPECIFICATIONS (typical @ +25°C and nominal line voltage)

DISPLAY OUTPUT
- Beckman Seven Segment Gas Discharge Display, 0.55" High (14mm) for Three Data Digits, 100% Overrange and Negative Polarity Indication. Overload indicated by blanking the three data digits and displaying the "1" overrange. The polarity remains valid.
- Decimal Points Selectable at Input.
- Display Blanking

ANALOG INPUT
- Configuration: Bipolar, Single Ended
- Full Scale Range: ±1.999V or ±199.9mV (see S option)
- Automatic Polarity
- Input Impedance: 100MΩ dc
- Bias Current, Both Ranges: 3nA @ 2V FS, 20nA @ 200mV FS
- Overvoltage Protection, Both Ranges: 200V dc Sustained

ACCURACY
- ±0.1% ±1 Digit[1]
- Resolution: 1mV or 100μV (S option)
- Temperature Range[2]: 0 to +50°C Operating
  -25°C to +85°C Storage
- Temperature Coefficient:
  Gain (both ranges) — +30 ±20ppm/°C
  Zero Offset (2V Input) — ±30μV/°C
  (200mV Input) — ±10μV/°C
- Warm-Up Time to Rated Accuracy: 15 minutes
- Settling Time to Rated Accuracy: 0.3 second

NORMAL MODE REJECTION
- 18dB @ 60Hz

COMMON MODE REJECTION (1kΩ source imbalance @ 50-60Hz, with standard shielded transformer)
- 2V Input — 100dB
- 200mV Input — 100dB

COMMON MODE VOLTAGE
- ±300V dc (600V ac p-p) (floated on power supply transformer when BCD outputs and control signals are not used)

CONVERSION TIME
- 10ms

CONVERSION RATE
- Internal Trigger: 6 conversions per second
- External Trigger: 0-100 conversions per second

DIGITAL CONTROL SIGNALS
- DTL/TTL Compatible

	In	Out
Logic "0"	<0.8V	<0.4V
	>2.0V	>2.4V

CONTROL INPUTS[3]
- Display Blank (1TTL Load). Logic "0" or grounding blanks the entire display, not including the decimal points. Logic "1" or open circuit for normal operation. Display blanking has no effect on output data and the display reading is valid immediately upon removal of a blanking signal.
- Hold (1TTL Load). Logic "0" or grounding disables either the external or internal trigger and the last conversion is held and displayed.
- External Trigger (1TTL Load). Positive pulse (500μs max width) will initiate conversion.
- Decimal Points (Not TTL Compatibie). Grounding will illuminate the desired decimal point. External drive circuitry must be capable of withstanding 100V when the decimal points are turned off.

DATA OUTPUTS[3]
- 3BCD Digits (Drives 6TTL Loads). Positive true, unlatched
- Overrange (Drives 6TTL Loads). Unlatched, Logic "0" indicates overrange (≥1000).
- Overload (Drives 6TTL Loads). Unlatched, Logic "0" indicates overload (≥2000).
- Polarity (Drives 6TTL Loads). Latched, Logic "1" indicates positive polarity.
- Status (Drives 10TTL Loads). All digital outputs are valid when status is at Logic "0". Logic "1" indicates conversion is in progress.
- Internal Trigger Output (Not TTL Compatible). When connected to External Trigger Input will cause the AD2009 to convert at 6 conversions per second. This output can only be used for triggering the AD2009.

POWER INPUT
- ac line, 50-60Hz, 4.2 Watts at 60Hz; 4.7 Watts at 50Hz (at nominal line voltages).

CALIBRATION ADJUSTMENTS
- Gain
- Zero
- Recommended recalibration interval — 6 months

SIZE
- 4.22"W x 1.97"H x 4.15"L (107 x 50 x 112mm)
- 4.77"L (121mm) to rear of card edge connector
- Panel cutout required: 1.682 x 3.924" (42.72 x 99.67mm)

WEIGHT
- 15 ounces (425 grams)

OPTIONS[4] — ORDERING GUIDE
- ac Power Inputs (50-60Hz)
  AD2009 — 117V ac
  AD2009/E — 220V ac
  AD2009/F — 100V ac
  AD2009/H — 240V ac
- Input Ranges
  AD2009 — 1.999V dc Full Scale
  AD2009/S — 199.9mV dc Full Scale
- Display Lens Options[5]
  Lens 7 — Red with ADI Logo
  Lens 8 — Red without ADI Logo
  Lens 13 — Amber with ADI Logo
  Lens 14 — Amber without ADI Logo

CONNECTOR
- 30 Pin, 0.156" Spacing Card Edge Connector, Amphenol 225-215 24-601 (117) or Equivalent
- Optional: Order AC2611

[1] Guaranteed @ +25°C.
[2] Guaranteed.
[3] Not to be used when the AD2009 is floating on common mode voltages.
[4] Only one input range and ac power input may be specified.
[5] Lens 7 is supplied if no lens option is specified.

Specifications subject to change without notice.

INTERFACING THE AD2009

Input Connections

The AD2009 has a single ended input with common analog and digital grounds. When digital control lines and BCD data outputs are not used, the entire DPM can be floated on the power supply transformer at up to 300V dc common mode voltages. If these signals are used, care should be taken to insure against ground loops within the system causing erratic and/or erroneous readings.

Decimal Points

Grounding the proper pin will illuminate the desired decimal point. If external logic drives are used to control the decimal points, drive circuitry must be able to withstand 100V when the decimal points are turned off.

Display Blanking

The entire display (excluding decimal points) may be blanked by applying logic "0" or grounding the proper control input (pin 13). Blanking the display has no effect on the output data or the conversion process. The data remains valid during blanking and the DPM reading is correct immediately upon removal of the blanking signal.

Interfacing Digital Data Outputs

The digital data outputs of the AD2009 are unlatched, positive true, parallel BCD, at DTL/TTL logic levels. As shown in the timing diagram (Figure 1), all data outputs are valid when the STATUS line is low. The STATUS line is high during conversion when erroneous data will be present on the outputs.

TRIGGERING CONVERSIONS

The AD2009 may be triggered internally at six conversions per second, or externally at rates of up to 100 conversions per second. For internal triggering, the Internal Trigger Output (Pin 1) should be connected to the Trigger Input (Pin B). For external triggering, a positive trigger pulse (<500μs width) should be applied to the Trigger Input (Pin B). Whether internal or external triggering is used, the last reading can be held and displayed by grounding or applying logic "0" to the Hold Input. At high conversion rates, the display may flicker unless synchronized to the ac line input, but data outputs will remain valid.

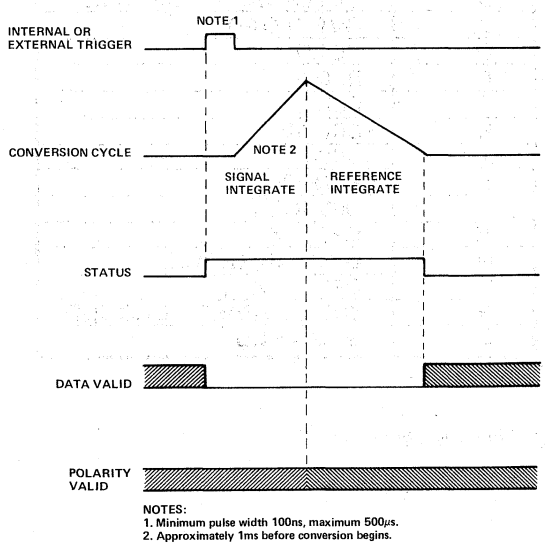


Figure 1. AD2009 Timing Diagram

CALIBRATION PROCEDURE

"WARNING: For the safety of personnel and interconnected equipment, all calibration should be done using a plastic trimming tool only."

A precision voltage reference is needed for calibration of the AD2009. The location of calibration potentiometers is shown in Figure 2. Before calibrating the AD2009, allow the unit to warmup to normal operating temperature. Always adjust the zero offset first then the gain.

Zero adjustment: Short the signal input (Pin 2) to the signal ground (Pin 10) and adjust the zero adjustment pot until the meter reads 000.

Gain adjustment: Apply an input of +1.900V (+190.0mV on AD2009/S) and adjust the gain pot until the meter reads 1900 exactly.

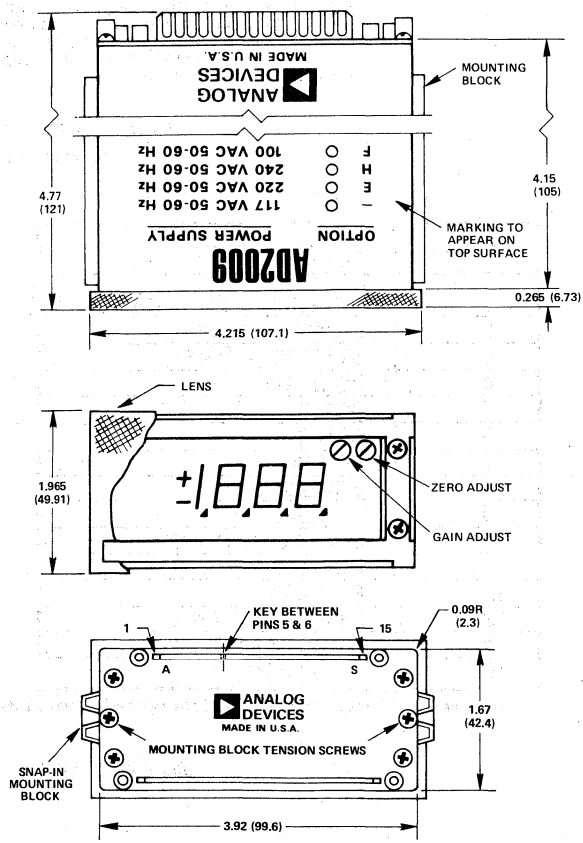
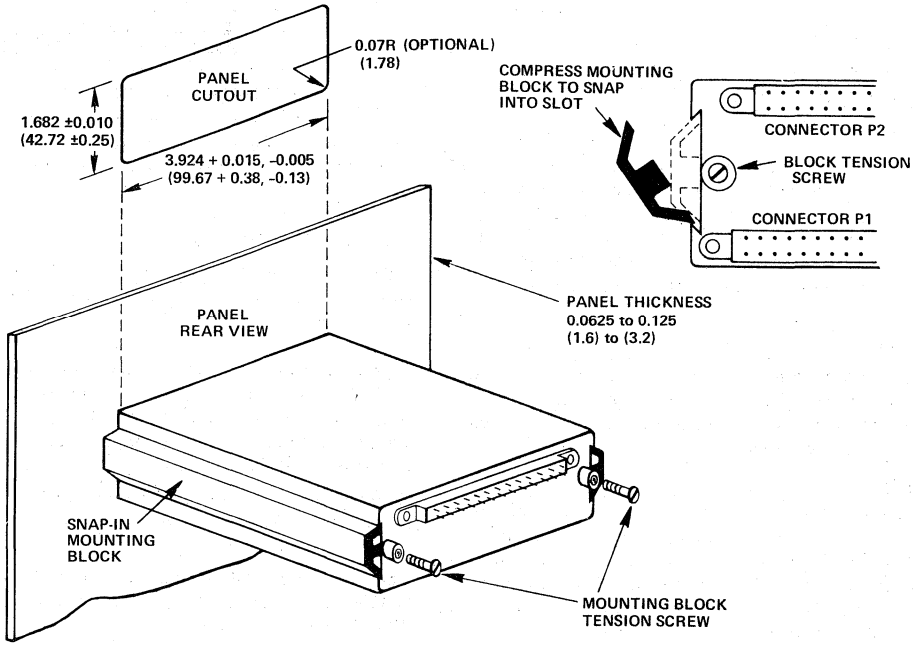


Figure 2. AD2009 Mechanical Outline (Dimensions shown in inches and (mm))

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MOUNTING INSTRUCTIONS:

1. SLIDE DPM THROUGH PANEL CUTOUT FROM FRONT OF PANEL.
2. SNAP MOUNTING BLOCK INTO SLOT ON DPM SIDES.
3. TIGHTEN MOUNTING BLOCK TENSION SCREWS SNUGLY TO SECURE DPM TO PANEL (DO NOT OVERTIGHTEN!)
4. SNAP LENS ONTO FRONT OF DPM.

Figure 3. AD2009 Mounting Instructions
(Dimensions shown in inches and (mm))

PIN REF	PIN FUNCTION
1	INTERNAL TRIGGER OUT[1]
2	SIGNAL INPUT
3	STATUS (PRINT)
4	POLARITY
5	BCD 8
6	BCD 2
7	BCD 80
8	BCD 20
9	BCD 800
10	SIGNAL GROUND
11	BCD 400
12	BCD 200
13	DISPLAY BLANK
14	OVERRANGE
15	ac LINE HI

KEY

PIN REF	PIN FUNCTION
A	NO CONNECTION
B	EXTERNAL TRIGGER IN[1]
C	OVERLOAD
D	HOLD
E	BCD 1
F	BCD 4
H	BCD 10
J	BCD 40
K	BCD 100
L	DP3/XX.X
M	DP2/X.XX
N	DIGITAL GROUND
P	DP1/.XXX
R	SHIELD (EARTH GROUND)
S	ac LINE LO

[1] Pin 1 and Pin B must be connected for operation with internal trigger.

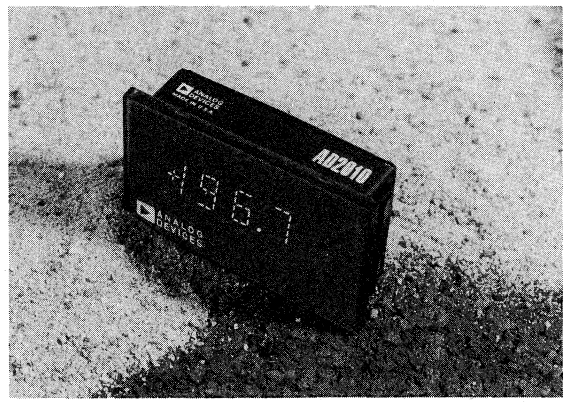
Figure 4. AD2009 Signal and Pin Designations

Low Cost 3½ Digit DPM For OEM Applications

AD2010

FEATURES
- LED Display with Latched Digital Outputs
- Small Size, Lightweight
- Automatic Zero Correction; Max Error: 0.05% ±1 Digit
- High Normal Mode Rejection: 40dB @ 50 or 60Hz
- Optional Ratiometric Operation
- Leading "0" Display Blanking
- 5V dc Powered

APPLICATIONS
- Medical/Scientific/Analytic Instruments
- Data Acquisition Systems
- Industrial Weighing Systems
- Readouts in Engineering Units
- Digital Thermometers



GENERAL DESCRIPTION

Analog Devices' model AD2010 represents an advance in price/performance capabilities of 3½ digit digital panel meters. The AD2010 offers 0.05% ±1 digit maximum error with bipolar, single ended input, resolution of 100μV, and a common mode rejection ratio of 60dB (CMRR) at ±200mV (CMV).

The AD2010 features a light-emitting-diode (LED) display with a full scale range of 0 to ±199.9 millivolts, latched digital data outputs and control interface signals, and leading zero display blanking. Automatic-zero correction circuitry measures and compensates for offset and offset drift errors, thereby providing virtually no error. Another useful feature of the AD2010 is its 5V dc operation. The AD2010 can operate from the users' 5V dc system supply, thereby eliminating the shielding and decoupling needed for line powered units when the ac line must be routed near signal leads.

To satisfy most application requirements, the conversion rate of the AD2010 is normally 4 readings per second. However, an external trigger may be applied to vary the sampling rates from a maximum of 24 readings per second down to an indefinite hold time. The AD2010 can also be connected for automatic conversion at its maximum conversion rate. During conversion, the previous reading is held by the latched logic. The numeric readout is available as BCD data. Application of the metering system in a computer or data logging system is made easy with the availability of the "overrange," "polarity," "overload," and "status" signals.

The AD2010/R option for ratiometric operation allows readings to be made of the ratio of two input voltages as well as the absolute value of the input. AD2010/R operation is described in a later section.

A simplified block diagram of the AD2010, illustrating the features described above is shown in Figure 1.

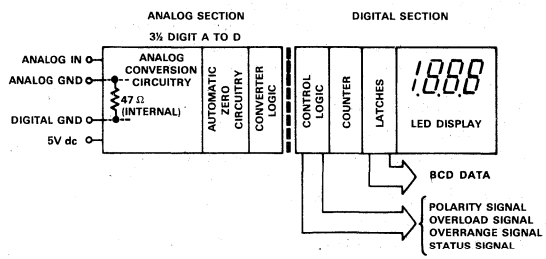


Figure 1. Simplified Block Diagram

IMPROVED NOISE IMMUNITY, ACCURACY AND ZERO STABILITY

Dual-slope integration, as used in the AD2010 and as described in the theory of operation section, offers several design benefits.

- Conversion accuracy, for example, is independent of both the timing capacitor value and the clock frequency, since they affect both the up ramp and down ramp integration in the same ratio.
- Normal mode noise at line frequencies or its harmonics is rejected since the average value of this noise is zero over the integration period.
- To achieve zero stability, a time interval during each conversion is provided to allow the automatic-zero correction circuitry to measure and compensate for offset and offset drift errors, thereby, providing virtually no zero error.

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For detailed information, contact factory.

SPECIFICATIONS (typical @ +25°C and +5VDC unless otherwise noted)

DISPLAY OUTPUT
- Display consists of four LED's (7 segment – 0.27" (6.9mm) high). for data digits plus 100% overrange and polarity indication.
- Overload – three data digits display zeros and flashes.
- Decimal Points – selectable at input connector.
- Leading "0" Display Blanking – controlled externally.

INPUT
- Full Scale Range – 0 to ±199.9 millivolts
- Automatic Zero
- Automatic Polarity
- Bias Current – 3nA
- DC Impedance – 100MΩ
- Overvoltage Protection – 20V sustained, 50V momentary without damage.
- Decimal Points (3) – illuminate with logic "1", extinguish with logic "0".

ACCURACY
- Maximum Error – 0.05% of reading ±1 digit
- Resolution – 0.1 millivolt
- Temperature Range – 0 to +50°C operating
  -30°C to +85°C storage
- Temperature Coefficient – ±50ppm/°C

NORMAL MODE REJECTION
- 40dB @ 60Hz (50Hz on AD2010/E)

COMMON MODE REJECTION
- 60dB @ ±200mV

CONVERSION RATE
- External Trigger – up to 24 conversions per second
- Internal Trigger – 4 conversions per second
- Automatic – A new conversion is initiated automatically upon completion of conversion in process; conversion rate will vary from 24/sec to 40/sec depending on input magnitude.
- Hold and Read upon command.

CONVERSION TIME
- Normal Conversion – 42ms max (full scale input)
  50ms max Model AD2010/E
- Overload Conversion – 62ms max

INTERFACE SIGNALS
- DTL/TTL Compatible

	IN	OUT
logic "0"	<0.8V	<0.4V
logic "1"	>2.0V	>2.4V

- Inputs

External Trigger – Operation in the "External Trigger" mode requires that the "External Hold" input be a logic "0" or ground.

Negative Trigger Pulses – Applying a logical "low" to the "HOLD" input disables the internal trigger. A negative trigger pulse (logic "1" to logic "0") of 1.0μs minimum applied to the "EXT TRIGGER" input will initiate conversion in the same manner as the internal oscillator. The external trigger should not be repeated, however, until the "status" indicates completion of the conversion in process.

Positive Trigger Pulses – The "HOLD" input can be used to trigger the AD2010 from a "normally low" signal with the "EXT TRIGGER" input open or logic "1". Following a "hold" a new reading will be initiated on the leading edge of the "hold" signal. Thus, a momentary positive pulse on the "HOLD" input can be used to trigger the AD2010. The drift correct interval, however, begins on the trailing edge of the positive pulse, so if the pulse width exceeds 1ms, the conversion will actually be initiated by the internal trigger.

Maximum Conversion Rate - Automatic – The AD2010 can also be connected for automatic conversion at its maximum conversion rate by connecting the "status" output back into the "hold" input. In this manner the status signal going high at the end of one conversion immediately initiates a new conversion. The pulses appearing on the status line can be used to step a multiplexer directly, since the built-in drift-correct delay of 8.33ms will allow settling of the input prior to conversion. A logic "0" applied to the "EXT TRIGGER" will inhibit the automatic trigger mode.

External Hold – Logic "0" or ground applied to this input disables the internal trigger and the last conversion is held and displayed. For a new conversion under internal control the input must be opened or at logic "1". For a new conversion under external control, a positive pulse of less than 1.0ms can be applied (as previously explained).

OUTPUTS
- 3 BCD Digits (8421 Positive True) - latched - 3TTL loads
- Overrange - logic "1" - latched - 6TTL loads, indicates overrange.
- Overload - logic "0" indicates overload (>199.9mV) logic "1" - latched - 6TTL loads, indicates data valid.
- Polarity - logic "1" - latched - 6TTL loads, indicates positive polarity input.
- Status - logic "0" - conversion in process logic "1" - latched - 6TTL loads, indicates conversion complete.

POWER
- +5V dc ±5%, 500mA

WARM UP
- Essentially none to specified accuracy

ADJUSTMENTS
- Range potentiometer for full scale calibration. Calibration recommended every six months.
- Normal Mode Rejection potentiometer (AD2010R only)

SIZE
- 3"W x 1.8"H x 0.84"D (76.2 x 45.7 x 21.3mm) (overall depth for case and printed circuit board extension is 1.40" (35.6mm)).

ORDERING GUIDE
- AD2010 - Standard AD2010 as described above - tuned for peak normal mode rejection at 60Hz and its harmonics.
- AD2010/E - Standard AD2010 as described above - tuned for peak normal mode rejection at 50Hz and its harmonics.
- AD2010/R - Standard AD2010 as described above - with Ratiometric option.
- AD2010/E/R - Standard AD2010/E as described above with Ratiometric option.

WEIGHT
- 4 oz. (113.5gm)

CONNECTOR RECOMMENDATION
- 30 Pin 0.156 spacing, Viking No. 2Vk 15D/1-2 or Cinch type 251 No. 5030A30.
- Optional - Order AC1501.

Specifications subject to change without notice.

5V dc OPERATION PROVIDES REDUCED NOISE PICKUP, IMPROVES RELIABILITY

A DPM designed for 5V dc operation offers the user many advantages over ac line powered devices. These benefits include:

- REDUCED NOISE PICKUP AND SUSCEPTIBILITY. Since line voltages are not required for operation, signal leads and internal circuitry need not be exposed to this source of noise, thereby, reducing power-frequency interference. A separate 5V dc power supply also provides additional isolation from line transients. Shielding and decoupling of the DPM circuits can also be eliminated. The DPM may be used as a component without danger of shock hazards to operational personnel or nearby circuitry.
- IMPROVED RELIABILITY. DPMs without power supplies generally require less space and generate less heat. The result is improved reliability while achieving lower cost. The smaller package size provides greater packaging flexibility and requires less ventilation behind the panel.

LEDs GIVE LONG LIFE, SHARP DISPLAY

The numeric outputs are displayed using 0.27" high, 7 segment, red LEDs. The LEDs provide the physical ruggedness typical of ICs, with a life expectancy in excess of 100,000 hours. The displayed numerals are sharp and easily readable at distances of up to 8 feet. The clean uncluttered look of the lens and case design further enhance the visual attractiveness of the display.

Optical features of the display include: a minimum photometric brightness of 200 foot-lamberts, and a 6300 angstrom, wavelength at peak emission (red). Other display features include programmable decimal points, automatic zero, 4 readings per second display rate, external trigger-and-hold rate of up to 24 readings per second, flashing-zeros overload indication, and leading "zero" display blanking.

COMPACT DESIGN FEATURES EASY SNAP-IN INSTALLATION

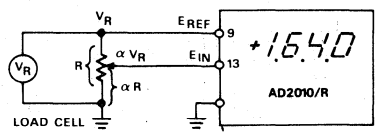
The AD2010 is housed in an aluminum case providing light weight, structural strength, optimum heat dissipation and shielding against external noise. With overall dimensions as shown in Figure 6, minimum space is required both on the panel and behind it. No tools are required for installation. You simply snap in the case, then snap on the filter and lens. Its light weight makes AD2010 ideal for applications in hinged panel equipment.

THEORY OF OPERATION

The AD2010 (Timing Diagram Figure 7) uses a dual-slope integrating A/D conversion scheme. When an input signal is applied to the DPM, it is applied to an integrator at the same time a counter is activated, initiating the count of clock pulses. After a predetermined number of counts (a fixed interval of time, T), the polarity of the input signal is strobed and a reference voltage having opposite polarity is applied to the integrator. At this instant, the accumulated charge on the integrating capacitor, C, is proportional to the average value of the input over the interval T. The integral of the reference is an opposite-going ramp having the fixed slop V_{REF}/RC. At the same time, the counter is again counting from zero. When the integrator output reaches zero, the count is stopped, and the analog circuitry is reset. Since the charge gained is proportional to $V_{IN}T$, and the equal amount of charge lost is proportional to $V_{REF}/\Delta t$, then the number of counts relative to the full count is proportional to $\Delta t/T$, or V_{IN}/V_{REF}. The output of the counter is a BCD number, which is decoded and displayed as the digital representation of the input.

AD2010/R OPTION EXPANDS APPLICATION

RATIOMETRIC OPERATION WITH EXTERNAL REFERENCE: The ratiometric option (AD2010/R) allows readings to be normalized to an external reference. This option can be useful where the analog voltage to be measured is accurate relative to an external reference which in itself is not accurate. A ratiometric application is illustrated in Figure 2. In this example, a position readout potentiometer operates with an external excitation supply which itself may not be very accurate. However, the potentiometer output relative to the reference supply, will be accurate due to the potentiometric configuration.



$$\text{DISPLAY} = 2000\left(\frac{E_{IN}}{E_{REF}}\right) = 2000\alpha$$

WHERE: $E_{IN} = \alpha V_R$, $E_{REF} = V_R$, $E_{IN} \leq E_{REF}$

LIMITS: $+100\text{mV} \leq E_{REF} \leq +300\text{mV}$ and $\pm 100\text{mV} \leq E_{IN}$ MAX $\leq \pm 200\text{mV}$

Figure 2. Ratiometric Operation

In the AD2010 the normal reference voltage is 200mV and is internally connected. The AD2010/R, however, has a "Reference Input" where an external reference voltage in the range of 100-300mV can be applied. The displayed output is given by:

$$\text{Display} = 2000\left(\frac{E_{IN}}{E_{REF}}\right)$$

The AD2010 also has a "Reference Output" where the normal 200mV reference is available. Absolute measurements using the AD2010/R can be made by externally connecting "Reference Output" to "Reference Input." The "Reference Output" is provided for this purpose only. It should be noted that the ratiometric option is intended only for normalization, and that the external reference must be a steady dc voltage.

INTERFACING THE DPM

The AD2010 can also be connected for automatic conversion at its maximum conversion rate by connecting the "status" output (Pin K) back into the "hold" input (Pin D). The 70ns pulses appearing on the status output line may be used to step a multiplexer. The status pulse width may be increased (if desired) as shown in Figure 3.

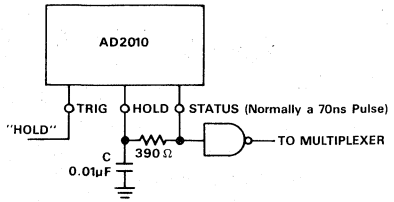


Figure 3. Increasing Pulse Width for Multiplexer Control in the Automatic Mode

To maximize the common mode rejection, an external 100μF @ 3V capacitor, C, is recommended as illustrated in Figure 4. The capacitor will reduce ground noise and ripple where the interconnection wires are 12 inches or longer. The polarization of C will depend on actual configuration.

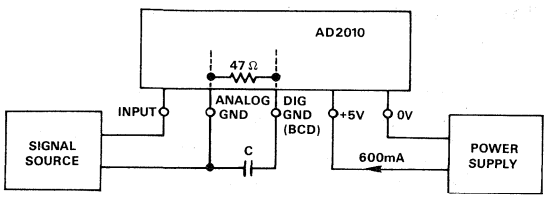


Figure 4. Insuring Maximum Common Mode Voltage Rejection

The latched digital data outputs and control interface signals are available at the rear of the AD2010. The signals may be interfaced with the system using a Cinch or Viking PC edge connector with 0.156" spacing or the AC1501 connector option. Signal and pin designations are shown in Figure 5.

PIN REF	PIN FUNCTION
1	EXTERNAL TRIGGER
2	800's DIGIT
— = KEY —	
3	400's DIGIT
4	DP 1XX.X
5	OVERLOAD
6	40's DIGIT
7	20's DIGIT
8	DIGITAL GRD
9*	REF IN (2010/R ONLY)
10	REF OUT
11	CLOCK OUT
12	4's DIGIT
13	ANALOG IN
14	ANALOG GRD
15	DP 1X.XX

PIN REF	PIN FUNCTION
A	1000's DIGIT (OVERRANGE)
B	100's DIGIT
C	200's DIGIT
D	HOLD
E	POLARITY
F	80's DIGIT
H	10's DIGIT
J	POWER SUPPLY GND
K	STATUS
L	8's DIGIT
M	1's DIGIT
N	+5V POWER INPUT
P	2's DIGIT
R	LEADING ZERO SUPPRESSION
S	DP 1.XXX

*WHEN IT IS DESIRED TO USE THE AD2010/R INTERNAL 200mV REFERENCE, EXTERNALLY CONNECT PIN "9" TO PIN "10". "REF IN" NOT PROTECTED AGAINST OVERLOAD.

Figure 5. AD2010 Connector Pin Designations

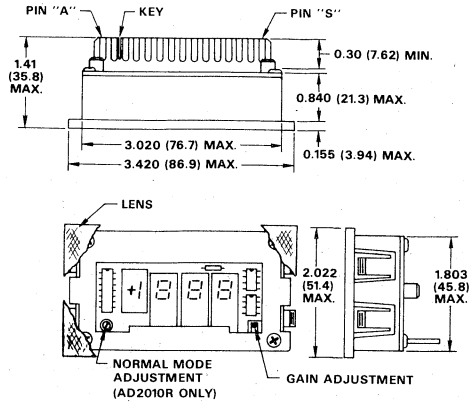
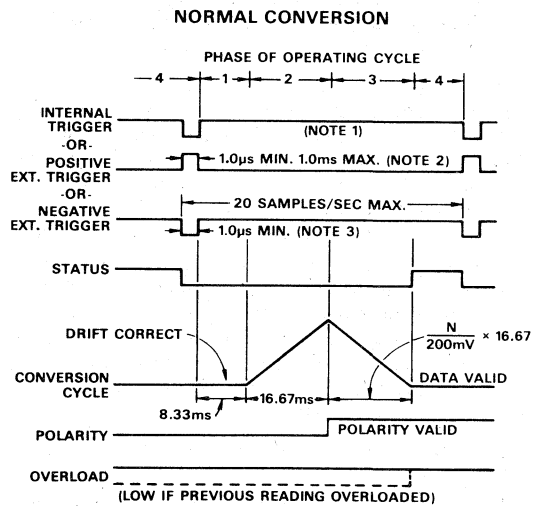
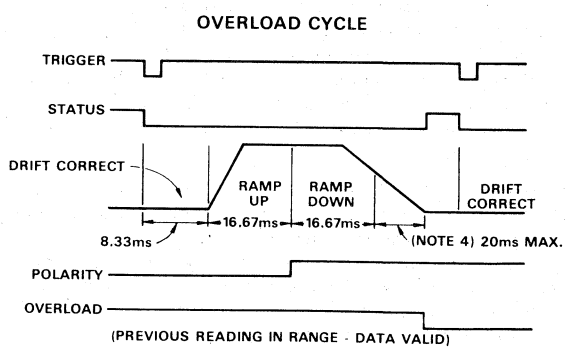


Figure 6. Overall Dimensions
All dimensions are given in inches and (mm).





NOTES:
1. The internal trigger rate is 4 conversions/sec.
2. A logic "0" applied to the "HOLD" input (pin D) disables the internal trigger. A positive pulse of 1ms max will initiate conversion. The "status" output may be used in this way for automatic triggering.
3. With the internal trigger disabled a negative pulse applied to the "external trigger" (pin 1) will initiate conversion.
4. Total ramp down time dependent on extent of overload (additional 20ms max).

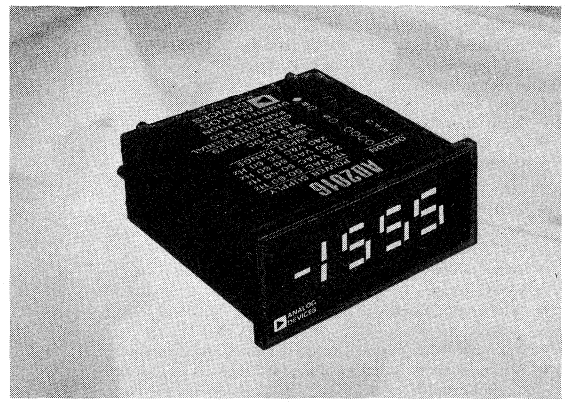
Figure 7. AD2010 Timing Diagram

Low Cost, 3½ Digit, Line Powered DPM With LED Display

AD2016

FEATURES
- "Second Generation" MOS/LSI Design
- Large 0.5" (13mm) LED Displays
- AC Line Powered, Universal Transformer
- ±199.9mV dc, ±1.999V dc or ±19.99V dc Full Scale Ranges
- Auto-Zero Correction
- Limited Differential Input
- Character Serial Data Output Standard, Parallel Data Optional
- Industry Standard Case Design — Second Sources Available

APPLICATIONS
- General Purpose ac Line Powered DPM Requirements



GENERAL DESCRIPTION

The AD2016 is a low cost, 3½ digit, line powered Digital Panel Meter with large LED displays, designed for general purpose DPM applications. The AD2016 measures bipolar input voltages over full scale ranges of ±199.9mV dc, ±1.999V dc or ±19.99V dc with an accuracy of ±0.05% reading ±0.025% full scale, ±1 digit. By using the "limited differential" input first used on Analog Devices' AD2010, the AD2016 input prevents ground loop problems and provides common mode noise rejection at common mode voltages up to ±200mV. Normal mode rejection is 40—45dB at 50 to 60Hz.

AD2016 models are available for operation at any line voltage and frequency required throughout the world. But, since the AD2016 uses a "universal" transformer, simple internal changes by bridging solder pads allow easy changing of the input power voltage for specific requirements. Thus, the OEM need not stock a variety of models for export requirements, but can easily change the voltage as required.

THE BENEFITS OF SECOND GENERATION DESIGN

The AD2016 is designed around MOS/LSI (Metal Oxide Semiconductor, Large Scale Integration) integrated circuits to reduce the number of components and power consumption, which greatly enhances reliability. However, these ICs provide the performance and features of earlier DPM design. The large 0.5 inch (13mm) LED displays provide the visual appeal of the gas discharge displays with the reliability of all solid state devices.

VERSATILE DATA INTERFACING

Since the AD2016 is designed around MOS/LSI circuits, the BCD output data is presented in a bit parallel, character serial format compatible to CMOS logic systems. Although some applications, such as interfacing with microprocessors are simplified with this data format, many applications involving line printers or comparators require parallel data outputs. For these applications, the AD2016/B provides parallel BCD data, TTL compatible. The conversion from a serial to a parallel format is done using shift registers, so the output data is fully latched. The AD2016/B also has two "Hold" inputs, one which stops DPM conversions and one which prevents data updating. Thus, the data outputs can be held for data transfer while the DPM continues to convert and update the display.

STANDARD PACKAGING/SECOND SOURCES

The AD2016 is packaged in Analog Devices' ac line powered DPM case, which requires the same panel cutout as cases used by most other manufacturers of ac line powered DPMs. In addition, the pin connections are the same as several other DPMs, including the Analog Devices' AD2009. (Even the BCD outputs of the AD2016/B are the same as the AD2009). With this commonality between DPMs, the user is assured of having second sources available or can update instrument or system designs to utilize the newer technology of the AD2016 without expensive mechanical or electrical changes to current products.

DESIGNED AND BUILT FOR RELIABILITY

Even beyond the reliability advantages of the LSI IC design and LED displays, the AD2016 has had extreme care taken in its design and manufacture to insure reliability. Manufacturing processes are monitored by continual quality assurance inspections to insure proper workmanship and testing. Automatic test equipment is used to test each DPM at board level and final assembly to assure thorough testing without error. And, each AD2016 gets one full week of failure-free burn-in at 50°C and with cycled power before shipment.

SPECIFICATIONS (typical at +25°C and nominal power supply voltage)

DISPLAY OUTPUT
- Light-emitting diode (LED), planar seven segment display readouts, 0.5″ (13mm) high for 3 data digits, 100% overrange and negative polarity indication. Overload indicated by flashing display, polarity remains valid.
- Decimal points (3) selectable at input connector.
- Display Blanking

ANALOG INPUT
- Configuration: bipolar, limited differential
- Full Scale Ranges: ±1.999V dc (standard), ±199mV dc ("S" option) or ±19.99V dc ("V" option)
- Automatic Polarity
- Auto Zero
- Input Impedance: 100MΩ (1MΩ – "V" option)
- Bias Current: 50pA
- Overvoltage Protection: ±200V dc sustained

ACCURACY
- ±0.05% reading ±0.025% full scale ±1 digit[1]
- Resolution: 1mV (standard), 100μV ("S" option), 10mV ("V" option)
- Temperature Range[2]: 0 to +50°C operating, -25°C to +85°C storage
- Temperature Coefficient: Gain: 50ppm/°C
  Zero: Auto Zero
- Warm Up Time to Rated Accuracy: less than one minute
- Settling Time to Rated Accuracy: 0.5 seconds (-full scale to +full scale)

NORMAL MODE REJECTION
- 45dB at 50–60Hz (40dB, "V" option)

COMMON MODE REJECTION

Input Range	Limited Differential (dc-10kHz, no imbalance)	Floating[3] (dc-100Hz, 1kΩ imbalance)
±199.9mV	50dB	120dB
±1.999V	35dB	120dB
±19.99V	15dB	100dB

COMMON MODE VOLTAGE
- Limited Differential Mode: ±200mV
- Floated On Power Supply Transformer When No BCD Outputs or Control Signals are Used: ±300V dc or 600V ac p-p

CONVERSION RATE
- 5 conversions per second
- Hold and read on command

CONTROL INPUTS[3]

Display Blanking (TTL/DTL Compatible, 3 TTL Loads)
Logic "0" or grounding blanks the entire display except for the decimal points at the tens and hundreds digits. Logic "1" or open circuit for normal operation. Display blanking has no effect on the output data and the display is valid immediately upon removal of a blanking input.

Converter Hold (CMOS, TTL/DTL Compatible, 1 LPTTL Load)
Logic "0" or grounding causes the DPM to cease conversions and display the data from the last conversion. Logic "1" or open circuit for normal operation. After a "Converter Hold" is removed, one or two conversions are needed before the reading or BCD data is valid.

Decimal Points (Not TTL Compatible)
Grounding or Logic "0" will illuminate the desired decimal point. External drive circuitry must sink 50mA at a 25% duty cycle when a decimal point is illuminated.

Data Hold (AD2016/B Only) (TTL/DTL Compatible, 1 TTL Load)
Logic "0" or grounding inhibits updating of the latched parallel output data of the AD2016/B. Logic "1" or open circuit allows the data to be updated after each DPM conversion. This input has no effect on the normal conversion of the DPM.

DATA OUTPUTS[3] (See applications section for details on the data outputs)

Bit Parallel, Character Serial BCD Data Outputs Standard. 4 BCD data bits, positive true logic (CMOS, LPTTL or LP Schottky compatible, 1 LP Schottky load); 4 digit strobes (CMOS, TTL compatible, 1 TTL load); Polarity (CMOS, TTL compatible, 1 TTL load), logic "1" indicates positive polarity; Clock Output (CMOS, LPTTL or LP Schottky compatible, 1 LP Schottky load); Status Output (CMOS or LPTTL, 1 LPTTL load) are available.

Parallel BCD (AD2016/B) Optional. 3 BCD digits, Overrange, Overload and Data Ready Outputs (TTL compatible, 4 TTL loads). BCD data outputs are latched, positive true logic. The Overload Output is at Logic "0" for inputs greater than full scale range, Logic "1" when other data outputs are valid. Polarity Output (TTL compatible, 4 TTL loads latched) indicates positive polarity when high (Logic "1").

POWER INPUT

AC line, 50–60Hz. Power Consumption: 3.3 watts at 60Hz; 3.8 watts at 50Hz (Parallel BCD: 3.9 watts at 60Hz; 4.4 watts at 50Hz).

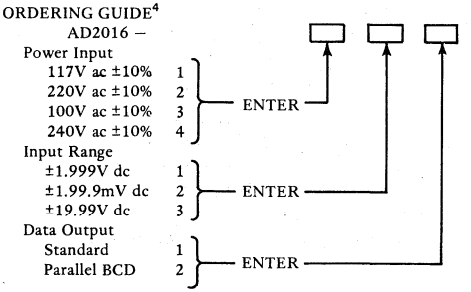
CALIBRATION ADJUSTMENTS (See application section for calibration instructions)
- Gain
- Zero (capability for system zero adjustment, meter is auto zero)
- Recommended recalibration interval: six months

SIZE
- 4.22″W x 1.97″H x 4.15″L (107 x 50 x 105mm)
- 4.77″ (121mm) to rear of card edge connector
- Panel Cutout Required: 1.682″ x 3.924″ (42.72 x 99.67mm)

WEIGHT
- 12 ounces (340 grams)

ORDERING GUIDE[4]

AD2016 –



DISPLAY LENS OPTIONS[5]
- Lens 7 – Red with ADI logo
- Lens 8 – Red without ADI logo

CONNECTORS

30 pin, 0.156 spacing card edge connector, Amphenol 225-21524-601 (117) or equivalent

Optional: Order AC2611

[1] Guaranteed at +25°C.
[2] Guaranteed
[3] No control inputs or data outputs can be used when the AD2016 is floated on the power supply transformer at high common mode voltages.
[4] Only one AC power supply input and input range may be specified. The "B" option can be ordered with any combination of power and range options.
[5] Lens 7 is supplied if no lens option is specified.

Specifications subject to change without notice.

Wiring Connections

Figure 1 is a wiring diagram for AD2016 applications. The "limited differential" input uses a 47Ω resistor to isolate the analog input from the digital and power supply sections to prevent ground loop problems. The analog ground must be connected to Pin 10 only, since there may be up to 200mV voltage difference between the input and digital ground.

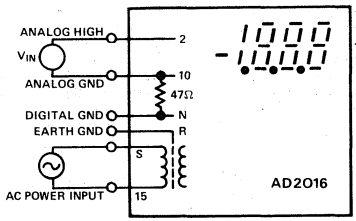


Figure 1. AD2016 Wiring Interconnections

Decimal Points

Grounding, or Logic "0", applied to the appropriate pin will illuminate the desired decimal point. External drive circuitry, if used, must sink 50mA at a 25% duty cycle when the decimal point is turned on.

Display Blanking

Grounding, or Logic "0", blanks the entire AD2016 display with the exception of the decimal points on the tens and hundreds digit. The display is valid immediately upon removal of a blanking signal.

Converter Hold

Grounding, or Logic "0", causes the DPM to cease conversions and display the data from the last conversion. After a "Converter Hold" input is removed, the auto zero circuitry requires one or two conversions before the display and data outputs are again valid.

Data Hold (AD2016/B only)

Grounding, or Logic "0", on this input inhibits updating of the parallel BCD outputs of the AD2016/B. If the parallel data is interfaced to a printer, comparators, or a computer, requiring the data to be held stable for proper operation, the Data Hold input should be used to prevent data updating, but the DPM itself will continue making conversions. After a Data Hold input is removed, the BCD data will be updated at the end of the conversion cycle.

Extended Range Measurements

Although the full scale range of the AD2016 is 2000 counts, and it flashes the display to indicate overrange beyond this point, it actually makes measurements up to approximately 3000 counts. Beyond this point, it will flash a constant number. Thus, one can use this extra measurement range as a guide to reducing the input to the normal range. Note that the display will flash only the three full digits, since it is impossible to flash a "2" on the overrange readout. Thus, a reading of 2.300V or 230.0mV on an AD2016 will read as "300" and will be flashing.

BCD outputs on the standard AD2016 also will be valid up through the 3000 count range, but the BCD parallel outputs of the AD2016/B will indicate overload beyond 1999 counts.

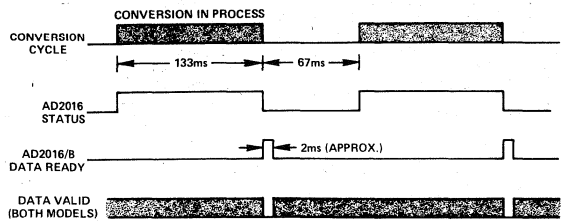


Figure 2. AD2016 Timing Diagram

Interfacing Data Outputs – Character Serial Data

The BCD data outputs standard on the AD2016 are in a bit parallel character serial format. There are four BCD bit outputs (1, 2, 4, 8) and four digit outputs (10^0, 10^1, 10^2, 10^3) called D1, D2, D3 and D4 respectively. The BCD bits are gated onto the output lines sequentially in the order D1, D3, D2, D4 and the BCD bits are valid for the digit whose digit line is high. The serial output data is valid except when it is being updated, which occurs within 2 milliseconds after the Status line goes low, indicating the end of a conversion.

Interfacing Data Outputs – Parallel Data

The AD2016/B has data outputs in a full parallel BCD format. The output data is latched and is valid except for a 2ms period at the end of conversion when the "Data Ready" output is high (Logic "1"). As described above, the "Data Hold" input can be used to inhibit updating of the parallel data outputs without affecting the conversion of the DPM.

Calibration Procedures

A precision voltage reference is needed for the calibration of the AD2016. The location of the calibration potentiometers is shown in Figure 5. Always adjust the zero offset before the gain if zero adjustment is necessary.

Zero Adjustment: Short the signal inputs (Pins 2 and 10) and adjust the zero offset potentiometer until the meter reads 000.

Gain Adjustment: Apply an input of +1.800V (+180.0mV on AD2016/S, or +18.00V on AD2016/V) and adjust the gain potentiometer until the meter reads 1800 exactly.

AD2016 CHARACTER SERIAL

PIN REF	PIN FUNCTION
1	NC
2	SIGNAL INPUT
3	STATUS ($\overline{\text{PRINT}}$)
4	POLARITY
5	NC
6	D4
7	BCD 2^3
8	BCD 2^1
9	CLOCK OUTPUT
10	SIGNAL GROUND
11	NC
12	D3
13	DISPLAY BLANK
14	NC
15	AC LINE HIGH

KEY

PIN REF	PIN FUNCTION
A	NC
B	NC
C	NC
D	CONVERTER HOLD
E	D2
F	NC
H	BCD 2^0
J	BCD 2^2
K	D1
L	DP3 XX.X
M	DP2 X.XX
N	DIGITAL GROUND
P	DP1 .XXX
R	SHIELD (EARTH GROUND)
S	AC LINE LOW

(NC = NO CONNECTION)

Figure 3.

AD2016/B

PIN REF	PIN FUNCTION
1	DATA HOLD
2	SIGNAL INPUT
3	DATA READY
4	POLARITY
5	BCD 8
6	BCD 2
7	BCD 80
8	BCD 20
9	BCD 800
10	SIGNAL GROUND
11	BCD 400
12	BCD 200
13	DISPLAY BLANK
14	OVERRANGE
15	AC LINE HIGH

KEY

PIN REF	PIN FUNCTION
A	NC
B	NC
C	OVERLOAD
D	CONVERTER HOLD
E	BCD 1
F	BCD 4
H	BCD 10
J	BCD 40
K	BCD 100
L	DP3 XX.X
M	DP2 X.XX
N	DIGITAL GROUND
P	DP1 .XXX
R	SHIELD (EARTH GROUND)
S	AC LINE LOW

Figure 4.

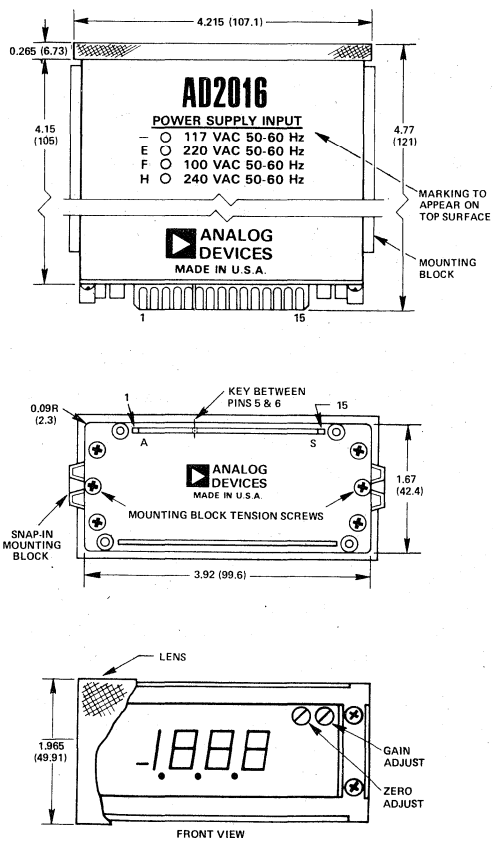


Figure 5. AD2016 Mechanical Outline (Dimensions shown in inches and (mm))

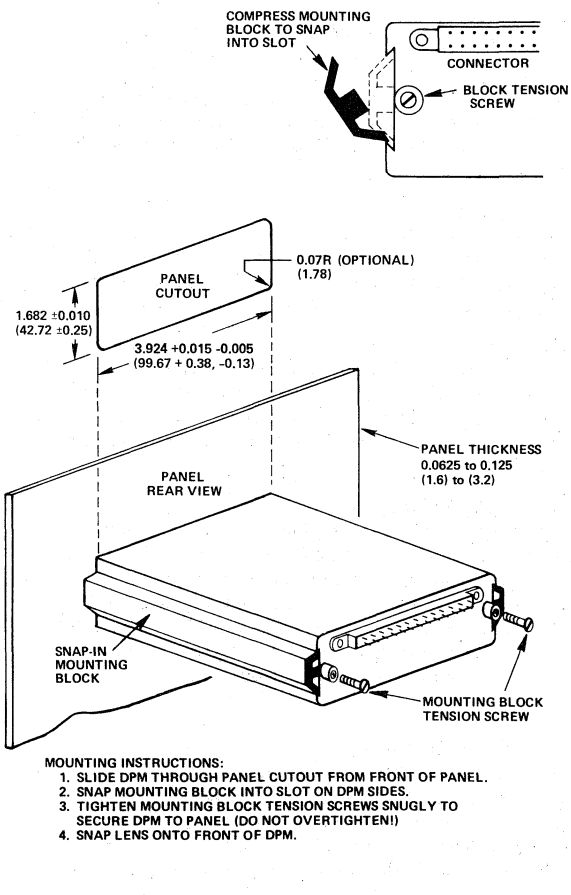


Figure 6. AD2016 Mounting Instructions (Dimensions shown in inches and (mm))

ANALOG DEVICES

Low Cost 3½ Digit Logic Powered DPM With LED Displays

AD2021

FEATURES
- "Second Generation" MOS-LSI Design
- Large 0.5" (13mm) LED Displays
- +5VDC Logic Powered
- ±1.999V, ±199.9mV or ±19.99V Full Scale Ranges
- Limited Differential Input
- Low Power Consumption: 2.0 Watts
- Small Size, Industry Standard Case Design

APPLICATIONS
- General Purpose Logic Powered DPM Applications
- Portable Applications Requiring Low Power Consumption



GENERAL DESCRIPTION

The AD2021 is a low cost, 3½ digit, +5V dc logic powered digital panel meter with large LED displays. While designed for general purpose DPM applications, the small size, light weight and low power consumption of the AD2021 make it an ideal digital readout for modern, compact instrument designs.

THE BENEFITS OF "SECOND GENERATION" DESIGN

The AD2021 is designed around MOS-LSI (Metal-Oxide-Semiconductor, Large Scale Integration) integrated circuits, which greatly reduce the number of components, and thereby the size, and reduce power consumption to 2.0 watts. Both the lower power consumption and fewer interconnections between components promise greatly increased reliability, and the circuit design maintains the performance and features of earlier DPMs. Large 0.5 inch (13mm) LED displays offer the visual appeal of gas discharge displays with the ruggedness and lifetime of all solid state devices.

EXCELLENT PERFORMANCE AND EASY APPLICATION

The AD2021 measures input voltage over a full scale range of ±1.999V dc or ±199.9mV dc ("S" option) with an accuracy of ±0.05% reading ±0.025% full scale ±1 digit. Using the "limited differential" input first used on Analog Devices' AD2010, the AD2021 prevents ground loop problems and provides 35 to 50dB of common mode rejection at common mode voltages up to ±200mV. Normal mode rejection is 40dB at 50Hz to 60Hz.

BCD data outputs are provided in a bit parallel, character serial format compatible to CMOS logic systems. For those applications requiring parallel BCD data, schemes for making the serial to parallel conversion are available. Controls to hold readings, select decimal points and blank the display are provided.

DESIGNED AND BUILT FOR RELIABILITY

The AD2021 is packaged in Analog Devices' logic powered DPM case size, only 1.25 inches (32mm) deep. The small size of this DPM makes it easy to accommodate in any instrument design, and since several other manufacturers now use the same panel cutout for logic powered DPMs, this industry standardization allows mechanical second sourcing. In addition, the AD2021 uses the same pin connections as the AD2010 (except in BCD outputs, of course) as a convenience to allow updating designs to take advantage of the second generation design and larger display of the AD2021. Each AD2021 receives a full one week failure free burn-in before shipment.

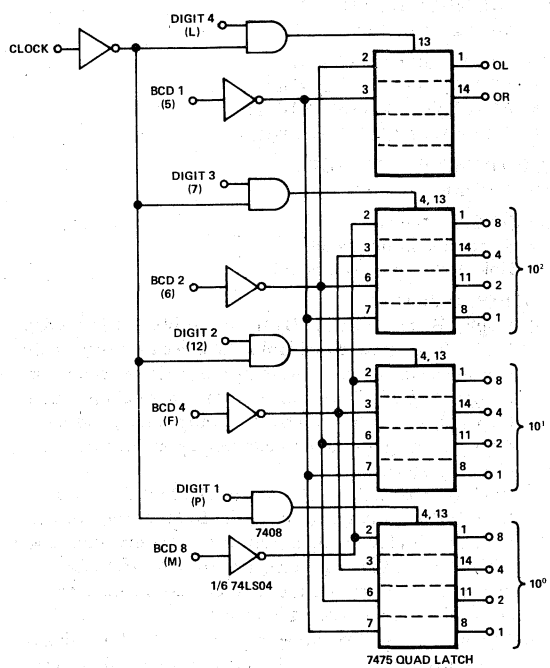


Figure 1. AD2021 Bit Parallel Character Serial to Full Parallel Data Conversion. AD2021 Pin Connections are Shown in Parentheses.

For detailed information, contact factory.

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SPECIFICATIONS (typical at +25°C and nominal power supply voltage)

DISPLAY OUTPUT
- Light emitting diode, planar seven segment display readouts, 0.5″ (13mm) high for three data digits, 100% overrange and negative polarity indication. Overload indicated by flashing display, polarity remains valid.
- Decimal points selectable at input connector.
- Display blanking on three data digits (does not affect overrange digit, polarity sign of decimal points).

ANALOG INPUT
- Configuration: bipolar, limited differential
- Full Scale Range: ±1.999V or ±199.9mV ("S" option) ±19.99V ("V" option)
- Automatic Polarity
- Auto Zero
- Input Impedance: 100MΩ (1MΩ – "V" option)
- Bias Current: 50pA
- Overvoltage Protection: ±50V dc, sustained

ACCURACY
- ±0.05% reading ±0.025% full scale ±1 digit[1]
- Resolution: 1mV or 100μV ("S" option)
- Temperature Range[2]: 0 to +50°C operating; -25°C to +85°C storage
- Temperature Coefficient: Gain: 50ppm/°C
  Zero: auto zero
- Warm-Up Time to Rated Accuracy: less than one minute
- Settling Time to Rated Accuracy: 0.4 second

NORMAL MODE REJECTION
- 40dB at 50–60Hz

COMMON MODE REJECTION
- AD2021: 35dB (dc -10kHz)
- AD2021/S: 50dB (dc -10kHz)
- AD2021/V: 15dB (dc -10kHz)

COMMON MODE VOLTAGE
- ±200mV

CONVERSION RATE
- 5 conversions per second
- Hold and read on command

CONTROL INPUTS
- Display Blanking: (TTL, DTL compatible, 2 TTL loads). Logic "0" or grounding blanks the three data digits only, not the decimal points, overrange digit (if on) and polarity sign. Logic "1" or open circuit for normal operation. Display blanking has no effect on output data and the display reading is valid immediately upon removal of a blanking signal.
- Hold: (CMOS, DTL, TTL compatible, 1LP TTL load). Logic "0" or grounding causes the DPM to cease conversions and display the data from the last conversion. Logic "1" or open circuit for normal operation. After the "Hold" input is removed, one to two conversions are needed before the reading is valid.
- Decimal Points: Grounding or Logic "0" will illuminate the desired decimal point. External drive circuitry must sink 35mA peak at a 25% duty cycle when the decimal points are illuminated.

DATA OUTPUTS (See Application Section for details on data outputs)
- BCD Data Outputs: (CMOS, LP TTL or LP Schottky compatible), bit parallel, character serial format.
- Digit Strobe Outputs: (CMOS, DTL, TTL compatible, one TTL load). Logic "1" on any of these lines indicates the output data is valid for that digit.
- Polarity Output: (CMOS, TTL, DTL compatible, one TTL load). Logic "1" indicates positive polarity input, logic "0" indicates negative polarity.
- Status: (CMOS or LP TTL compatible). When this signal is at Logic "1", the output data is valid.
- Clock: (CMOS, DTL, TTL compatible, one TTL load). The clock signal is brought out to facilitate conversion from character serial to parallel data.
- INTERFACING DATA OUTPUTS. The BCD data outputs are in a bit parallel, character serial format. There are four BCD bit outputs (1, 2, 4, 8) and four digit outputs (10^0, 10^1, 10^2, 10^3). The BCD digits are gated onto the output lines sequentially, and the BCD bits are valid for the digit whose digit line is high. The data is valid except when being updated which occurs within 2 milliseconds after the status line goes low.

REFERENCE OUTPUT
- A 6.4V ±5% analog reference output is made available. This reference should be buffered and filtered if use in external circuitry is desired.

POWER INPUT
- +5V dc ±5%, 1.45 watts

CALIBRATION ADJUSTMENTS (See Application Section for calibration instructions)
- Gain
- Zero
- Recommended recalibration interval: six months

SIZE
- 3″W x 1.8″H x 1.33″D (76 x 46 x 34mm)
- 1.90″ (48mm) overall depth to rear of card edge connector.
- Panel cutout required: 3.175″ x 1.810″ (80.65 x 45.97mm).

WEIGHT
- 4 ounces, (115 grams)

OPTIONS – ORDERING GUIDE
- Input Voltage Range: AD2021 – 1.999V dc Full Scale
  AD2021/S – 199.9mV dc Full Scale
  AD2021/V – 1.999V dc Full Scale

  (Consult the factory or representative for other input ranges)
- Display Lens Option[3]: Lens 5 – Red with ADI logo
  Lens 6 – Red without ADI logo

CONNECTOR
- 30 pin, 0.156″ spacing card edge connector, Viking 2VK15D/1-2 or equivalent
- Optional: Order AC1501

[1] Guaranteed at 25°C and nominal supply voltage
[2] Guaranteed
[3] If no lens is specified, Lens 5 will be supplied.

Specifications subject to change without notice.

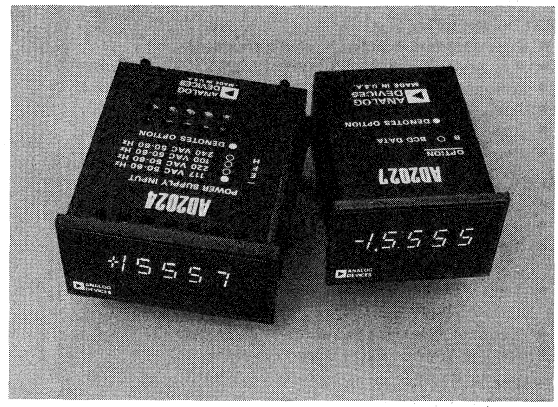
Low Cost 4½ Digit DPMs With LED Displays

AD2024/AD2027

FEATURES
- "Second Generation" MOS-LSI Design
- Large 0.43" (11mm) LED Displays
- 4½ Digit Resolution – 20,000 Counts Full Scale
- Limited Differential Input
- Either Line Powered (AD2024) or Logic Powered (AD2027)
- Industry Standard Case Designs

APPLICATIONS

High Resolution/High Accuracy Readout for:
- Test Equipment
- Process Control Instrumentation
- Analytical and Scientific Instruments



GENERAL DESCRIPTION

The AD2024 and AD2027 are low cost 4½ digit DPMs with large LED displays. Both units offer the same features and identical performance, but the AD2024 is ac line powered and the AD2027 is +5V dc powered.

THE BENEFITS OF SECOND GENERATION DESIGN

The AD2024 and AD2027 are designed around MOS-LSI (Metal Oxide Semiconductor, Large Scale Integration) integrated circuits which greatly reduce the number of components and interconnections required to provide the performance and features expected in a high resolution 4½ digit DPM.

This "Second Generation" design, therefore, offers greatly increased reliability and significantly lower cost at little compromise in performance. The large 0.43 inch (11mm) LED displays offer the brightness and readability previously available only with gas discharge displays with the added advantage of an all solid state component.

HIGH RESOLUTION AND VERSATILE FEATURES

These DPMs measure dc input voltages over a full scale range of ±1.9999V with an accuracy of ±0.005% reading ±0.005% of full scale ± 1 digit. Using the "limited differential" input first used by Analog Devices on the AD2010, the AD2024 and AD2027 prevent ground loop problems and provide 50dB of common mode rejection at common mode voltages up to ±200mV. Normal mode rejection is 25dB at 50–60Hz.

BCD data outputs are provided in a bit parallel, character serial format compatible with CMOS logic systems. When applications require parallel BCD data, such as interfaces to printers, comparators or slave displays, parallel BCD output options are available that are compatible to standard TTL logic systems.

External power supply outputs at +5V and -25V (-25V only on the AD2027) are made available for powering external circuitry. In addition, control inputs for conversion "Hold", display blanking and decimal point selection are provided.

INDUSTRY STANDARD CASE DESIGNS

Although both the AD2024 and AD2027 have identical electrical designs, they are packaged in the case sizes that have become industry standards for ac line powered and +5V dc logic powered DPMs respectively. The AD2024 fits the 3.924" x 1.682" (99.67 x 42.74mm) panel cutout common to most ac line powered DPMs, and the AD2027 fits the 3.175" x 1.810" (80.65 x 45.97mm) panel cutout of the Analog Devices logic power case design, now used by several other manufacturers of logic powered DPMs. Thus, interchangeability is assured, allowing mechanical second sourcing for both these DPMs.

DESIGNED AND BUILT FOR RELIABILITY

Even beyond the reliability advantages of the LSI-IC design and LED displays, the AD2024 and AD2027 have had extreme care taken in their design and manufacture to insure reliability. Manufacturing processes are monitored by continual quality assurance inspections to insure proper workmanship and testing. Automatic test equipment is used to test each DPM thoroughly and without error. And each AD2024 and AD2027, like every Analog Devices DPM, receives a full one week failure-free burn-in before shipment.

For detailed information, contact factory.

SPECIFICATIONS

DISPLAY OUTPUTS
- Seven Segment LED Display, 0.43" (11mm) high, for four data digits, 100% overrange and polarity indication.
- Overload indication by blanking all digits, polarity sign remains valid.
- Decimal points (4) selectable at input.
- Display Blanking

ANALOG INPUT
- Configuration: Bipolar, limited differential
- Full Scale Range: ±1.9999V (±19.999V, "V" Option)
- Automatic Polarity
- Input Impedance: 100MΩ (1MΩ, "V" Option)
- Bias Current: 30nA (3nA, "V" Option)
- Overvoltage Protection: 120V rms sustained

ACCURACY
- ±0.005% reading ±0.005% full scale ±1 digit [1]
- Resolution: 100μV
- Temperature Range[2]: 0 to +50°C operating. -20 to +85°C storage. (AD2024/B: 0 to +45°C operating)
- Temperature Coefficient: Gain: ±30ppm/°C. Zero Offset: ±10μV/°C (±40ppm/°C & ±100μV/°C, "V" Option)
- Warmup Time: One minute to rated accuracy
- Settling Time to Rated Accuracy: 450ms

NORMAL MODE REJECTION
- 25dB at 50–60Hz

COMMON MODE REJECTION
- 50dB, dc to 1kHz, ±200mV common mode voltage
- AD2024 (floated on power supply transformer if data outputs and control signals are not used) – 110dB at 120V rms common mode voltage, 1kΩ imbalance at input.

CONVERSION TIME
- 180ms for full scale reading
- 210ms for overload conversion

CONVERSION RATE
- 5 conversions per second

DIGITAL INTERFACE SIGNALS
- Inputs

  Display Blank – (DTL/TTL Compatible, 4 TTL Loads). Logic "0" or grounding blanks display, including polarity sign, but not decimal points. The display is valid immediately upon removal of the blanking signal.

  Hold – (DTL/TTL Compatible, 2 TTL Loads). Logic "0" or grounding causes the DPM to hold and display the last conversion. Upon removal of the hold, the DPM resumes conversions.

  Decimal Points – (Not TTL Compatible). Logic "0" or grounding turns on appropriate decimal point. External circuitry must sink 60mA when a decimal point is illuminated.
- Outputs

  DTL/TTL Compatible[3] – Status. Logic "1" indicates conversion in process. All digital outputs are valid when status is at logic "0". 5 TTL loads. – Polarity. Logic "1" indicates positive polarity, latched. 5 TTL loads.

  CMOS and LP Schottky Compatible – Overload, Logic "1" indicates overload (≥20,000), latched. – BCD outputs. 4½ BCD digits, character serial, bit parallel, 1 LP Schottky Load.

  Digital Strobe Outputs – (CMOS or LP Schottky Compatible) Logic "1" on any of these line indicates the output data is valid for that digit, 1 LP Schottky Load.

  Parallel BCD Output (Option "B"). – 4½ BCD digits, positive true, latched. Drives 5 TTL loads. – Data Ready. Logic "1" indicates output data is valid. Drives 2 TTL loads.

EXTERNAL POWER SUPPLY OUTPUTS
- AD2024: +5V at 25mA, -25V at 5mA
- AD2027: -25V at 5mA

POWER SUPPLY INPUTS
- AD2024: ac line, 50-60Hz, 4.2W
- AD2027: +5V dc, ±5% at 850mA

CALIBRATION ADJUSTMENTS
- Gain
- Zero
- Recommended recalibration interval: 6 months

SIZE
- AD2024: 3.92"W x 1.67"H x 4.48"D (100 x 42 x 114mm)
  Panel cutout: 3.930" x 1.682" (99.8 x 42.7mm)
- AD2027: 3"W x 1.8"H x 4"D (76 x 46 x 102mm)
  Panel cutout: 3.175" x 1.810" (80.65 x 45.97mm)

WEIGHT
- AD2024: 14 ounces (395 grams)
- AD2027: 10 ounces (280 grams)

OPTIONS – ORDERING GUIDE
- AD2024

  AC Power Inputs

  AD2024 – 117V ac
  AD2024/E – 220V ac
  AD2024/F – 100V ac
  AD2024/H – 240V ac
  } ±10%

  Input Range Options

  AD2024 – ±1.9999V Full Scale
  AD2024V – ±19.999V Full Scale

  Data Output Options (available with any power input options)

  AD2024 – Character serial data outputs
  AD2024/B – Parallel BCD option

  Display Lens Options[4]

  Lens 7 – Red with ADI logo
  Lens 8 – Red without ADI logo

  Connector – 36 pin, 0.156" spacing, card edge connector, Viking 2VK18D/1-2 or equivalent. – Optional: Order AC2610.

  AD2024/B option also requires a 30 pin, 0.156" spacing, card edge connector, Viking 2VK15D/1-2 or equivalent. – Optional: Order AC1501.
- AD2027

  Input Range Options

  AD2027 – ±1.9999V Full Scale
  AD2027V – ±19.999V Full Scale

  Data Output Options

  AD2027 – Character serial data outputs
  AD2027/B – Parallel BCD option

  Display Lens Options[4]

  Lens 5 – Red with ADI logo
  Lens 6 – Red without ADI logo

  Connector – AC1501 (see above) or equivalent. AD2027/B option requires two each.

[1] Guaranteed at +25°C and nominal power supply voltage.
[2] Guaranteed.
[3] For CMOS compatibility, 3.3k pullup resistors to the +5V output of the DPM are required.
[4] If no lens is specified, Lens 5 or 7 is supplied as appropriate.
Specifications subject to change without notice.

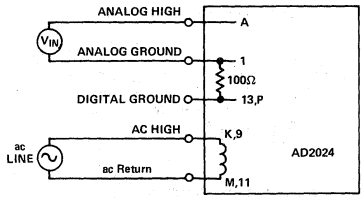


Figure 1. AD2024 Wiring Interconnections

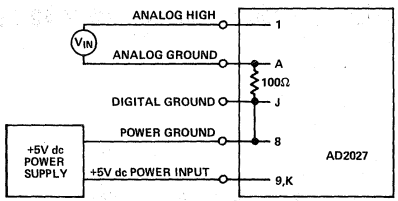


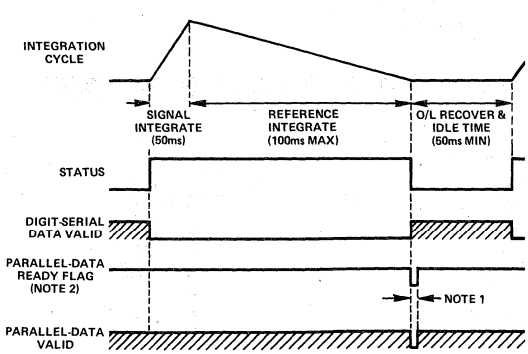
Figure 2. AD2027 Wiring Interconnections

Interfacing Data Outputs

The standard data outputs are in a bit parallel character serial format compatible to CMOS and LP Schottky logic systems. The BCD outputs are multiplexed, and a digit output is provided for each of the five digits of output. Thus, the four BCD lines on the output at a given time are valid for the digit whose digit line is currently high. The bit parallel character serial data is valid when the DPM status line is low for a period of 50ms between each conversion cycle. The overload line is latched output which is at logic "1", whenever the input exceeds the full 20,000 count range.

Optional parallel BCD outputs ("B" option) are available on a separate card which is internally connected to the DPM. The output data then is presented in a full parallel format and is latched. The parallel data is valid whenever the data ready output is high.

Pin connections for the "B" option are shown in the interconnection tables and a full timing diagram is shown in Figure 3.



NOTE 1. APPROX. 5ms REQUIRED TO LOAD PARALLEL-OUT REGISTERS.
NOTE 2. B OPTION.

Figure 3. AD2024/AD2027 Timing Diagram

PIN	FUNCTION	PIN	FUNCTION
1	Analog Ground	A	Analog High
2	10^1 Digit	B	10^0 Digit (LSD)
= KEY		= KEY	
3	BCD 2	C	10^2 Digit
4	10^3 Digit	D	BCD 4
5	BCD 8	E	BCD 1
6	Mux Step 1	F	10^4 Digit (MSD)
7	+5V dc (Out)	H	-25V dc (Out)
8	NC	J	NC
9	ac High	K	ac High
10	NC	L	NC
11	ac RETURN	M	ac Return
12	NC	N	NC
13	Digital Ground	P	Digital Ground
14	NC	R	Status
15	Polarity	S	Hold
16	Display Blank	T	DP1.XXXX
17	DP1XXX.X	U	DP1X.XXX
18	Overload	V	DP1XX.XX

AD2024 – Signal and Pin Connections

PIN	FUNCTION	PIN	FUNCTION
1	Analog High	A	Analog Ground
2	10^0 Digit (LSD)	B	Mux Step 1
3	BCD 8	C	BCD 1
4	BCD 2	D	BCD 4
5	10^4 Digit (MSD)	E	10^1 Digit
6	10^3 Digit	F	10^2 Digit
7	NC	H	-25VDC (Out)
8	Power Ground	J	Digital Ground
9	+5V (In)	K	+5V (In)
10	NC	L	NC
= KEY		= KEY	
11	Display Blank	M	NC
12	Hold	N	Polarity
13	Overload	P	Status
14	DP1.XXXX	R	DP1X.XXX
15	DP1XX.XX	S	DP1XXX.X

NOTE 1: BCD multiplexer clock pulse available for remote placement of BCD option.

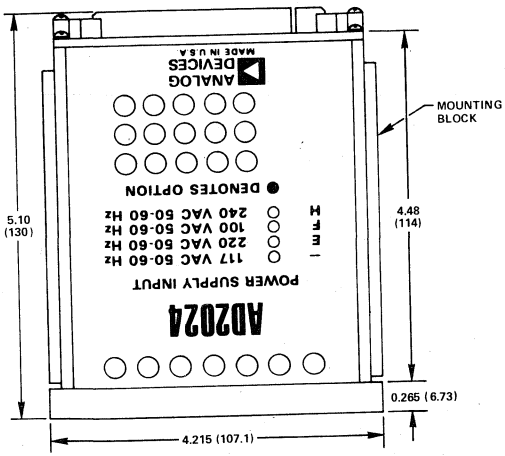
AD2027 – Signal and Pin Connections

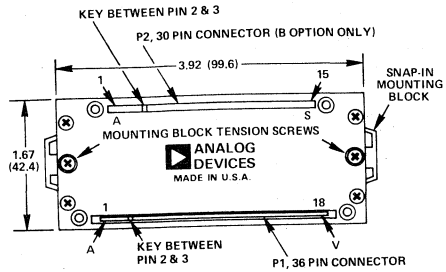
PIN	FUNCTION	PIN	FUNCTION
1	+5V dc (In)	A	NC (Do Not Use)
2	BCD 1 (In)	B	BCD 8 (In)
= KEY		= KEY	
3	BCD 4 (In)	C	BCD 2 (In)
4	BCD 2000	D	BCD 4
5	BCD 40	E	BCD 80
6	BCD 800	F	BCD 8000
7	BCD 100	H	BCD 1000
8	BCD 10,000	J	BCD 200
9	BCD 20	K	BCD 2
10	BCD 8	L	BCD 10
11	BCD 1	M	BCD 4000
12	BCD 400	N	10^4 Digit (In)
13	Data Ready	P	Status (In)
14	Polarity (In)	R	Mux Step (In)
15	Polarity (Out)	S	Digital Ground

NOTES: 1) Overload output is on main DPM connector.
2) Pins marked "In" are made available for remote placement of BCD option card and are not normally used since all connections are interval.

AD2024/AD2027 BCD Options – Signal and Pin Connections

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PANEL CUTOUT: 3.930 X 1.682 (99.82 X 42.72)

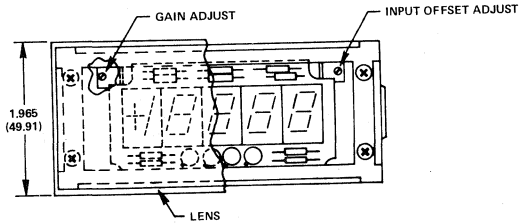
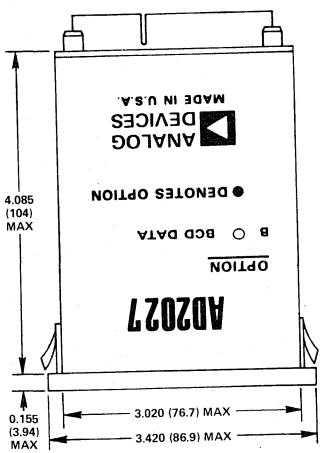
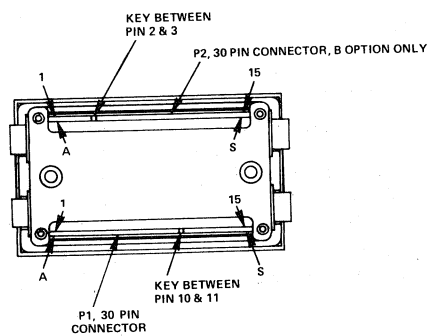
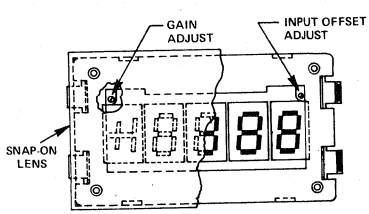


Figure 4. AD2024 Mechanical Outline (Dimensions shown in inches and (mm))





PANEL CUTOUT: 3.175 X 1.180 (80.65 X 45.97)



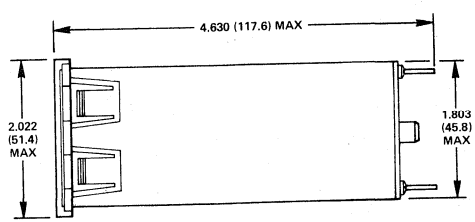


Figure 5. AD2027 Mechanical Outline (Dimensions shown in inches and (mm))

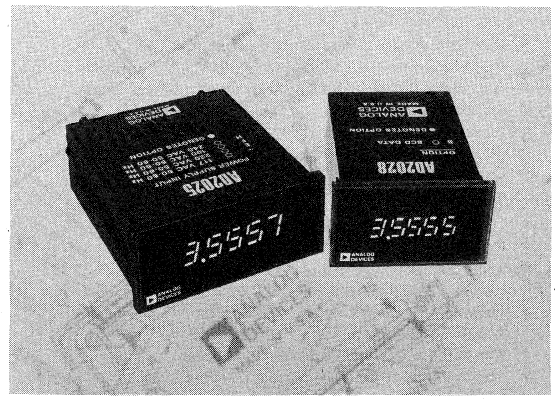
Low Cost 4¾ Digit DPMs With LED Displays

AD2025/AD2028

FEATURES
- "Second Generation" MOS-LSI Design
- Large 0.43" (11mm) LED Displays
- 4¾ Digit Resolution – 40,000 Counts Full Scale
- Limited Differential Input
- Either Line Powered (AD2025) or Logic Powered (AD2028)
- Interchangeable with 4½ Digit DPMs (AD2024 or AD2027)
- Industry Standard Case Designs

APPLICATIONS

High Resolution/High Accuracy Readout for:
- Test Equipment
- Process Control Instrumentation
- Analytical and Scientific Instruments



GENERAL DESCRIPTION

The AD2025 and AD2028 are low cost 4¾ digit DPMs with large LED displays. Both units offer the same features and identical performance, but the AD2025 is ac line powered and the AD2028 is +5V dc powered.

The AD2025 and AD2028 are interchangeable with two 4½ digit DPMs available from Analog Devices, the AD2024 and AD2027 respectively. Thus, they can be used in applications where either a 4¾ or 4½ digit display may be desirable in one basic application.

THE BENEFITS OF SECOND GENERATION DESIGN

The AD2025 and AD2028 are designed around MOS-LSI (Metal Oxide Semiconductor, Large Scale Integration) integrated circuits which greatly reduce the number of components and interconnections required to provide the performance and features expected in a high resolution 4¾ digit DPM.

This "Second Generation" design, therefore, offers greatly increased reliability and significantly lower cost at little compromise in performance. The large 0.43 inch (11mm) LED displays offer the brightness and readability previously available only with gas discharge displays with the added advantage of an all solid state component.

HIGH RESOLUTION AND VERSATILE FEATURES

These DPMs measure DC input voltages over a full scale range of ±3.9999V or ±39.999V with an accuracy of ±0.005% reading ±0.005% of full scale ±1 digit. Using the "limited differential" input first used by Analog Devices on the AD2010, the AD2025 and AD2028 prevent ground loop problems and provide 50dB of common mode rejection at common mode voltages up to ±200mV. Normal mode rejection is 25dB at 50–60Hz.

BCD data outputs are provided in a bit parallel, character serial format compatible with CMOS logic systems. When applications require parallel BCD data, such as interfaces to printers, comparators or slave displays, parallel BCD output options are available that are compatible to standard TTL logic systems.

External power supply outputs at +5V and -25V (-25V only on the AD2028) are made available for powering external circuitry. In addition, control inputs for conversion "Hold", display blanking and decimal point selection are provided.

INDUSTRY STANDARD CASE DESIGNS

Although both the AD2025 and AD2028 have identical electrical designs, they are packaged in the case sizes that have become industry standards for ac line powered and +5V dc logic powered DPMs respectively. The AD2025 fits the 3.924" x 1.682" (99.67 x 42.74mm) panel cutout common to most ac line powered DPMs, and the AD2028 fits the 3.175" x 1.810" (80.65 x 45.97mm) panel cutout of the Analog Devices logic power case design, now used by several other manufacturers of logic powered DPMs. Thus, interchangeability is assured, allowing mechanical second sourcing for both these DPMs.

DESIGNED AND BUILT FOR RELIABILITY

Even beyond the reliability advantages of the LSI-IC design and LED displays, the AD2025 and AD2028 have had extreme care taken in their design and manufacture to insure reliability. Manufacturing processes are monitored by continual quality assurance inspections to insure proper workmanship and testing. Automatic test equipment is used to test each DPM thoroughly and without error. And each AD2025 and AD2028, like every Analog Devices DPM, receives a full one week failure-free burn-in with power cycling before shipment.

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'or detailed information, contact factory.

SPECIFICATIONS (typical at +25°C and nominal power supply voltage)

DISPLAY OUTPUTS
- Seven Segment LED Display, 0.43″ (11mm) high, for four data digits and 300% overrange.
- Overload indication by blanking all digits except overrange, which indicates "0".
- Decimal points (5) selectable at input.
- Display Blanking

ANALOG INPUT
- Configuration: Bipolar, limited differential
- Full Scale Range: ±3.9999V (±39.999V, "V" option)
- Automatic Polarity (See applications section for details on polarity display)
- Input Impedance: 100MΩ (1MΩ, "V" option)
- Bias Current: 30nA (3nA, "V" option)
- Overvoltage Protection: 120V rms sustained

ACCURACY
- ±0.005% reading ±0.005% full scale ±1 digit[1]
- Resolution: 100μV (1mV, "V" option)
- Temperature Range[2]: 0 to +50°C operating. -20 to +85°C storage. (AD2025/B: 0 to +45°C operating)
- Temperature Coefficient: Gain: ±30ppm/°C. Zero Offset: ±10μV/°C (±40ppm/°C and ±100μV/°C, "V" option)
- Warmup Time: One minute to rated accuracy
- Settling Time to Rated Accuracy: 450ms

NORMAL MODE REJECTION
- 25dB at 50–60Hz

COMMON MODE REJECTION
- 50dB, DC to 1kHz, ±200mV common mode voltage
- AD2025 (floated on power supply transformer if data outputs and control signals are not used) – 110dB at 120V rms common mode voltage, 1kΩ imbalance at input.

CONVERSION TIME
- 300ms for full scale reading
- 400ms for overload conversion

CONVERSION RATE
- 3 conversions per second

DIGITAL INTERFACE SIGNALS
- Inputs

  Display Blank – (open collector TTL Compatible, 4 TTL Loads). Logic "0" or grounding blanks display, but not decimal points. The display is valid immediately upon removal of the blanking signal.

  Hold – (DTL/TTL Compatible, 2 TTL Loads). Logic "0" or grounding causes the DPM to hold and display the last conversion. Upon removal of the hold, the DPM resumes conversions.

  Decimal Points – (Not TTL Compatible). Logic "0" or grounding turns on appropriate decimal point. External circuitry must sink 35mA when a decimal point is illuminated.
- Outputs

  DTL/TTL Compatible[3] – Status. Logic "1" indicates conversion in process. All digital outputs are valid when status is at logic "0". 4 TTL loads. – Polarity. Logic "1" indicates positive polarity, unlatched. 6 TTL loads. – Overload, Logic "1" indicates overload (⩾40,000), unlatched 4 TTL Loads.

  CMOS and LP Schottky Compatible – BCD outputs, 4¾ BCD digits, character serial, bit parallel, 1 LP Schottky load.

  Parallel BCD Output (Option"B"). – 4¾ BCD digits, positive true, latched. Drives 5 TTL loads. – Data Ready. Logic "1" indicates output data is valid. Drives 2 TTL loads. – Polarity. Logic "1" indicates positive polarity, latched, Drives 2 TTL loads.

  Digit Strobe Outputs – (CMOS or LP Schottky Compatible) Logic "1" on any of these lines indicates the output data is valid for that digit, 1 LP Schottky load.

EXTERNAL POWER SUPPLY OUTPUTS
- AD2025: +5V at 25mA, -25V at 5mA
- AD2028: -25V at 5mA

POWER SUPPLY INPUTS
- AD2025: ac line, 50–60Hz, 4W
- AD2028: 5V dc, ±5% at 800mA

CALIBRATION ADJUSTMENTS
- Gain
- Zero
- Recommended recalibration interval: 6 months

SIZE
- AD2025: 3.92″W x 1.67″H x 4.48″D (100 x 42 x 114mm)
  Panel cutout: 3.930″ x 1.682″ (99.8 x 42.7mm)
- AD2028: 3″W x 1.8″H x 4″D (76 x 46 x 102mm)
  Panel cutout: 3.175″ x 1.810″ (80.65 x 45.97mm)

WEIGHT
- AD2025: 14 ounces (395 grams)
- AD2028: 10 ounces (280 grams)

OPTIONS – ORDERING GUIDE[4]
- AD2025

  AC Power Inputs – No cost option
  AD2025 – 117V ac
  AD2025/E – 220V ac
  AD2025/F – 100V ac
  AD2025/H – 240V ac
  } ±10%

  Input Range Options – No cost option
  AD2025 – ±3.9999V Full Scale
  AD2025/V – ±39.999V Full Scale

  Data Output Options – See pricing guide
  AD2025 – Character serial data outputs
  AD2025/B – Parallel BCD option

  Display Lens Options[5]
  Lens 7 – Red with ADI logo
  Lens 8 – Red without ADI logo

  Connector – 36 pin, 0.156″ spacing, card edge connector, Viking 2VK18D/1-2 or equivalent. – Optional: Order AC2610.

  AD2025/B option also requires a 30 pin, 0.156″ spacing, card edge connector, Viking 2VK15D/1-2 or equivalent. – Optional: Order AC1501.
- AD2028

  Input Range Options – No cost option
  AD2028 – ±3.9999V Full Scale
  AD2028/V – ±39.999V Full Scale

  Data Output Options – See pricing guide
  AD2028 – Character serial data outputs
  AD2028/B – Parallel BCD option

  Display Lens Options[5]
  Lens 5 – Red with ADI logo
  Lens 6 – Red without ADI logo

  Connector – AC1501 (see above) or equivalent. AD2028/B option requires two each.

[1] Guaranteed at +25°C and nominal power supply voltage.
[2] Guaranteed.
[3] For CMOS compatibility, 3.3k pullup resistors to the +5V output of the DPM are required.
[4] Only one AC Power Input and/or Input Range option may be specified. The "B" option can be ordered with any combination of power and range options.
[5] If no lens is specified, Lens 5 or 7 is supplied as appropriate.

Specifications subject to change without notice.

APPLYING THE AD2025 AND AD2028

Wiring Connections

Figures 1 and 2 are wiring diagrams for AD2025 and AD2028 applications. The "limited differential" input uses a 100Ω resistor to isolate the analog input from the digital and power supply sections to prevent ground loop problems. The analog input must be connected between the "analog high" and "analog ground" inputs only, since in some applications there may be up to a ±200mV CMV difference between analog and digital grounds.

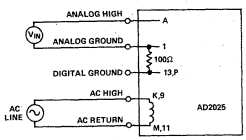


Figure 1. AD2025 Wiring Interconnections

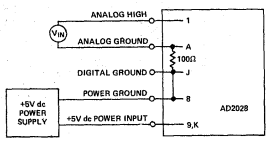


Figure 2. AD2029 Wiring Interconnections

Polarity Indication

No direct polarity indication is provided on the AD2025 or AD2028 although both DPMs measure bipolar inputs. If indication of negative polarity is desired, the "polarity" output can be connected to the far left hand decimal point (DP .XXXXX) provided. When the polarity is negative, this decimal point will then be illuminated.

Interfacing Data Outputs

The standard data outputs are in a bit parallel character serial format compatible to CMOS and LP Schottky logic systems. The BCD outputs are multiplexed, and a digit output is provided for each of the five digits of output. Thus, the four BCD lines on the output at a given time are valid for the digit whose digit line is currently high. The bit parallel character serial data is valid when the DPM status line is low for a period of 150ms between each conversion cycle. The overload line is latched output which is at logic "1", whenever the input exceeds the full 40,000 count range.

Optional parallel BCD outputs ("B" option) are available on a separate card which is internally connected to the DPM. The output data then is presented in a full parallel format and is latched. The parallel data is valid whenever the data ready output is high.

Pin connections for the "B" option are shown in the interconnection tables and a full timing diagram is shown in Figure 3.

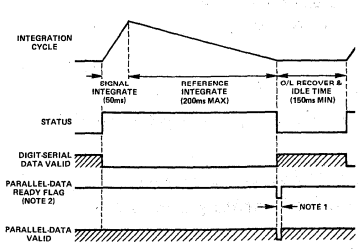


Figure 3. AD2025/AD2028 Timing Diagram

PIN	FUNCTION	PIN	FUNCTION
1	Analog Ground	A	Analog High
2	10^1 Digit	B	10^0 Digit (LSD)
= KEY		= KEY	
3	BCD 2	C	10^2 Digit
4	10^3 Digit	D	BCD 4
5	BCD 8	E	BCD 1
6	Mux Step[1]	F	10^4 Digit (MSD)
7	+5V dc (Out)	H	-25V dc (Out)
8	NC	J	NC
9	AC High	K	AC High
10	NC	L	NC
11	AC Return	M	AC Return
12	NC	N	NC
13	Digital Ground	P	Digital Ground
14	DP .XXXXX	R	Status
15	Polarity	S	Hold
16	Display Blank	T	DPX.XXXX
17	DPXXXX.X	U	DPXX.XXX
18	Overload	V	DPXXX.XX

NOTE 1: BCD multiplexer clock pulse available for remote placement of BCD option.

AD2025 – Signal and Pin Connections

PIN	FUNCTION	PIN	FUNCTION
1	Analog High	A	Analog Ground
2	10^0 Digit (LSD)	B	Mux Step[1]
3	BCD 8	C	BCD 1
4	BCD 2	D	BCD 4
5	10^4 Digit (MSD)	E	10^1 Digit
6	10^3 Digit	F	10^2 Digit
7	NC	H	-25V dc (Out)
8	Power Ground	J	Digital Ground
9	+5V (In)	K	+5V (In)
10	NC	L	NC
= KEY		= KEY	
11	Display Blank	M	DP.XXXXX
12	Hold	N	Polarity
13	Overload	P	Status
14	DPX.XXXX	R	DPXX.XXX
15	DPXXX.XX	S	DPXXXX.X

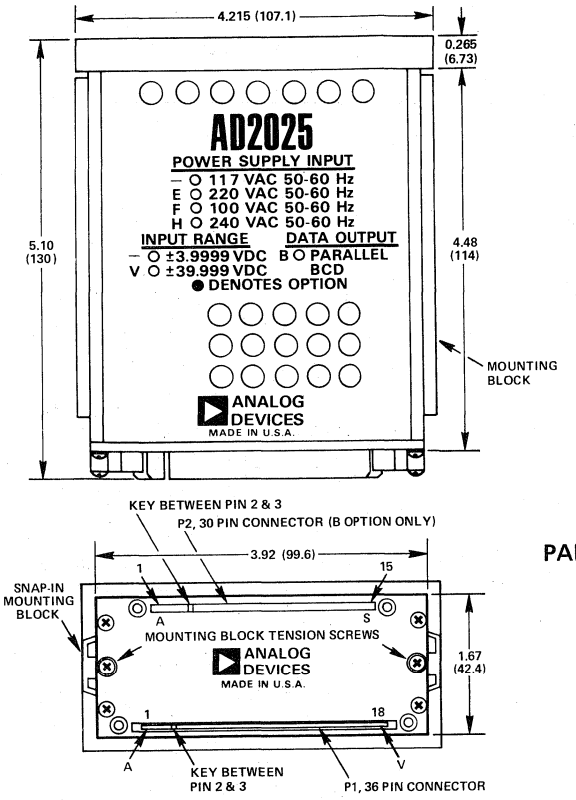
AD2028 – Signal and Pin Connections

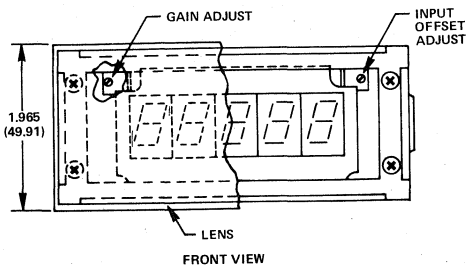
PIN	FUNCTION	PIN	FUNCTION
1	+5V dc (in)	A	BCD 20,000
2	BCD 1 (In)	B	BCD 8 (In)
= KEY		= KEY	
3	BCD 4 (In)	C	BCD 2 (In)
4	BCD 2000	D	BCD 4
5	BCD 40	E	BCD 80
6	BCD 800	F	BCD 8000
7	BCD 100	H	BCD 1000
8	BCD 10,000	J	BCD 200
9	BCD 20	K	BCD 2
10	BCD 8	L	BCD 10
11	BCD 1	M	BCD 4000
12	BCD 400	N	10^4 Digit (In)
13	Data Ready	P	Status (In)
14	Polarity (In)	R	Mux Step (In)
15	Polarity (Out)	S	Digital Ground

NOTES: 1) Overload output is on main DPM connector.
2) Pins marked "In" are made available for remote placement of BCD option card and are not normally used since all connections are internal.

AD2025/AD2028 BCD Options – Signal and Pin Connections

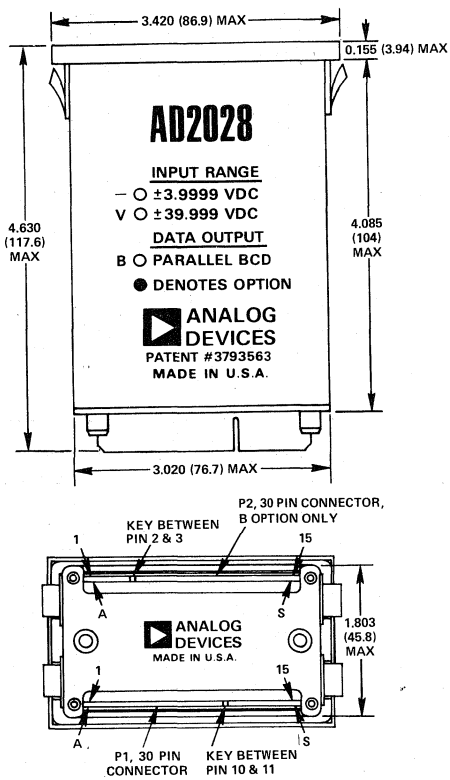
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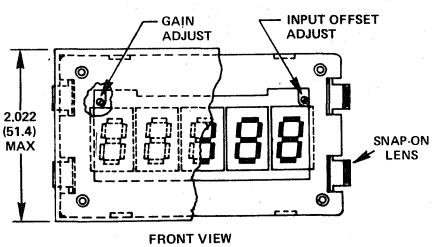




PANEL CUTOUT: 3.930 X 1.682 (99.82 X 42.72)

Figure 4. AD2025 Mechanical Outline (Dimensions shown in inches and (mm))





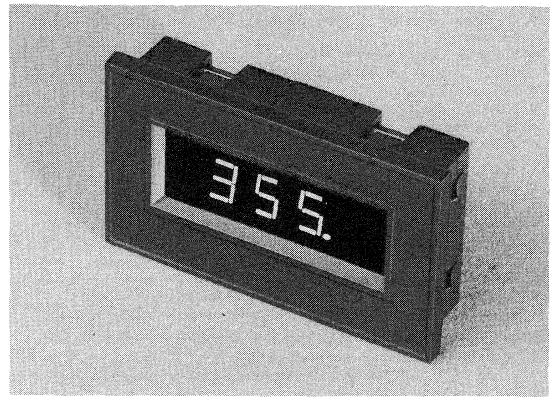
PANEL CUTOUT: 3.175 X 1.810 (80.65 X 45.97)

Figure 5. AD2028 Mechanical Outline (Dimensions shown in inches and (mm))

Low Cost 3 Digit AC Line or Logic Powered DPM

AD2026*

FEATURES
Third Generation I^2L LSI Design
Either Line Powered or Logic Powered
Large 0.56″ Red Orange LEDs
Balanced Differential Input/Floating 1000V, CMV
Terminal Block Interface (ac Version)
High Reliability: > 250,000 Hour MTBF
Small Size and Weight
Low Cost



Optional 10.0V full scale (F.S.) range is available on the ac line version that will accept inputs from –0.99V to 9.99V.

GENERAL DESCRIPTION

The AD2026 is specifically designed to provide a digital alternative to analog panel meters. The AD2026 is available either logic powered (+5V dc) or ac line powered. Most of the analog and digital circuitry is implemented on a single I^2L LSI chip, the AD2020. Only 13 additional components are required to complete the AD2026 +5V dc version. The entire dc version is mounted on a single 3″ X 1 5/8″ PCB. AC line power is achieved with the addition of a second PCB containing the ac power transformer and power supply circuitry.

The AD2026, on both the ac line and logic powered versions, offers as a standard feature, 0.56″ high LED Displays. Brightness is enhanced on both versions due to the Red Orange lens. In addition to the Red Orange lens, the AD2026 is also available with a dark red lens for applications where maximum brightness is not required and minimum backlighting is desired.

A unique patented case design utilizes molded-in fingers, both to capture the PCB in the case and to provide snap-in mounting of the DPM in a standard panel cutout. No mounting hardware of any kind is used. The dc version occupies less than 1″ of space behind the panel. The line powered version offers the same mounting features but occupies 2 1/2″ of behind-panel space.

EXCELLENT PERFORMANCE

The AD2026 offers the instrument designer digital accuracy, resolution and use of readout while occupying less space than its analog counterpart. Other features of analog meters such as reliability and instantaneous response are retained in the AD2026.

The AD2026 measures and displays inputs from –99mV to +999mV, with an accuracy of 0.1% of reading ±1 digit. Zero shift is less than one bit over the full operating temperature range, resulting in the same performance as a DPM with auto zero. The balanced differential input of the dc powered AD2026 rejects common mode voltages up to 200mV, enough to eliminate most ground loop problems. The floating differential input inherent in the ac line powered version offers 1000V of common mode voltage rejection.

***Covered by patent numbers: 4,092,698; 29,992; 3,872,466; and 3,887,863.**

WIRING CONNECTIONS

For Balanced Differential operation with the AD2026 dc version, connect input as shown in Figure 1. The common mode loop must provide a return path for the bias currents internal to the AD2026. The resistance of this path must be less than 100kΩ and total common mode voltages must not exceed 200mV.

For applications where attenuation is required, scaling resistors can be connected between pins 6 and 7 and between pins F and H. Pin 5 must be used as the High Analog Input when scaling resistors are used and pin 4 when they are not. Pin E is the Analog Low Input.

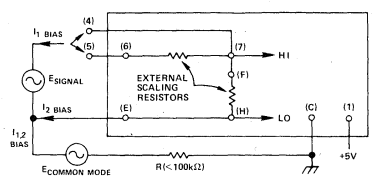


Figure-1.

Connection to the ac line powered AD2026 is via the terminal strip on the rear. AC line power is connected to terminals 4 and 5 and the signal input is connected to terminal 1 (Analog HI) and 2 (Analog Ground).

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SPECIFICATIONS (typical at +25°C and nominal supply voltage unless otherwise noted)

DISPLAY OUTPUT
- Light emitting diode, planar seven segment display readouts, 0.56" (14.6mm) high (orange)
- Overload Indication: EEE
- Negative Indication: -XX
- Negative Overload Indication: ---
- Decimal Points: three (3) selectable at input connector (dc version); internally on ac version

ANALOG INPUT
- Configuration: balanced differential input (dc version) single ended isolated (ac version)
- Full Scale Range: -99mV to +999mV
  -0.99V to +9.99V (10V option on ac version)
- Automatic Polarity
- Input Impedance: 100MΩ; 100kΩ (10V option)
- Bias Current: 100nA
- Overvoltage Production: ±15V dc, sustained

ACCURACY
- ±0.1% ±1 digit[1]
- Resolution: 1mV or 10mV
- Temperature Range[2]: -10°C to +60°C operating; -25°C to +80°C storage
- Temperature Coefficient: Gain: 50ppm/°C
  Zero: 10μV/°C (essentially auto zero)
- Warm-Up Time to Rated Accuracy: Instantaneous
- Settling Time to Rated Accuracy: 0.3 second for full input voltage swing (dc version); 0.75 second for full input voltage swing (ac version)

COMMON MODE REJECTION (1kΩ source imbalance, dc to 1kHz)
- 50dB, ±200mV common mode voltage (dc version)
- 116dB (96dB on 10V range); 1000V rms max CMV (ac version)

NORMAL MODE REJECTION
- 30dB at 50-60Hz (ac version)

CONVERSION RATE
- 4 conversions per second
- Hold and read on command (dc version only)

CONTROL INPUTS

Display Blanking/Display Power Input, (dc version only): The display of the AD2026 can be blanked by removal of power to the display power input, with no effect on conversion circuitry. If external logic switching is used, the display requires 110mA peak (85mA average) when illuminated.

Hold (dc version only): When the Hold input is at Logic "0", grounded or open circuit, the AD2026 will convert at 4 conversions per second. If a voltage of 0.6V to 2.4V is applied to this input, the DPM will stop converting and hold the last reading. A 12kΩ resistor in series with this input to +5V will provide the proper voltage input. (Consult factory for "HOLD" on ac version.)

DECIMAL POINT
- To illuminate decimal points on dc version, ground appropriate pin (A, B or 3).
- To illuminate decimal points on ac version, remove shroud and bridge appropriate solder pad (A, B or 3).

POWER INPUT LOGIC POWER[3]
- Converter: +5V ±5%, 0.2 watts typ; 0.33 watts max
- Display: +5V ±40%, 0.45 watts typ; 0.75 watts max

POWER INPUT AC LINE POWER
- AC line, 50-60Hz, 1.5 watts

CALIBRATION ADJUSTMENTS
- Gain
- Zero
- Recommended recalibration interval: six months

SIZE[4]
- 3.43"W X 2.0"H X 0.85"D (87 X 52 X 22mm)
- 0.88" (22mm) overall depth to rear of connector
- Panel cutout required: 3.175 ±0.015" X 1.810 ±0.015" (80.65 ±0.38 X 45.97 ±0.38mm)

WEIGHT
- 1.8 ounces (53 grams) (dc version)
- 7 ounces (198 grams) (ac version)

CONNECTIONS

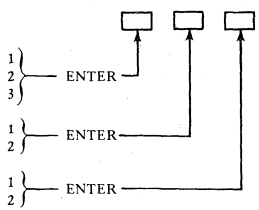
A 10-pin T&B/Ansley 609-1000M with two feet of 10 conductor ribbon cable is available. Order AC2618 (dc version, only).

Conductor to pin A is color coded. Sequence of ribbon connections is A, 1, B, 2, C, 3, etc.

The AD2026 ac version is complete with terminal strip for easy interface.

ORDERING GUIDE

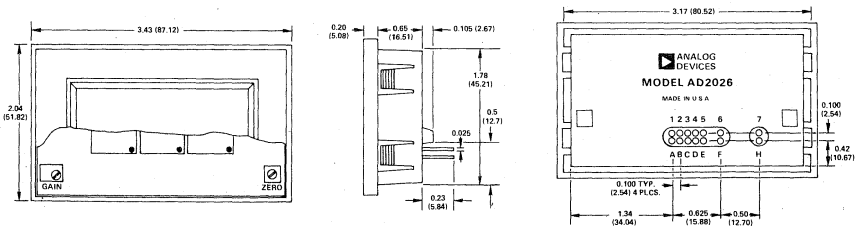
AD2026		
Power Input		
+5V dc	1	ENTER
90-129V ac	2	
198-264V ac	3	
Full Scale Input[5]		
1V dc Full Scale	1	ENTER
10V dc Full Scale[6]	2	
Lens[5]		
Red Lens	1	ENTER
Red Orange Lens	2	



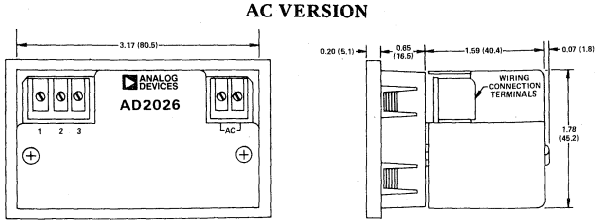
NOTES:
[1] Guaranteed at +25°C and nominal supply voltage.
[2] Guaranteed.
[3] When the same power supply is used to power both display and converter, +5V, ±5%, 0.65 watts typical, 0.9 watts max is required.
[4] Dimensions for ac line powered version: 3.43"W X 2.0"H X 2.44"D (87mm X 52mm X 63mm)
[5] No Charge Options
[6] 10V dc full scale option is available on ac power only
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



AC VERSION



PIN CONNECTIONS

AC VERSION

PIN	FUNCTION
1	Input
2	Analog Ground
3	NC
4	AC HI
5	AC LO

DC VERSION

PIN	FUNCTION
1	+5V Power
2	+5V Display Power
3	Decimal Point X.XX
4	Input (When Scaling Resistors Not Used)
5*	Input (When Scaling Resistors Are Used)
6*	Series Arm of Scaling Resistor Divider
7*	Series Arm of Scaling Resistor Divider

PIN	FUNCTION
A	Decimal Point XX.X
B	Decimal Point XXX.
C	Power Ground
D	Hold
E	Analog Ground
F*	Shunt Arm of Scaling Resistor Divider
H*	Shunt Arm of Scaling Resistor Divider

*NOT NORMALLY USED. ALLOWS CONVENIENT MOUNTING OF SCALING RESISTORS.

ANALOG DEVICES

True rms/dB Multirange Meter

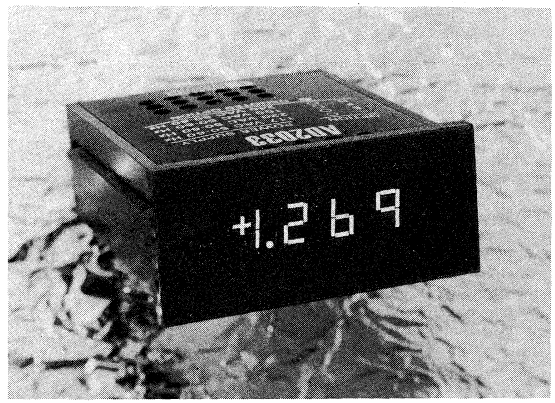
AD2033

FEATURES

- True rms Measurement
- dB Measurements
- Bipolar dc Measurements
- High Accuracy/Wide Frequency Response
- Full Floating Input Isolation
- Parallel BCD Data Outputs
- Five Input Ranges
- 3½ Digits
- Large 0.5" (13mm) LED Displays
- Line Powered
- Industry Standard Case Design

APPLICATIONS

- Accurate True rms Measurement of Complex ac or ac+dc Waveforms
- Decibel Display of ac or ac+dc Inputs
- For Use in Test Equipment, Power Controllers, Process Control Equipment and Analytical and Scientific Instruments



GENERAL DESCRIPTION

The AD2033 is a 3½ digit, LED display, line-powered digital panel meter (DPM) that measures dc and ac input signals. The AD2033 measures either the true rms value of ac+dc signals or the dB value of the ac+dc inputs.

The input of the AD2033 is dc coupled and therefore accepts ac and/or dc inputs. The input can be ac coupled if it is desired to measure an ac signal riding on a constant dc voltage, as in measuring the ripple of a dc power supply.

TRUE rms MEASUREMENTS

Unlike most ac meters which display rms but measure the rectified average of ac input signals, the AD2033 uses implicit computing techniques to derive the actual rms value of the ac signals. Thus, the accuracy of the AD2033 does not depend on input waveforms. Pulse trains, triangular pulses and SCR chopped sinewaves, even with high crest factors (ratio of peak to rms) and pure sinewaves, are all measured with high accuracy and no recalibration over a wide frequency range.

dB MEASUREMENTS

dB measurements can be made with respect to internal or external references (including standard 1mW/600Ω used in audio measurements). In either case, internal or external, the measurements are made with regard to a voltage level from +5mV to +5V. With internal reference, the voltage can be adjusted via a built-in reference adjust pot. dB measurements can also be made against an arbitrary external reference, either constant or slow varying. The external reference is applied to a pin on the top rear connector, and may be divided down from a higher reference voltage.

FIVE INPUT RANGES

The AD2033 provides five separate inputs: 199.9mV; 1.999V; 19.99V; 199.9V and 600V rms Full Scale (FS). 1000V rms FS input is available upon special request. When reading is dB, these input ranges are extended to 500mV, 5V, 50V, 500V and 625V rms.

Factory calibration provides excellent accuracies on all five ranges, but the standard unit is optimized for the 1.999V rms FS range. Optimized calibration for the other ranges is also available. The floating opto-isolated analog input withstands common mode voltages up to 300V rms, even with digital outputs and control lines connected. This not only facilitates making measurements in various electrical environments, but is essential in making current measurements which are rarely referenced directly to ground.

SECOND GENERATION DPM DESIGN

The use of MOS/LSI (Metal Oxide Semiconductor/Large Scale Integration) integrated circuits in the AD2033 reduces the number of components, cuts power consumption and greatly increases reliability.

For detailed information, contact factory.

SPECIFICATIONS (typical at +25°C and nominal power supply voltages)

DISPLAY OUTPUT
- Light emitting diode (LED), seven segment display readouts, 0.5" (13mm) high for 3 data digits, 100% overrange and polarity indication. Overload indicated by flashing display.
- Decimal points (3) selectable at input connector.
- Display Blanking

SIGNAL INPUT
- Type: Single ended, floating, dc coupled
- Full Scale Ranges: MAX V rms INPUT

Range	With rms Readout[1]	With dB Readout
A	199.9mV	500mV
B	1.999V	5V
C	19.99V	50V
D	199.9V	500V
E	600V (See Note 2)	625V (See Note 2)

- Voltage x Frequency Limit: 10^7 V Hz
- Input Impedance: 1MΩ||10pF for all ranges except 200mV (100kΩ|| 10pF)
- Bias Current[3]: 1nA on all ranges except 200mV (10nA)
- Overvoltage Protection: 625V rms sustained on all ranges except 200mV FS (120V rms)
- Common Mode Voltage: 300V rms max at 60Hz
- Common Mode Rejection at 60Hz:

F.S. Input	CMR
A	100dB
B	80dB
C	75dB
D	60dB
E	40dB

- Temperature Range: Operating 0 to +50°C; Storage -25°C to +85°C
- Settling Time to Rated Accuracy: 2 seconds
- Provisions for external capacitor to extend low frequency response (reference applications section)
- Warm-Up Time: 20 minutes to rated accuracy

CONVERSION RATE
- 5 conversions per second
- Hold and read on command

CONTROL INPUTS

Display Blanking (TTL/DTL Compatible, 1 TTL Load) - Logic "0" or grounding blanks entire display except for decimal points; Logic "1" or open circuit for normal operation. Display blanking has no effect on output data. Display is valid immediately upon removal of blanking input.

Converter Hold (CMOS/TTL/DTL Compatible, 1 LPTTL Load) - Logic "0" or grounding causes DPM to cease conversions and display data from last conversion; Logic "1" or open circuit for normal operation. After "Converter Hold" is removed, one or two conversions are needed before reading and BCD data are valid.

Decimal Points (Not TTL Compatible) - Logic "0" or grounding illuminates desired decimal point. External drive circuitry must sink 25mA peak at a 25% duty cycle, when decimal point is illuminated.

Data Hold (TTL/DTL Compatible, 1 TTL Load) - Logic "0" or grounding inhibits updating of latched parallel output data; Logic "1" or open circuit allows data to be updated after each DPM conversion. This input has no effect on the normal conversion of the DPM and its display.

DATA OUTPUTS

Isolated Parallel BCD Outputs - 3 BCD digits, Overrange, Overload and Data Ready Outputs (TTL compatible, 4 TTL Loads). BCD Data Outputs are latched, positive true logic. Overload output is Logic "0" for inputs greater than full scale range, Logic"1" when other data outputs are valid. Polarity Output (TTL Compatible, 4 TTL Loads Latched) indicates positive polarity when high (Logic "1"). Digital Outputs are fully isolated from input circuitry; all logic levels are referenced to digital ground.

rms MEASUREMENTS
- Accuracy: See Table 1 (accuracy guaranteed)
- Inputs: 199mV; 1.999V; 19.99V, 199.9V; 600V rms FS
- Temperature Coefficient: See Table 1
- Frequency Response: See Table 1
- Resolution: 0.05% of FS (3½ digits)
- Crest Factor: 1% error at C.F. = 4 at ½ FS
  4% error at C.F. = 9 (max) at ½ FS
  1% error at C.F. = 4 at FS

dB MEASUREMENTS
- Accuracy: See Figure 3 (accuracy guaranteed)
- Readout Resolution: 0.1dB
- Input: 500mV; 5V; 50V; 500V; 625V rms FS
- Temperature Coefficient: ±0.01dB/°C typical
- Reference Voltage Span: +5mV dc to +5V dc (internal adjustable or external)
- Signal Voltage Span: See Figure 3
- V_{REF} Input Resistance: 24.9kΩ ±1%
- V_{REF} Bias Current: 40nA typical; 500nA max

BIPOLAR DC MEASUREMENTS
- Full Scale Input: ±1.999V dc (See AD2022 Data Sheet for complete information)

POWER INPUT
- AC line 50–400Hz
- Power Consumption: 6.8 watts at 60Hz

CALIBRATION ADJUSTMENTS
- Input Offset
- Zero Width
- Gain
- Internal (dB) Reference Adjust
- Recommended Calibration Interval: 6 months

SIZE
- 3.92"W x 1.67"H x 4.48"D (100 x 42 x 114mm)
- Panel Cutout: 3.924" x 1.682" (99.8 x 42.7mm)

WEIGHT
- 17 ounces (485 grams)

OPTIONS
- AC Power Inputs (no cost option) (50–400Hz)
  AD2033 – 117V ac
  AD2033/E – 220V ac
  AD2033/F – 100V ac
  AD2033/H – 240V ac
  } ±10%
- Display Lens Options[4]
  Lens 7 – Red with ADI Logo
  Lens 8 – Red without ADI Logo
- AD2033 Converter Card Connector P1
  30 pin, 0.156" spacing card edge connector, Viking 2VK150/1-2
  Optional: Order AC1501
- AD2033 rms/dB Card Connector P2
  36 pin, 0.156" spacing card edge connector, Viking 2VK18D/1-2
  Optional: Order AC2610

[1] Overrange of 250% of full scale is available for analog only output (pin R) on all ranges except E. For E overrange capability is 4%.
[2] 1000V is optional, contact factory.
[3] Bias Current approximately doubles for each change in ambient temperature of +10°C.
[4] Lens 7 is supplied if no lens option is specified.

Specifications subject to change without notice.

Range	199.9mV rms	1.999V rms	19.99V rms	199.9V rms	600V rms
Accuracy	±1.2% RDG	±0.1% RDG	±0.3% RDG	±0.3% RDG	±1.2% RDG
DC or 30Hz to	±0.05% FS	±0.05% FS	±0.05% FS	±0.05% FS	±0.05% FS
3kHz Sinewave	±1 digit	±1 digit	±1 digit	±1 digit	±1 digit
Temperature Coefficient:					
Zero	±20μV/°C	±60μV/°C	±0.6mV/°C	±6mV/°C	±60mV/°C
Gain	±75ppm/°C	±75ppm/°C	±75ppm/°C	±75ppm/°C	±75ppm/°C
Frequency Response: (Sinewave Input)					
±1% RDG ±0.05% FS ±1 digit (max error)	30Hz to 10kHz	30Hz to 10kHz	30Hz to 10kHz	30Hz to 10kHz	30Hz to 5kHz
3dB (max error)	30Hz to 100kHz	30Hz to 100kHz	30Hz to 100kHz	30Hz to 100kHz	30Hz to 30kHz

Table 1. AD2033 rms Specifications

APPLYING THE AD2033

Description Of Operation

The timing and block diagrams are shown in Figures 1 and 2 respectively. The input pin for all ranges except range A is Pin K. Range A input connects to Pin E. The input signal is fed into a buffer amplifier. Range selection is made by connecting the appropriate feedback resistor. The Bias Current Compensate (Pin B), for stabilization of bias current over extended temperatures, should be tied to ground on all

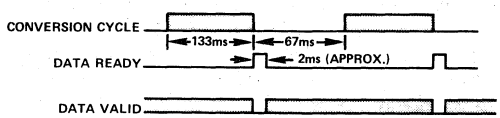


Figure 1. AD2033 Timing Diagram

ranges except Range B. The output of the buffer amplifier drives a True rms to dc converter that combines logarithmic and implicit computing techniques to achieve low overall error and a wide dynamic range, as in the equation:

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T (V_{IN})^2\ dt}$$

For True rms readout, the above is used as the A/D input. It also drives the log ratio circuitry which develops a dB output relative to either internal or external reference voltage. For dB readout, the log ratio output feeds the A/D input.

The A/D conversion is performed via a special technique ("Charge Balancing") that requires interaction between analog and digital processing. The analog processor provides buffering, integration, autozeroing and comparison functions. The digital processor contains control, counting, storage and data multiplexing functions. As can be seen from the block diagram, the two processors are opto and pulse transformer isolated. This isolation increases DPM tolerance to front end noise and high common mode voltage. The output of the digital processor drives the display via a seven segment decoder driver and is also available via the parallel BCD data storage.

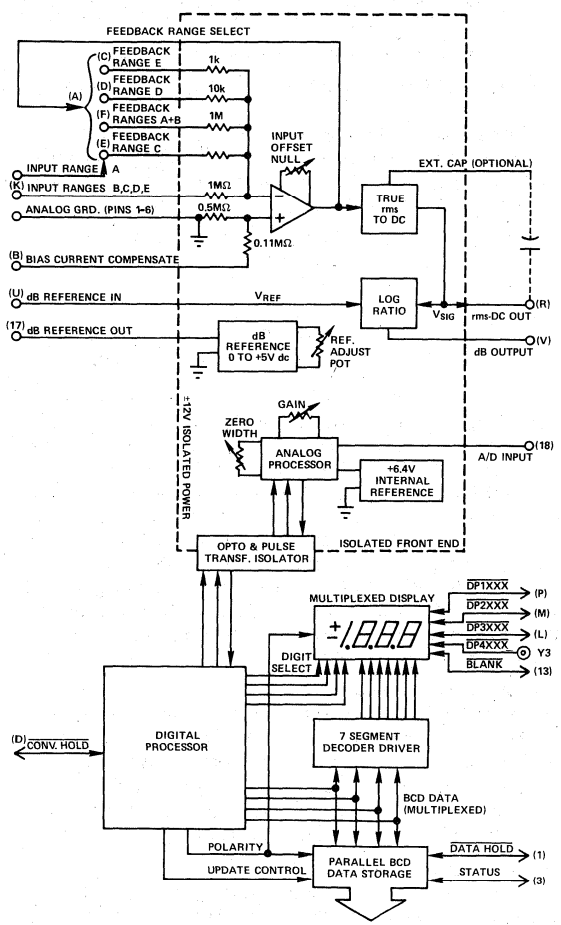


Figure 2. AD2033 Block Diagram

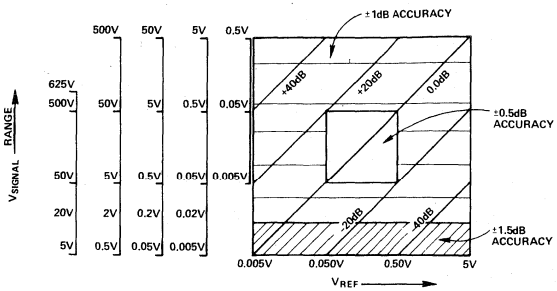
True rms Measurements

A typical setup for measuring 1.999V rms FS (Range B) can be accomplished by linking Feedback Range Select (Pin A) to Feedback (Pin F). Connect 1.999V source between Input (Pin K) and Ground (Pins 1-6). Then connect rms/dc fashion in setting up for all other ranges except when using the 199.9mV rms FS range where Pin K *must* be grounded and the input must go to Pin E. The Bias Current Compensate (Pin B) must be connected to Ground on all ranges except the 1.999V rms FS.

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dB Measurements

As shown in Figure 3, dB readout for a particular V_{SIG} can be varied by controlling V_{REF}, either via the Internal Reference Adjust or by control of an external reference (which can can be divided down from a higher voltage).



NOTE: FIGURE 3 IS SET UP FOR ABSOLUTE VOLTAGES ON THE 5V SCALE. 20dB CORRECTION PER DECADE WOULD BE NEEDED IF V_{REF} REMAINS ABSOLUTE ON OTHER RANGES.

CAUTION: THERE IS NO INPUT OVERLOAD INDICATION IN dB MODE.

Figure 3. dB Readout as a Function of V_{SIG} and V_{REF}

Adjustment of the dB range can also be accomplished by selecting the proper V_{SIG} input range and V_{REF}. The 60dB readout range can be offset anywhere within the total meter range of +60dB to -60dB.

Examples: 1. V_{SIG} = 50V rms on the 50V rms range with V_{REF} = 5V. dB readout = 0.00dB and the full dB readout range is 0.00dB to -60dB.
2. V_{SIG} = 50V rms on the 500V rms range with V_{REF} = 0.5V. dB readout = 0.00dB and the full dB readout range is +20dB to -40dB.

To set up for a full scale of 500mV input range, link Feedback Range Select (Pin A) to Feedback (Pin F). Connect source between 200mV Input (Pin E) and Ground (Pins 1-6). Connect dB Reference In (Pin U) to dB Reference Out (Pin 17) for use of internal reference and then link dB Output (Pin V) to A/D Input (Pin 18). To use external reference, connect source between dB Reference In (Pin U) and Analog Ground (Pins 1-6). Since the input pin for this range is Pin E, the Input Pin (Pin K) for all other ranges must be grounded and the Bias Current Compensate must be linked to Ground (Pins 1-6) on all ranges except the 1.999V rms FS Range. Set up in similar fashion on other ranges.

Bipolar dc Measurements

By bypassing the rms/dB front end, it is possible to use the AD2033 to measure and display a bipolar dc value on the 1.999V FS. The input pin for this measurement would be the A/D Input Pin (Pin 18 of P2). Connect low side to Ground (Pins 1-6). A shunt capacitor (0.047μF) at the A/D Input is needed to limit input impedance.

Ac Coupling Input of AD2033

For measurements of ac voltages superimposed upon dc voltage, put the following dc blocking capacitors at DPM input:

Range	Capacitor (Rated Accuracy at 45Hz)
200mV	1μF
All Others	0.1μF

Measurement of Very Low Frequencies

If the input signal to be measured has a frequency of dc to about 30Hz, the AD2033 will "track" the input signal and the constantly changing readout may be difficult to read. To extend the low frequency response of the AD2033, two pins are provided at the connector of P2 to allow an external capacitor to be attached. Table 2 will aid in choosing the proper value of averaging capacitance.

Frequency	Averaging Capacitor Value	Settling Time to Rated Accuracy
25Hz	15μF	6 Seconds
10Hz	100μF	30 Seconds

Table 2. External Capacitor Selection

Interfacing Data Outputs - Parallel BCD

The AD2033 has data outputs in a full parallel BCD format. The output data is latched and is valid except for a 2ms period at the end of conversion, when the "Data Ready" output is high (See Figure 1). As described above, the "Data Hold" input can be used to inhibit updating of the parallel data outputs without affecting DPM conversions or the DPM display.

Extended True rms ac Range Measurements

Although the full scale display range of the AD2033 is 1999 counts, and the display flashes to indicate overrange beyond this point, measurements are actually made up to approximately 3000 counts. Since it is impossible to display "2" in the most significant digit of the AD2033, overrange from 2000 to 2999 counts produces a flashing display of the 3 least significant digits only (a reading of 2.300mV displays as "300" flashing). Overrange beyond 2999 counts is indicated by a constant number flashing. Thus, one can use the extra range measurements as a guide to reducing the input to the normal range. The parallel BCD outputs of the AD2033 beyond 1999 counts go to Logic "0" on all BCD lines, as does the Overload Output.

KEY

PIN	FUNCTION
1	DATA HOLD
2	
3	DATA READY
4	POLARITY
5	BCD 8
6	BCD 2
7	BCD 80
8	BCD 20
9	BCD 800
10	
11	BCD 400
12	BCD 200
13	DISPLAY BLANK
14	OVERRANGE
15	ac LINE HIGH

KEY

PIN	FUNCTION
A	N/C
B	N/C
C	OVERLOAD
D	CONVERTER HOLD
E	BCD 1
F	BCD 4
H	BCD 10
J	BCD 40
K	BCD 100
L	DP3 XX.X
M	DP2 X.XX
N	DIGITAL GROUND
P	DP1 .XXX
R	SHIELD (EARTH GROUND)
S	ac LINE LOW

Figure 4. AD2033 Connector P1

KEY

PIN	FUNCTION
1	ANALOG LOW
2	ANALOG LOW
3	ANALOG LOW
4	ANALOG LOW
5	ANALOG LOW
6	ANALOG LOW
7	
8	
9	
10	
11	
12	
13	
14	
15	
16	
17	dB REF OUT (0 TO +5V)
18	A/D INPUT ±1.999V FS

KEY

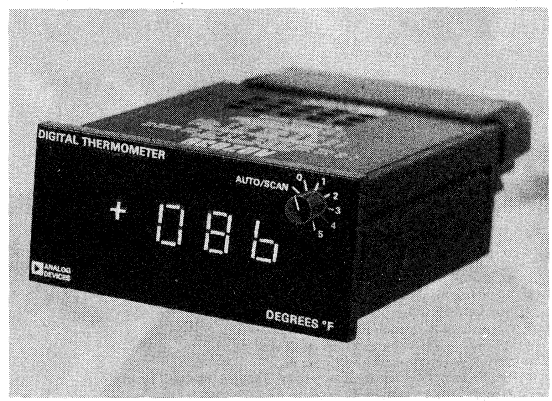
PIN	FUNCTION
A	RANGE SELECT (CONNECT TO C,D,E,F)
B	BIAS CURRENT COMPENSATE
C	RANGE E FEEDBACK
D	RANGE D FEEDBACK
E	RANGE C
F	RANGE A AND B
H	
J	
K	INPUT (EXCEPT 200mV)
L	
M	
N	
R	rms OUT ±1.999V FS/EXT CAP (+)
S	EXT CAP (-)
T	dB REF IN (OPTIONAL)
U	dB REF IN (+5mV ≤ V_{REF} ≤ +5V)
V	dB OUT (200mV/DECADE)

Figure 5. AD2033 Connector P2

ANALOG DEVICES

6 Channel Scanning Digital Thermometer

AD2036



FEATURES

Automatic/Manual Scan of 6 Thermocouples (TCs)
External Channel Selection by BCD Code
J, K, or T Thermocouple
°C or °F Readout
Self-Contained Linearization
Isolated Analog Input
Parallel BCD Output
1° Resolution, 0.1° Optional
AC Line or dc Powered
+5V dc at 10mA for External Logic

APPLICATIONS

Multi-Point Temperature Measurements for Remote Data Acquisition and Data Logging
Temperature Monitoring in Design, Laboratory, Manufacturing and Quality Control

GENERAL DESCRIPTION

The AD2036 is a low cost 3½ digit, ac line or dc powered digital readout temperature meter. Inputs for six thermocouples of identical types, either J, K, or T and calibrated temperature ranges in °C or °F, make up a total of six available models.

Cycling on an internal clock, the AD2036 can continually scan 6 input channels. Individual channels can be manually selected via a small switch on the front. Channel selection can also be made via an external BCD input at the rear connector. A separate channel select output identifies the selected channel independent of selection mode. The channel select output together with the BCD Output provides complete information for automatic data collection. The Isolated Parallel BCD Output provides an easy interface to conventional recording and controlling instruments. For applications where there are high common mode voltages (CMV) present, the AD2036 has as a standard feature a floating opto isolated analog front end that will withstand CMV's up to 250V rms.

The AD2036 displays readings on large 0.5″ (13mm) high LED displays. Both (+) and (–) polarities are indicated. Controls are provided for blanking the display.

AUTO/SCAN

The AD2036, while in the Auto/Scan mode, will permit unattended scanning of all six input channels. The rate of the channel select is 3.2 seconds, 1.6 seconds or 0.8 seconds. The AD2036 can be used as a stand-alone instrument and with the Scan input held high will continually scan six channels. When the Scan input is brought low the AD2036 will continue to cycle and stop at channel 0. When used with a printer the channel select number in addition to the converted BCD value can be recorded.

MANUAL CHANNEL SELECTION

A switch on the front enables the user to manually select an individual thermocouple. As in the Auto/Scan mode, the BCD Output of the selected channel and the channel number are available. Selection of an individual TC channel automatically disables Scan and external channel selection is overridden. The Mode Output pin indicates when the switch is in this condition. On special order, meters can be supplied with card edge control for disabling the switch.

EXTERNAL CHANNEL SELECTION

For remote control of channel selection the AD2036 provides an input for an external BCD code selection. This feature enables external BCD switch, automatic microprocessor or computer control.

STANDARD PACKAGING

The AD2036 is packaged in Analog Devices' ac line powered DPM case which uses the same panel cutout as most other ac line powered DPM's from other manufacturers. In addition, the pin connections for the AD2036 converter board are the same as for the AD2022, AD2009, AD2016 and DPM's available from several other manufacturers.

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For detailed information, contact factory.

SPECIFICATIONS (typical @ +25°C and nominal line voltage unless otherwise specified)

TYPES OF THERMOCOUPLE (TCs): J, K, or T

ACCURACY[1]

°C		Error ±½LSB	°F		Error ±½LSB
J	-60 to 0	±1.4	J	-76 to 32	±2.5
	0 to 500	±1.4		32 to 932	±2.5
	500 to 760	±2.2		932 to 1400	±4.0
K	-60 to 0	±1.4	K	-76 to 32	±2.5
	0 to 150	±1.4		32 to 302	±2.5
	150 to 1350	±2.6		302 to 2000	±4.7
T	-100 to 0	±1.3	T	-148 to 32	±2.3
	0 to 250	±1.5		32 to 450	±2.7
	250 to 400	±2.0		450 to 752	±3.6

DISPLAY OUTPUT
- Light emitting diode (LED), seven segment display readouts, 0.5" (13mm) high for 3 data digits, 100% overrange and polarity indication. Overload >1999 indicated by flashing display, polarity remains valid. There is no overload indication for out of range readings.
- Decimal points (3) selectable at input connector.
- Display Blanking

SIGNAL INPUT
- Input Impedance: 100MΩ
- Bias Current: 10nA
- Overvoltage Protection Between Channels: ±18V peak max
- Common Mode Voltage: ±350V peak max
- CMV Between Channels: ±6V peak max
- Temperature Coefficient: Span: +temp, 100ppm; -temp, 120ppm Zero: 0.03degrees/degree C or F
- Settling Time to Rated Accuracy: 2.0 seconds (full span step input)
- Normal Mode Rejection: 60dB at 50 – 400Hz
- Common Mode Rejection: 120dB @ 250V rms max CMV (Between TC's and digital gnd), $dv_{cm}/dt < 10^6$ V/sec, 250Ω imbalance

CONVERSION RATE
- 5 conversions per second
- Hold and read on command

CONTROL INPUTS

Display Blanking (TTL Compatible, 3 LSTTL Load) - Logic "0" or grounding blanks entire display except for decimal points; Logic "1" or open circuit for normal operation. Display blanking has no effect on output data. Display is valid immediately upon removal of blanking input.

Converter Hold (CMOS, TTL Compatible, 1 LSTTL Load) - Logic "0" or grounding causes DPM to cease conversions and display data from last conversion; Logic "1" or open circuit for normal operation. After "Converter Hold" is removed, one or two conversions are needed before reading and BCD are valid.

Decimal Points (Not TTL Compatible) - Logic "0" or grounding illuminates desired decimal point. External drive circuitry must sink 35mA peak at a 25% duty cycle, when decimal point is illuminated.

Data Hold (TTL Compatible, 1 TTL Load) - Logic "0" or grounding inhibits updating of latched parallel output data of AD2036. Logic "1" or open circuit allows data to be updated after each DPM conversion. This input has no effect on the normal conversion of the DPM and its display.

Scanner Enable (CMOS/TTL Compatible 1 LSTTL Load) - Logic "1" will enable Scanner to control the channel selection. External channel input BCD lines can remain connected. A Logic "0" enables external channel selection.

Scan (Scan) (CMOS/TTL Compatible, 1 LSTTL Load) - A Logic "1" ("0") for <4 seconds will initiate a scan of six channels. To use Scan input, the Scan input must be a Logic "0". Both inputs have debounce circuitry. A momentary scan pulse while in the switch or external selection mode will initiate a sequence of six readings of the channel that is addressed then stop.

Channel BCD Input (CMOS/TTL Compatible 1 LSTTL Load) - Logic "0" on Scanner Enable will allow use of external control. All other control inputs remain the same.

Channel Increment (CMOS/TTL Compatible 1 LSTTL Load) - Positive going edge will initiate sequence to the next channel.

Spare Inverter Input (CMOS, TTL Compatible 1 LSTTL Load) - Spare inverter supplied for customer convenience.

DATA OUTPUTS

Isolated Parallel BCD Outputs - 3 BCD digits, Overrange, Overload and Data Ready Outputs (TTL Compatible, 4 TTL Loads). BCD data outputs are latched positive true logic. Overrange Output is Logic "1" for data display greater than 999. Overload Output is Logic "0" for inputs greater than full scale range, Logic "1" when other data outputs are valid. Polarity Output (TTL Compatible, 4 TTL Loads latched) indicates positive polarity when high (Logic "1"). Digital outputs are fully isolated from input circuitry; all logic levels are referenced to digital ground.

Channel BCD Outputs (CMOS/TTL Compatible 2 TTL Loads) - BCD Channel number data outputs are positive true.

Mode Output (CMOS/TTL Compatible 2 TTL Loads) - Logic "1" indicates channel selection is by switch. Logic "0" indicates selection is by scanner or external control, useful in microcomputer interface.

Data Ready (Data Ready) (CMOS/TTL Compatible 2 TTL Loads) - Logic "1" ("0") indicates data from Temperature Card is ready. Data remains valid until next clock pulse (198ms).

Spare Inverter Output (CMOS/TTL Compatible 2 TTL Loads) - Spare inverter supplied for customer convenience.

Clock OUT (CMOS, TTL Compatible, 2 TTL Loads) - Indicates E.O.C. When Clock pulse is high latches are being updated, data is invalid. Data is valid on negative going edge. Clock OUT pulse is disabled when DATA HOLD line is low.

Analog Output - Nonlinear Error ±0.5% ±1mV
V_{OUT}, °C = (1.784mV/°C) Temperature
V_{OUT}, °F = (0.991mV/°F)(T-32)

TEMPERATURE RANGE[2]
- 0 to +50°C Operating
- -25°C to +85°C Storage

POWER OUTPUT
- +5V dc @ 10mA

POWER INPUT
- AC line 50 – 400Hz, See Voltage Options below
- Power Consumption - 5.8W @ 50 – 400Hz
- 12V dc +20% - 10%, 4.8W
- 5V dc ± 5%, 4W

CALIBRATION ADJUSTMENTS
- Span
- Zero
- Recommended Recalibration Interval: six months

SIZE
- 3.92" x 1.67"H x 5.80"D (100 x 42 x 147mm)
- Panel cutout 3.930" x 1.682" (99.8 x 42.7mm)

WEIGHT
- 1.25 pounds (0.568 kg)

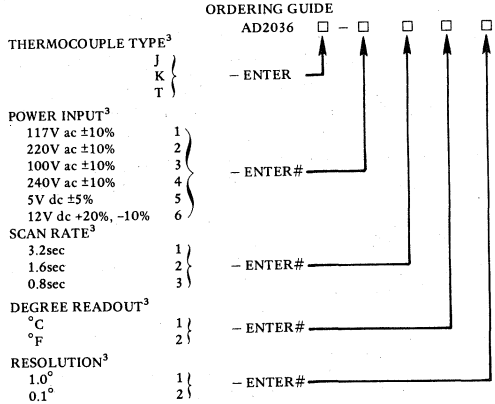
DISPLAY LENS[4]

Lens 22-1: Red, °C with ADI Logo
Lens 22-2: Red, °F with ADI Logo
Lens 23-1: Red, °C without ADI Logo
Lens 23-2: Red, °F without ADI Logo

CONNECTORS(2)

2 each, 30 pin, 0.156" spacing card edge connector
Viking 2VK15D/1-2 or equivalent.
Optional: Order AC1501.

ORDERING GUIDE



NOTES
[1] For 0.1° resolution accuracy remains the same. Range is limited to 200.0°.
[3] Guaranteed
[3] Only one option may be specified.
[4] Lens 22 is supplied if no lens option is specified.

Specifications subject to change without notice.

6 Channel Scanning Digital Voltmeter/ Thermometer

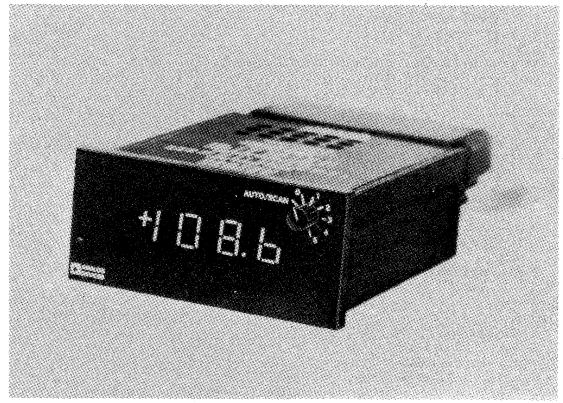
AD2037/AD2038

FEATURES

Automatic Scan of 6 Channel Inputs
Manual Selection of Individual Channel
External Channel Selection by BCD Code
±199.9mV or ±1.999V dc Full Scale Range
Isolated Analog Input
Parallel BCD Output
Accessible Gain Points for Implementation of Selectable Gain, to 6V dc F.S.
±12V dc and +5V dc for External Use
AD2038: High Accuracy Temperature Measurements Used with AD590/AC2626 Transducer/Probe
0.1° Resolution; 6 Channels
-55.0°C to +150.0°C (-67.0°F to +199.9°F)

APPLICATIONS

AD2037: Multi-point Measurements for Data Acquisition, Logging and Control
Data Processing from: Pressure and Flow Transducers; RTD and Thermistor Transducers; AD590 Temperature Transducers; LVDT and Level Transducers; Voltage and Current Sources.
AD2038: Temperature Monitoring in Laboratory, Manufacturing, and Quality Control



AD2037 GENERAL DESCRIPTION

The AD2037 is a low-cost 3 1/2 digit, ac line powered, 6 channel digital scanning voltmeter designed to interface to printers, computers, serial data transmitters, telephone lines, etc., for display, control, logging or transmission of multi-channel analog data. With appropriate external signal conditioning on each channel, the AD2037 becomes a versatile building block for a broad range of data acquisition, data logging, or control applications.

Channel selection is made via three methods: manual, using the switch provided on the front; Auto/Scan, where the AD2037 cycling on an internal clock can continually scan the 6 input channels; or External selection, where control inputs provided on the rear connector enables channel selection via external BCD code.

A separate channel select output identifies the selected channel independent of selection mode. The channel select output together with converted BCD output provides complete information for automatic data collection. For applications where there are high common mode voltages (CMV) present, the AD2037 has as a standard feature, a floating opto isolated analog front end that will withstand CMV's up to 250V rms. The ±199.9mV full scale range or ±1.999V dc full scale range are user selectable via a jumper on the rear connector. Other full scale ranges, to 6V dc, are programmable, via one (1) external resistor.

For detailed information, contact factory.

AD2038 GENERAL DESCRIPTION

The AD2038 is a dedicated 6 channel digital scanning thermometer. Based on the AD2037 and designed to be used in conjunction with Analog Devices' AD590 Temperature Transducer or Analog Devices' AC2626 Temperature Probe, the AD2038 retains all of the input/output features of the AD2037 as well as the channel selection methods.

The AD2038 and AD590/AC2626 will measure and display temperatures to ±1.3°C accuracy over the temperature range of -55.0°C to +150.0°C (-67.0°F to 200.0°F), over limited temperature ranges around a calibration point, accuracies approach a few tenths of a degree.

The AD590 is a laser trimmed, two terminal IC Temperature Sensor. Its output is a current (1μA per °K) linearly proportional to absolute temperature thus eliminating the need for linearization and cold junction compensation.

Due to the AD590's high impedance current output, it is insensitive to voltage drops over long lines thus enabling remote monitoring with no need for costly transmitters or special wire.

For normal applications the AD590J can be used and calibrated at a single temperature point. Where better linearity or sensor interchangeability is needed, the "K" and "L" versions are available. All versions are available to MIL-STD-883A Class B processing. In addition, the AC2626 (an AD590JF mounted in a 3/16 inch diameter, by 6 inch long stainless steel probe) is available. The probe is supplied with 3 feet of wire for easy interface to the AD2038.

SPECIFICATIONS (typical @ +25°C and nominal power supply voltage)

DISPLAY OUTPUT
- Light emitting diode (LED), seven segment display readouts, 0.5" (13mm) high for 3 data digits, 100% overrange and polarity indication. Overload indicated by flashing display, polarity remains valid. There is no indication of out of sensor range on AD2038.
- Decimal Points (3) Selectable at Input Connector
- Display Blanking
- Sensor Disconnect Indication same as overload.

ANALOG INPUT
- Opto/Transformer Isolated
- Configuration: Differential, isolated
- ±1.999V dc and ±199.9mV dc Full Scale Range
- Full Scale Range Programmable to 6V dc
- Input Impedance: 250MΩ
- Bias Current: 1.5nA
- Overvoltage Protection: (Continuous Without Damage)
  Normal Mode: ±30V pk
  Channel to Channel: ±30V pk

ACCURACY
AD2037
- ±0.05% Reading ±1 digit[1]
- Resolution: Programmable
- Temperature Range: 0 to +50°C operating; -25°C to +85°C storage
- Temperature Coefficient: Gain: 50ppm/°C
  Zero: 1.5μV/°C
- Warm-up Time to Rated Accuracy: Less than 5 minutes
- Settling Time to Rated Accuracy: 0.6 seconds (- full scale to + full scale)
- Max Voltage Between Channels: ±199.9mV FS; ±6.1V pk
  ±1.999V FS; ±2.5V pk

ACCURACY
AD2038
- Resolution 0.1°
- Range -55°C to +150°C
  -67°F to +200°F
- Accuracy: (±0.1° digitizing error)[2]

	AD590J	AD590K	AD590L
Sensor calibrated at +25°C (over range)	±2.2°C max	±1.2°C max	±1.2°C max
Uncalibrated Error at +25°C	±5.2°C max	±2.2°C max	±1.2°C max
Uncalibrated Error (over range)	±9.2°C max	±4.0°C max	±2.6°C max
Nonlinearity (over range)	±2.0°C max	±0.5°C max	±0.5°C max

- Temperature Coefficient: Span: 50ppm/°C
  Offset: 0.01 degrees/degree

NORMAL MODE REJECTION
- 50dB at 50 - 60Hz (Additional capacitor filtering may be added between pins A and 4 with degradation of response time)

COMMON MODE REJECTION
- Floated on Power Supply: 120dB at 250V rms max CMV, dV_{cm}/dt 10^6 V/sec max, 1kΩ Imbalance

CONVERSION RATE
- 5 Conversion/sec
- Hold and Read on Command

POWER INPUT
- AC Line 50 - 400Hz, see Voltage Options Below
- Power Consumption - 5.8W @ 50 - 400Hz

ANALOG OUTPUTS
- ±12V dc ±10% @ 10mA (Referenced to Isolation Analog Grd.)
- +5V dc ±5% @ 30mA
- Reference Voltage +6.4V ±1% (Referred to Analog Grd.) 25ppm/°C @ 50μA max output

DATA OUTPUTS

Isolated Parallel BCD Outputs - 3 BCD digits, overrange, overload outputs (TTL Compatible, 4 TTL Loads). BCD data outputs are latched positive true logic. Overrange output is Logic "1" for data display greater than 999. Overload output is Logic "0" for inputs greater than full scale range, Logic "1" when other data outputs are valid. Polarity output (TTL compatible, 4 TTL Loads latched) indicates positive polarity when high (Logic "1"). Digital outputs are fully isolated from input circuitry; all Logic levels reference to digital ground.

Channel Address Outputs (CMOS/TTL Compatible 2 TTL Loads) - BCD Channel number data outputs are positive true.

Mode Output (CMOS/TTL Compatible 2 TTL Loads) - Logic "1" indicates channel selection is by switch. Logic "0" indicates selection is by scanner or external control, useful in Microcomputer Interface.

Data Ready (Data Ready) CMOS/TTL Compatible 2 TTL Loads) - Logic "1" ("0") indicates data from Scan Card is ready. Data remains valid until next clock pulse.

Spare Inverter Output (CMOS/TTL Compatible 2 TTL Loads) - Spare inverter supplied for customer convenience.

Clock Out (CMOS/TTL Compatible, 2 TTL Loads) - Indicates EOC. When clock pulse is high, latches are being updated, data is invalid. Data is valid on negative going edge for 198ms. Clock Out pulse is disabled when Data Hold line is low.

ANALOG OUTPUT (P2 Pin A): 1mA max output

AD2037: $V_O = K V_{IN}$
Where K is gain of programmable input amplifier. (K = 1 for 1.999V F.S. and K = 10 for 199.9mV)

AD2038: $V_O = (18.95mV/°C)T$ for T = °C
$V_O = (10.53mV/°F)(T-32)$ for T = °F
error = ±6mV

Notes:
[1] Guaranteed at 200mV full scale at +25°C and nominal power supply.
[2] Overall accuracy of meter plus sensor over entire sensor range (guaranteed max) Meter is factory calibrated for ideal sensor.
[3] Lens 22 (AD2038) Lens 28 (AD2037) supplied if no lens option is specificed.
[4] Only one option may be specified.
[5] Options not listed are no charge.

Specifications subject to change without notice.

CONTROL INPUTS

Display Blanking (TTL Compatible, 3 LSTTL Load) - Logic "0" or grounding blanks entire display except for decimal points; Logic "1" or open circuit for normal operation. Display blanking has no effect on output data. Display is valid immediately upon removal of blanking input.

Converter Hold (CMOS/TTL Compatible, 1 LSTTL Load) - Logic "0" or grounding causes DPM to cease conversions and display data from last conversion; Logic "1" or open circuit for normal operation. After "Converter Hold" is removed, one or two conversions are needed before reading and BCD are valid.

Decimal Points (Not TTL Compatible) - Logic "0" or grounding illuminates desired decimal point. External drive circuitry must sink 35mA peak at a 25% duty cycle, when decimal point is illuminated.

Data Hold (TTL Compatible, 1 TTL Load) - Logic "0" inhibits updating of latched parallel output data. Logic "1" or open circuit allows data to be updated after each DPM conversion. This input has no effect on normal conversion of the DPM and its display.

Scanner Enable (CMOS/TTL Compatible 1 LSTTL Load) - Logic "1" will enable Scanner to control the channel selection. External channel input BCD lines can remain connected. A Logic "0" enables external channel selection.

Scan (Scan)(CMOS/TTL Compatible; 1 LSTTL Load) - A Logic "1" ("0") for <4 seconds will initiate a scan of six channels. To use Scan input, the Scan input must be a Logic "0". Both inputs have debounce circuitry. A momentary scan pulse while in the switch or external mode will initiate a sequence of six readings of the channel that is addressed then stop.

Channel Address Input (CMOS/TTL Compatible 1 LSTTL Load) - Logic "0" on Scanner Enable will allow use of external control. All other control inputs remain the same.

Channel Address Increment (CMOS/TTL Compatible 1 LSTTL Load) - Positive going edge will initiate sequence to the next channel.

Spare Inverter Input (CMOS/TTL Compatible 1 LSTTL Load) - Spare inverter supplied for customer convenience.

CALIBRATION ADJUSTMENTS
- Gain
- Offset, Course
- Offset, Fine
- Span/per Channel (AD2038 only)
- Recommended Recalibration Interval: Six Months

SIZE
- 3.92" x 1.67"H x 5.80"D (100 x 42 x 147mm)
- Panel Cutout 3.930" x 1.682" (99.8 x 42.7mm)

WEIGHT
- 1.25 pounds (0.563 kg)

OPTIONS[3]

AD2037 Lens: 28 Red with ADI Logo
Lens: 27 Red without ADI Logo

AD2038 Lens 22-1, Red °C with ADI Logo
Lens 22-2, Red °F with ADI Logo
Lens 23-1, Red °C without ADI Logo
Lens 23-2, Red °F without ADI Logo

CONNECTORS (2)
2 each, 30 pin, 0.156" Spacing Card Edge Connector
Viking 2Vk 15/1-2 or Equivalent
Optional: Order AC1501 at $5.00 each

ORDERING GUIDE

AD2037 or AD2038 -

POWER INPUT[4]
117V ac ±10% 1
220V ac ±10% 2
100V ac ±10% 3
240V ac ±10% 4
Enter

SCAN RATE[4]
3.2 sec 1
1.6 sec 2
0.8 sec 3
Enter

TEMPERATURE SCALE READOUT (AD2038 Only)[4]
°C 1
°F 2
Enter

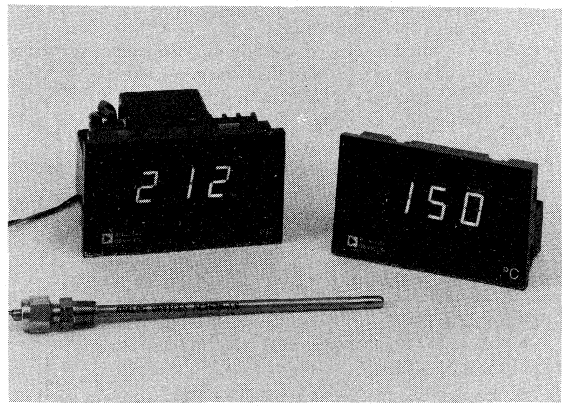
ANALOG DEVICES

Low Cost Temperature Indicator

AD2040

FEATURES
- Low Cost
- Direct Interface to AD590 or AC2626 Sensors
- Large 0.56″ Red Orange LED Display
- Accuracy to ±1.0° ±1 Digit
- Either ac Line or +5V dc Powered
- Temperature Range: -55°C to +150°C
  -67°F to +302°F
- 1000V rms Isolation (ac)
- Terminal Block Interface
- Small Size, Panel Mount

APPLICATIONS
- Temperature Monitoring in Design, Laboratory, Manufacturing and Quality Control for Both +5V dc or Line Powered Applications



GENERAL DESCRIPTION

The AD2040 is a low-cost 3 digit temperature indicator. Based on the highly successful AD2026 low-cost DPM and designed to be used in conjunction with Analog Devices' AC2626 general purpose probe or the AD590 temperature transducer, the AD2040 is available in both 5V logic-powered, or ac line-powered versions.

The 5V powered AD2040-12 reads out directly in °C, °F, °R or K. A precision voltage reference, resistor network, and span and zero adjusts, needed to implement display of the different temperature scales, are all self-contained. User selectable degree readout, as well as all other connections, i.e., +5V power and sensor or probe interface, are all made via a terminal block on the rear.

For many stand-alone temperature measurement applications, i.e., in factories, labs, ovens, inspection stations, etc., +5V dc power is not available. For these applications, the AD2040 is available in an ac version. The ac-powered version retains all of the features of the 5V version, with the exception of the user selectable degree readout. °C or °F must be specified when ordering (see Ordering Guide).

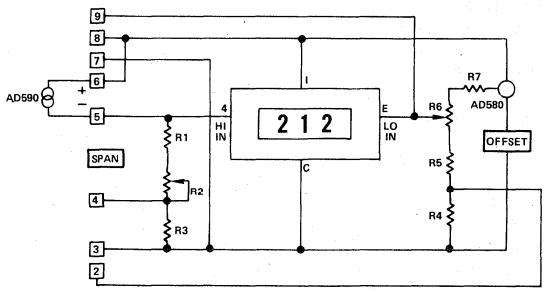
If required, calibration adjustments are easily accessible. No mounting hardware of any kind is used.

The AD2040 and AC2626 or AD590 will measure and display temperatures on large 0.56″ orange LED displays from -55°C to +150°C (-67°F to +302°F) with accuracy to ±1.0° ±1 digit. Reliability is assured with the inherent simplicity and accuracy of the sensor, combined with the highly efficient design of the AD2040.

THE SENSOR

The AD590 is a laser-calibrated, two terminal IC temperature transducer. Its output is a current (1μA per K) linearly proportional to absolute temperature, thus eliminating the need for costly linearization and cold junction compensation.

Due to the AD590's high impedance current output, it is insensitive to voltage drops over long lines thus enabling remote monitoring with no need for costly transmitters or special wire.



AD2040-12 (dc) Block Diagram

Above is a block diagram of the AD2040-12, showing the AD2026 DPM input, the current-to-voltage conversion resistors (R1, R2, R3), the offsetting resistance network (R4, R5, R6, R7), and the connections to the terminal strip. Attenuated voltage from the AD580, 2.5V reference, provides the offsets for readout on the °F and °C scales. On the AD2040-12 dc version, jumpers are connected by the user at the terminal strip to select the appropriate units of temperature for display. °C or °F must be specified when ordering the ac version (see Ordering Guide).

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SPECIFICATIONS (typical @ +25°C and nominal supply unless otherwise specified)

ACCURACY

- Resolution: 1°
- Range: −55°C to +150°C
  −67°F to 302°F
  218K to 423K
  425°R to 793°R
- Accuracy: (±1 digit)[1]

	AC2626J/ AD590J	AC2626K/ AD590K	AC2626L/ AD590L
Calibration Error @ +25°C	±5.0°C max	±2.5°C max	±1.0°C max
Absolute Error (overrated performance temperature range)	±10.0°C max	±5.5°C max	±3.0°C max
Without External Calibration Adjustment	±3.0°C	±2.0°C max	±1.6°C max
With +25°C Calibration Error Set to Zero	±1.5°C	±0.8°C max	±0.4°C max
Nonlinearity			

- Temperature Coefficient:
  Offset: 0.03 degrees/degree
  Span: 70ppm/°C
- Common Mode Rejection (ac)
  117dB, 1000V rms max Common Mode Voltage
- Normal Mode Rejection
  30dB @ 50-60Hz

DISPLAY OUTPUT[2]

- 7 Segment, Red Orange, LED 0.56" (13mm) High for 3 Data Digits
- Sensor Disconnect Indication: ––– (for °C and °F only)
- DPM Positive Overload: EEE
- DPM Negative Overload: –––
- No Indication of Out of Sensor Range

INPUT IMPEDANCE

- °C, K: 1.0KΩ
- °F, °C: 1.8KΩ

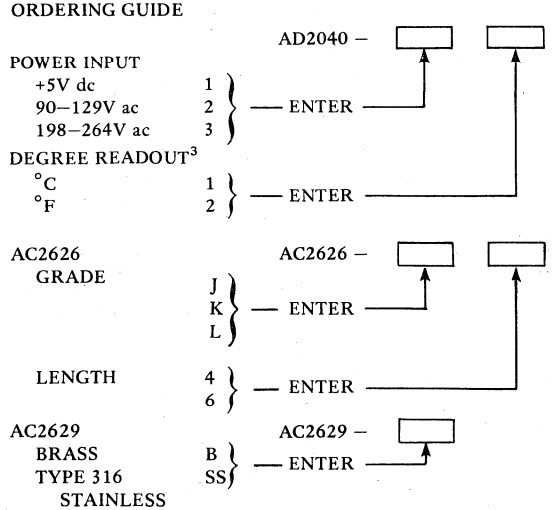
CONVERSION RATE

- 4 Conversions Per Second

POWER INPUT

- +5.0V ±5%; 160mA (dc version)
- AC Line 50-400Hz; See Voltage Options Below

ORDERING GUIDE



POWER INPUT (ac Line Power)

- AC Line Power, 50-60Hz, 1.5 Watts

CALIBRATION ADJUSTMENTS

- Span
- Gain
- Zero
- Offset
- Recommended Recalibration Interval: Six Months

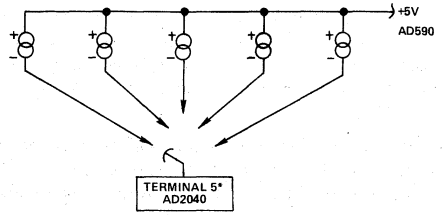
SIZE

- 3.43"W X 2.0"H X 1.65"D (87 X 52 X 42mm)
- Panel Cutout Required: 3.175 ±0.015" X 1.810 ±0.015" (80.65 ±0.38 X 45.97 ±0.38mm)

WEIGHT

- 3 ounces (88 grams) (+5V dc)
- 7 ounces (198 grams) (ac Line Powered)

NOTES:
[1] Overall accuracy of meter plus sensor over entire range.
[2] Leading zero cannot be blanked.
[3] Select Degree Readout when ordering ac version only. (+5V dc version offers user selectable temperature scales—see Table 1. For +5V dc version enter 2, e.g., AD2040-12.)
Specifications subject to change without notice.

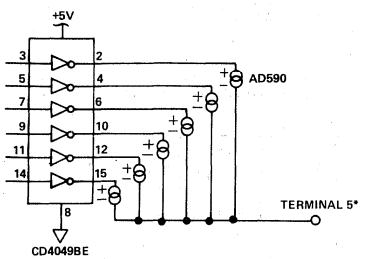


*TERMINAL 5 IS -SENSOR INPUT ON THE +5V DC VERSION.
THIS TERMINAL IS TERMINAL #2 ON THE AC VERSION.

Figure 1. Manual Switching with Multiple Inputs

MULTIPLE SENSOR INPUTS

Expansion to multiple sensors via manual switching is shown in Figure 1. The sensor selected will pass a signal current through the current measuring circuitry, internal to the AD2040. Similarly automatic switching, shown in Figure 2 is accomplished. A low level input on an inverter input will allow selection of the appropriate AD590.



*TERMINAL 5 IS -SENSOR INPUT ON THE +5V DC VERSION.
THIS TERMINAL IS TERMINAL #2 ON THE AC VERSION.

Figure 2. Automatic Switching

SCALE	TERMINAL 2	TERMINAL 3	TERMINAL 4	TERMINAL 9
°C	X	X	X	
°F				
K		X	X	X
°R		X		X

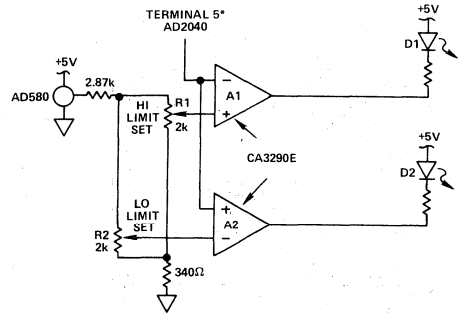
Table 1. Temperature Scale Selection (+5V dc Only)

TEMPERATURE SCALE SELECTION

As shown in Table 1 any of the standard temperature scales may be displayed using the +5V dc AD2040-12.

The AD2040-12dc version is factory calibrated in degrees Fahrenheit. Readout in degrees Celsius, Rankine or Kelvin are achieved via simple jumper connections on the terminal block, listed in the above table. (Connect terminals marked X.)

Figure 3 shows how the AD2040, in conjunction with 4 resistors, 2 trim pots, and a dual comparator, can be used to control as well as monitor particular applications via high and low set points. When the voltage at the AD2040 sense terminal (terminal 5) goes higher than the Hi Limit Set Voltage, the



*TERMINAL 5 IS -SENSOR INPUT ON THE +5V DC VERSION.
THIS TERMINAL IS TERMINAL #2 ON THE AC VERSION.

Figure 3. Hi and Low Set Points

output of A1 goes low and D1 is illuminated. Similarly when the voltage at terminal 5 goes below the Lo Limit Set Voltage, the output of A2 goes low illuminating D2.

To set the high limit, replace the AD590 with a variable resistor. Adjust the resistor until the desired high temperature set point is displayed on the meter. Adjust R1 until D1 is just turning on. Repeat procedure for R2 (Lo Limit Set).

CALIBRATION PROCEDURE

The AD2040 is factory calibrated using an ideal sensor. The dc version is calibrated in °F and the ac version is calibrated to order. If sensor accuracy is adequate, no calibration is required (see note). If a lower grade sensor is used (i.e., J) and calibration is required, adjust Span Adjust on the rear with sensor at a known temperature for that temperature, e.g. for °F place sensor in Ice Bath at 32°F and adjust span for reading of 32.

Recalibration may be required after six (6) months; if so, proceed as follows:

1. With AD590 disconnected, short input of AD2040 (terminal 5 to 9 on dc version, or 2 to 3 on ac version). Remove AD2040 lens and adjust Front Panel ZERO Adjust to display 000.
2. Attach AD590 sensor and stabilize at a known Reference Temperature; e.g., Ice Bath. Connect terminal 9 to terminal 3 (on dc version) or terminal 3 to access port (on ac version) and adjust Rear SPAN Adjust for a display of 273 plus Reference Temperature for °C or 460 plus Reference Temperature for °F.
3. Remove jumper between terminals 9 and 3 (dc version) or 3 and access port (ac version). Adjust the Rear OFFSET Adjust for Reference Temperature. (For K or °R omit step 3.)

For optimum linearity calibration for °C, repeat steps two (2) and three (3) with Reference Temperature at 0. Then with sensor at 100°C adjust Front Panel GAIN Adjust for a meter display of 100. Other high end temperatures may be used with this procedure as long as they are known to be accurate.

For °F repeat steps two and three with Reference Temperature at 32°F. Then with sensor at the high temperature, adjust Front Panel GAIN Adjust for readout equal to high temperature. The above temperature can be selected for optimum linearity over user's temperature range.

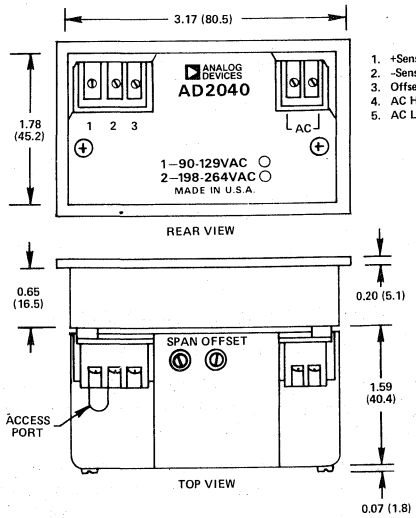
NOTE: If other than °F readout on the dc version is desired, follow step 2 and 3 of Recalibration Procedure.

16

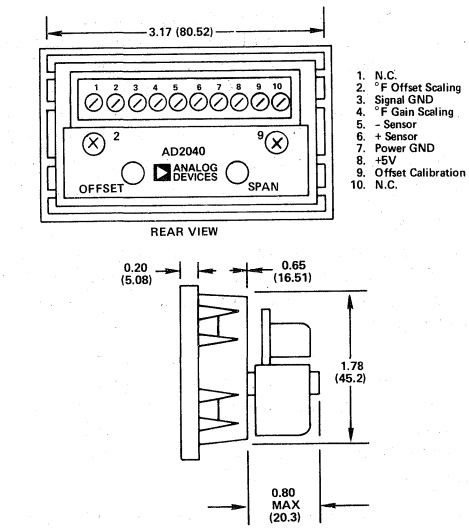
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

AD2040 (ac)



AD2040 (dc)



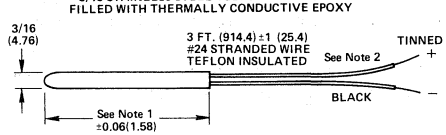
THE AC2626

The AC2626 is a stainless steel tubular probe measuring 3/16 inch (4.76mm) in outside diameter and is available in 6 inch (152.4mm) or 4 inch (101.6mm) lengths. Based on the new AD590F, the probe is available in linearity grades of 0.4°C, 0.8°C or 1.5°C.

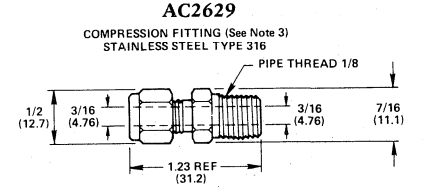
The probe is designed for both liquid and gaseous immersion applications as well as temperature measurements in refrigeration or any general temperature monitoring application.

For taking measurements in pipes or other closed vessels, the AD2629 compression fitting is available. The AC2629 may be applied anywhere along the probe and is supplied in two materials. The low cost AC2629B is constructed of brass and the higher priced AC2629SS is made of stainless steel.

AC2626



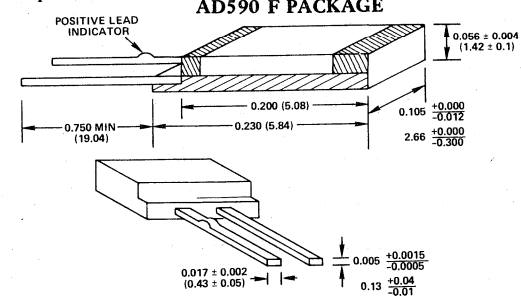
AC2629



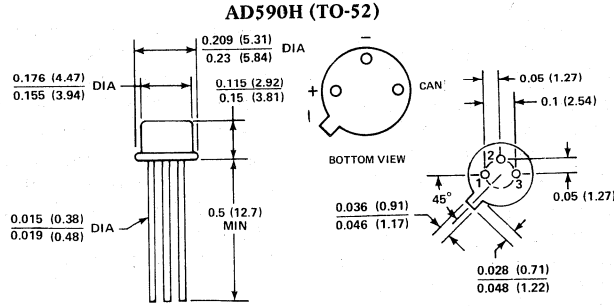
NOTES
1. PROBES ARE AVAILABLE IN 4-INCH OR 6-INCH LENGTHS.
2. + LEAD WIRE IS COLOR CODED: J, YELLOW; K, ORANGE; L, BLUE.
3. WHEN ASSEMBLING COMPRESSION FITTING (AC2629) TO PROBE, TIGHTEN THE 1/2" NUT 3/4'S OF A TURN FROM FINGER TIGHT.

The AD590 temperature transducer is available in two packages–the "H" package (TO-52) and the "F" package (ceramic flat pack).

AD590 F PACKAGE



AD590H (TO-52)



Microprocessor Based Thermocouple Meters

AD2050/AD2051

FEATURES

- Automatic Self-Calibration for Gain, Offset, Cold Junction Compensation and Thermocouple Linearization
- J, K, T, E, R, S Thermocouple Selections (AD2050) Universal Meter (AD2051), User Programmable
- Character Serial ASCII Digital Output
- Optional Linearized Analog Output: 1mV/degree
- Optional Isolated 20mA Loop Serial Output
- Meets DIN/NEMA Dimension Specifications
- Temperature Ranges: −265°F to +1999°F
  −165°C to +1760°C
- Power Options: 120V ac, 240V ac, +7.5V dc to +15V dc

APPLICATIONS

- Temperature Monitoring in Laboratory, Manufacturing, and Quality Control Environments
- Process Control Temperature Measurements
- Remote Data Logging



GENERAL DESCRIPTION

The AD2050 and AD2051 are high performance single channel 3½ digit thermocouple meters that can measure temperatures accurately between −265 and +1999 in degrees Celsius or Fahrenheit. The AD2050 is supplied factory programmed to interface directly with any of the following six thermocouple types: J, K, T, E, R and S. The AD2051 is a universal instrument in which the user selects one of the six thermocouple types via switch programming. Being microprocessor based, all gain and offset error correction, cold junction compensation, thermocouple linearization, and °C/°F scaling are automatically performed in firmware.

The AD2050 and AD2051 display temperature information on large 0.56″ (14.3mm) high LEDs. Digital information is provided in standard ASCII character serial format with rate selection for easy interface to printers, terminals, and other peripherals. For remote data acquisition applications, an optional isolated 20mA serial loop interface is available. Also an optional analog output linearized to 1mV/degree is provided for driving recorders and other analog instruments. Selection of °C or °F scaling is accessed by removing the front panel lens and connecting two terminals together with a jumper wire.

The AD2050 and AD2051 can also be ordered with any of the following power versions: 120V ac, 240V ac, or +7.5V dc to +15V dc. Input over voltage protection for 300V peak (thermocouple to ac line shorts) and common mode voltages as high as 1400V peak (ac version) with overrange and open thermocouple detection are provided. These instruments are rated for operation over the +10°C to +40°C temperature range. Testing is performed per MIL-STD-202E Method 103B to insure specified operation during various relative humidity conditions. The AD2050 and AD2051 are supplied in rugged high impact plastic cases that meet DIN/NEMA standard dimensions.

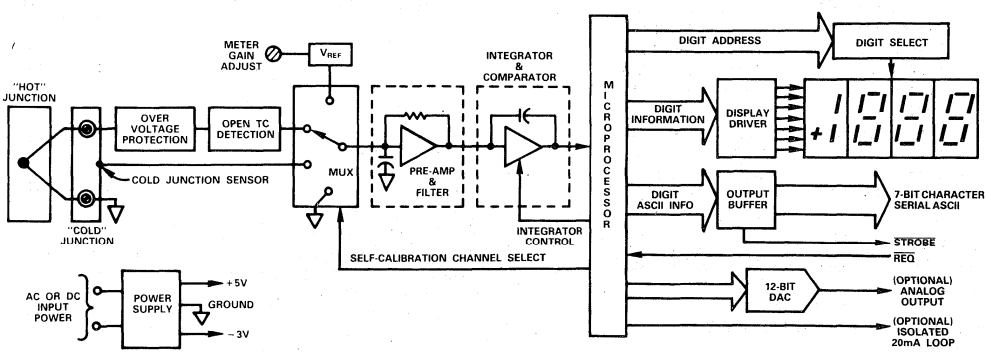


Figure 1. AD2050 & AD2051 Functional Block Diagram

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SPECIFICATIONS (typical @ +25°C and rated supply voltages unless otherwise specified)

THERMOCOUPLE INPUTS
- Thermocouple Types: J, K, T, E, S, R
- Input Impedance: >100MΩ
- External (Lead) Resistance Effect: <20μV per 350Ω of Lead Resistance
- Cold Junction Compensation Error: ±0.5°C max (10°C to +40°C)
- Open Thermocouple: +EEE Display; +EEEE ASCII Digital Output; +2.048V Analog Output
- Thermocouple Short to ac Line: Internal Protection Provided to 300V peak (200V ac rms)
- Common Mode Voltage: 1400V peak (dc or ac), between Input and Power Line Ground (ac Versions)
- Common Mode Rejection Ratio: >130dB with 250Ω Source Imbalance (ac Versions); (dc to 60Hz)
- Normal Mode Rejection Ratio: >80dB @ 50/60Hz

DIGITAL OUTPUTS
- Data: Character Serial ASCII
  Drive Capability: 2TTL Loads, CMOS/TTL Compatible
- $\overline{\text{Strobe}}$: Negative transition determines when character serial data is valid. CMOS/TTL compatible.
- Overrange: ±EEEE
- Character Rate: Selectable on J1 (pin 32)
  Grounded: 25 characters/sec. (slow)
  Open: 100 characters/sec. (fast)
- Minimum Time Between New Data Update: 150ms

DIGITAL INPUTS
- $\overline{\text{REQ}}$: Low-Level Triggered; must go low at any time other than during data transmission to be recognized. $\overline{\text{REQ}}$ line taken low during data transmission will not be acknowledged and the ASCII digital output transmission will not occur. Display readings are not effected by $\overline{\text{REQ}}$.

ANALOG OUTPUT (OPTIONAL)
- Voltage: 1mV/degree, linearized
- Current: ±2mA max drive
- CMV: 1400V peak (ac or dc) Peak between Analog Output Ground & ac Power Line Ground
- Overrange: +2.048V, −0.512V

ACCURACY
- Temperature Resolution: 1°C/1°F
- All Ranges are Guaranteed Monotonic
- Range Temperature Coefficient: ±25ppm/°C typ, ±60ppm/°C max
- Readout Accuracy @ 25°C:

Sensor Type	Range	Accuracy	
J	−165°C to 760°C	±0.7°C	±1/2LSD
J	−265°F to 1400°F	±1.3°F	±1/2LSD
K	−50°C to 1250°C	±0.9°C	±1/2LSD
K	−58°F to 1999°F	±1.6°F	±1/2LSD
T	−150°C to 400°C	±0.8°C	±1/2LSD
T	−238°F to 752°F	±1.4°F	±1/2LSD
E	−100°C to 870°C	±1.0°C	±1/2LSD
E	−148°F to 1598°F	±2.0°F	±1/2LSD
S	+300°C to 1760°C	±1.5°C	±1/2LSD
	0° to 299°C	±6.0°C	±1/2LSD
S	+572°F to 1999°F	±3.0°F	±1/2LSD
	+32°F to 571°F	±12.0°F	±1/2LSD

ANALOG TO DIGITAL CONVERSION
- Technique: Offset Dual Slope with Gain and Offset Error Correction
- Rate: 2.5 Conversions/Second Typical
- Input Integration Period: 100ms for 50/60Hz Noise Rejection

POWER REQUIREMENTS (Choice of Three Supply Ranges)
- ac: 90V ac to 132V ac @ 25mA (47Hz to 500Hz)
  198V ac to 264V ac @ 12.5mA (47Hz to 500Hz)
- dc: +7.5V to +15V dc @ 200mA (Protected Against Supply Reversals)

DISPLAY
- Type: Seven Segment Orange LED 0.56" (14.3mm) high
- Polarity Indication: "+" or "−" displayed
- Overrange Indication: ±EEE
- Display Test: At Power Turn-On, 3 Second Display of "+1888" Tests all Segments of Display

ENVIRONMENTAL
- Rated Temperature Range: +10°C to +40°C
- Operating Temperature Range: −10°C to +50°C
- Storage Temperature Range: −40°C to +85°C
- Relative Humidity: Meets MIL-STD-202E, Method 103B

DIMENSIONS
- Case: 3.78" × 1.89" × 5.13" (96.8mm × 48.9mm × 131.3mm), high impact molded plastic case. DIN/NEMA Standard
- Weight: 15.2 oz (431 grams) max, ac powered
  12.0 oz (341 grams) max, dc powered.

RELIABILITY
- Burn In: 168 Hours at +50°C and Power ON/OFF Cycles.
- Calibration: NBS Traceable
- Recalibration: Recommended 15-Month Intervals
- Warranty: 12 months

CONNECTOR
One 44 pin 0.1" (2.54mm) spacing card edge connector
Viking 3VH22/1 JN5 or equivalent
Optional: Order AC2630

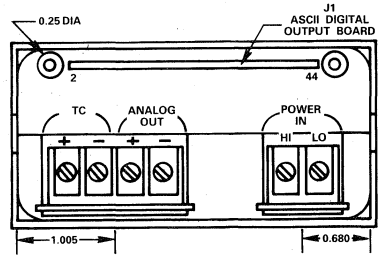
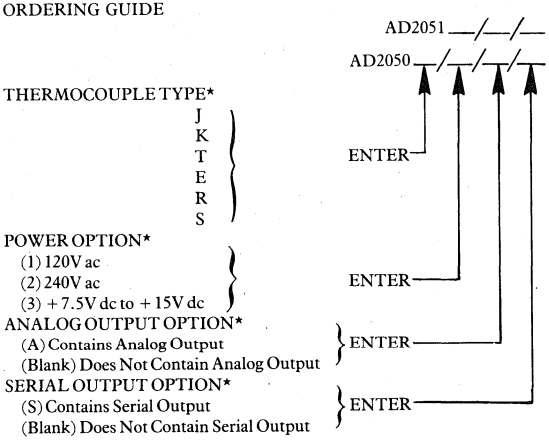


Figure 2. Rear Panel View

ORDERING GUIDE



*Only one option can be ordered. The thermocouple type does not need to be specified when ordering the AD2051 since it is user programmable.

Specifications subject to change without notice.

Microcomputer Analog I/O Subsystems

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•New product since *1980 Data-Acquisition Components and Subsystems Catalog*

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Selection Guide
Microcomputer Analog I/O Subsystems

Analog Devices Real-Time Interface (RTI) products provide a direct memory-mapped interface between popular microcomputers and analog input and output signals. Each RTI board is electrically and mechanically compatible with the bus it is designed to interface with. No additional interface logic or power are required for the board, which plugs directly into the microcomputer card cage.

As the Selection Guide indicates, there are Input-only, Output-only, and—in most cases—Input/Output cards available for each bus type. Within each card family, there are optional features available to provide a close fit to the individual user's application.

The Selection Guide provides selection information in capsule form, permitting card types to be matched to desired features. Additional information and complete specifications are provided on the individual card or family data sheets.

		MICROCOMPUTER BUS COMPATIBILITY									
		INTEL NATIONAL MULTIBUS™						PRO-LOG MOSTEK STD BUS			
		RTI-1200-001	RTI-1200-004	RTI-1200-011	RTI-1200-014	RTI-1201	RTI-1202	RTI-1225	RTI-1226	RTI-1260	RTI-1262
Board Type	Input	•		•			•		•	•	
	Input/Output		•		•			•			
	Output					•					•
Channel Capacity	Input (Single ended/ differential)	16/8	16/8	32/16	32/16		16/8	16/8	16/8	32/16	
	Output		2		2	4		2			4
Input Resolution	10 Bits							•	•		
	12 Bits	•	•	•	•		•			•	
Output Resolution	8 Bits							•			
	12 Bits		•		•	•					•
Additional Features											
DC/DC Converter		•	•	•	•	•	•	•	•	•	•
Software PGA											
Gains of 1, 2, 4, 8V/V		•	•	•	•						
Resistor PGA											
Gains of 1 to 1000V/V							•			•	
4-20mA Output			•		•	•					•
Digital Output Drivers		•	•	•	•	•					
Volume II Page		17-5	17-5	17-5	17-5	17-7	17-9	17-11	17-11	17-19	17-19

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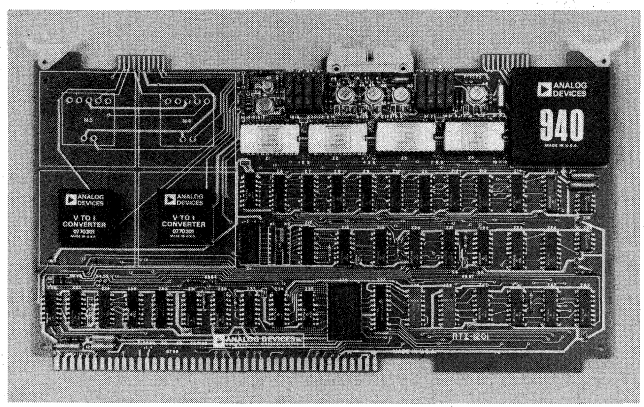
		MICROCOMPUTER BUS COMPATIBILITY									
		MOTOROLA MICROMODULE BUS				TEXAS INSTRUMENT TM990 BUS			DEC LSI BUS		
		RTI-1230	RTI-1231	RTI-1232	RTI-1240	RTI-1241	RTI-1242	RTI-1243	RTI-1250	RTI-1251	RTI-1252
Board Type	Input	•			•				•		
	Input/Output		•			•				•	
	Output			•			•	•			•
Channel Capacity	Input (Single ended/ differential)	32/16	32/16		32/16	32/16			32/16	16/8	
	Output		2	4		2	4	8		2	4
Input Resolution	10 Bits										
	12 Bits	•	•		•	•			•	•	
Output Resolution	8 Bits										
	12 Bits		•	•			•	•		•	•
Additional Features											
DC/DC Converter		•	•	•	•	•	•	•	•	•	•
Software PGA											
Gains of 1, 2, 4, 8V/V		•	•		•	•			•		
Resistor PGA											
Gains of 1 to 1000V/V		•			•	•			•	•	
4-20mA Output				•		•					
Digital Output Drivers				•			•	•			•
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MULTIBUS™ Intel Compatible Combination Analog I/O Subsystem

MODEL RTI-1200

FEATURES

- **Complete Analog I/O Subsystem**
- **Intel SBC-80/10, 80/20, and MDS Compatible**
- **Memory Mapped I/O Interface**
- **Data Acquisition:**
  - **Up to 32 Input Channels**
  - **Sample and Hold Amplifier**
  - **Programmable Gain Amplifier**
  - **12-Bit A/D Converter**
  - **Input Fault Protection**
- **Real-Time Pacer Clock System**
- **On-Board PROM Socket**
- **Two Optional 12-Bit DAC's**
- **Optional 4-20mA Current Outputs**
- **Optional Single +5V Power**
- **Memory Overlay — RAM and ROM Inhibit**



GENERAL DESCRIPTION

The RTI-1200 is a complete analog input/output subsystem that greatly simplifies the task of interfacing analog signals to Intel SBC-80 Single Board Computers, or other 8080-based microcomputers. It is functionally, electrically, and mechanically compatible with the SBC-80, and all connections to it are made simply by plugging the RTI-1200 into a slot in a card cage that also contains an SBC-80. The RTI-1200 can also be readily interfaced to other 8080-based microcomputers whose address, data, and control busses are accessible.

The RTI-1200 is interfaced to an SBC-80 or other 8080 based microcomputer as a block of contiguous memory locations. It combines on a single printed circuit card many features and capabilities which reduce the hardware required to interface analog signals to a microcomputer, and significantly ease the programming effort associated with inputting and outputting analog signals.

DATA ACQUISITION

The RTI-1200's most basic function is data acquisition. This is accomplished with an analog input multiplexer, a programmable gain amplifier, a sample-and-hold amplifier, and a 12-bit A/D converter. The standard RTI-1200 offers either 16 single ended or 8 differential input channels (user selected). An optional multiplexer expander allows for up to 32 single ended or 16 differential input channels. All of the analog inputs are fully protected up to ±28 volts, and additional protection against larger, potentially destructive overloads is afforded by fusing resistors located at the inputs.

The RTI-1200's A/D Converter can be configured by the user to accept 0 to +10V, ±5V, or ±10V full scale input signals. A programmable gain amplifier preceding the A/D converter has software selectable gains of 1, 2, 4 and 8. This expands the dynamic range of the A/D converter to 15 bits, and results in greater input sensitivity. For example, when operating on the 0 to +10V input range with a programmable gain amplifier gain of 8, the actual input range is 0 to +1.25V. The programmable gain amplifier allows the user to program different gains for different input channels, or to have different gains for varying input levels on the same channel. It is even possible to write software to implement automatic gain ranging operation.

Eight of the input channels have provisions for resistors provided by the user that allow the inputs to accept 4-20mA current loop signals. Output data from the A/D converter is in natural binary code for unipolar input ranges, and at the user's option can be either offset binary or two's complement coding when using bipolar input ranges. A special feature of the RTI-1200's data acquisition operation is that the controlling microcomputer's CPU (i.e., the 8080) is not tied up while a conversion is taking place. This significantly enhances system throughput capability and flexibility, as the CPU is free to pursue other tasks while an A/D conversion is in progress.

ANALOG OUTPUTS

The RTI-1200 has provisions for two optional 12-bit D/A converters which are software driven via double buffered registers. They can be used for such functions as driving an analog recorder, or generating analog control signals. Both D/A converters can be user set to any of five voltage output ranges. The D/A input data is natural binary for unipolar output ranges, and at the user's choice can be offset binary or two's complement for bipolar output ranges. Both analog output channels can also be optionally equipped with 4-20mA current loop outputs. This permits them to drive directly the 4-20mA control loops often used in process and industrial controls.

MULTIBUS is a trademark of Intel Corporation

SPECIFICATIONS (typical @ +25°C and with +5V and ±15V, unless otherwise noted)

DATA ACQUISITION	
Number of Analog Inputs	
Standard	16 Single-Ended or 8 Diff.
With Multiplexer Expander[1]	32 Single-Ended or 16 Diff.
Multiplexer Switching Characteristics	Break-Before-Make. All Switches Open When Power is Off.
Input Voltage Ranges[2]	0 to +10V, ±5V, ±10V
Programmable Gains[3]	1, 2, 4, 8 Software Selectable
Input Impedance	>10^9 Ohms
Input Bias Current	
at +25°C	5nA
over 0 to +70°C	50nA
Diff. Input Bias Current	
at +25°C	3nA
over 0 to +70°C	3.5nA
Input Overvoltage Protection	
Continuous Overvoltage	±28 Volts maximum
Overvoltage >±28V	Fusing Resistors
Accuracy	
Resolution	12 Bits
Nonlinearity Error[4]	±1/2LSB typ, ±1LSB max
Diff. Nonlinearity Error	±1/2LSB typ, ±1LSB max
Quantization Error	±1/2LSB max
Input Offset Voltage[5]	Adjustable to Zero
Gain Error[5]	Adjustable to Zero
CMRR	75dB min
CMV	±10V
Noise Error[6]	±1/2LSB max
Temperature Coefficients	
Gain	±15ppm/°C typ, ±25ppm/°C max
Offset	±25μV/°C Referred to Input
Diff. Nonlinearity	±3ppm/°C max
Settling Time to ±0.01%[7]	10μs max at any Gain
SHA Aperture Time	90ns
SHA Aperture Width	20ns
SHA Aperture Uncertainty	±5ns
Conversion Time	25μs max
Maximum Throughput Rate[8]	28kHz
ANALOG OUTPUTS	
Number of DAC Channels[9]	2
Accuracy	
Resolution	12 Bits
Nonlinearity Error[4]	±1/2LSB
Diff. Nonlinearity Error	±1/2LSB
Voltage Output Characteristics	
Voltage Output Ranges[2]	±2.5V, 0 to +5V, ±5V, 0 to +10V, ±10V
Output Current	5mA min @ ±10V
Settling Time[10]	10μs max
Gain TC	±8ppm/°C typ, ±15ppm/°C max
Offset TC	±5μV/°C typ, ±20μV/°C max
Current Loop Characteristics[11]	
Current Output Range	4 to 20mA
Load Resistance Range	0 to 500Ω
Loop Supply Voltage	+15V to +30V
Settling Time[12]	50μs max
Gain TC	±10ppm/°C typ, ±25ppm/°C max
Offset TC	±0.4μA/°C
Reference Voltage Output	+5.00V ±0.02% @ 5mA max

REAL-TIME PACER CLOCK SYSTEM	
Modes of Operation	Pacer-Timed Conversion Trigger, Pacer-Timed Interrupt, Pacer Off
Types of Clocks	Variable Frequency R-C, Fixed Frequency Crystal, External
Crystal Clock Freq.[13]	Determined by User Supplied Crystal
Variable Freq. Clock Range	30Hz to 30kHz, User Adjustable
LOGIC DRIVER OUTPUTS	
Number Available	2
Characteristics	Open Collector, 30V max, 300mA max Continuous Sink Current per Output
MICROCOMPUTER INTERFACE	
Compatibility	Completely Compatible with Intel SBC-80/10, SBC-80/20, and MDS Bus System
Type of Interface	Interfaces as a Block of Memory Locations, Using Address, Data and Control Busses.
Position in Memory	User Selectable Among any of 14 Possible Locations.
On-Board PROM	Socket for Intel 2708 or Equivalent 1024 Byte x 8 Bit PROM, of which 1008 Bytes are Usable.
Memory Overlay (Inhibit)	RAM or ROM
POWER REQUIREMENTS[14, 16]	
Without DC/DC Option[15]	+15V ±3% @ 40mA -15V ±3% @ 40mA +5V ±5% @ 1.2A
With DC/DC Option	+5V ±5% @ 1.7A
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	-55°C to +85°C
MECHANICAL	6.75" x 12.00" with 0.6" Board-to-Board Spacing (171.5 x 304.8 x 15.24mm)

NOTES

[1] The multiplexer expander is an option, and is shown in the ordering guide as MUX EXP.

[2] The desired range is user selectable with straps.

[3] The input gain of a channel is multiplied by the gain setting of the programmable gain amplifier (e.g., the input range of the 0 to +10V range when using a gain of 8 is 0 to +1.25V).

[4] Defined as deviation from a straight line passing through the end points of the range.

[5] For any one software programmable gain setting. Maximum offset shift of ±1LSB or gain shift of ±0.02% when using a programmable gain setting other than the one used during calibration.

[6] When using a programmable gain setting of 1. It is ±1.5LSB max when using a programmable gain setting of 8.

[7] For a 20V step. This specification is valid for a step change on one input, or following a channel change, or following a programmable gain change, or simultaneous changes involving any combination of these changes.

[8] Based on a 10μs settling time, followed by a 25μs A/D conversion time. Overall system throughput rate is enhanced because the CPU is not held up during conversions.

[9] Two channels of D/A converters and two channels of current loops are available on an option basis. See Ordering Guide.

[10] To ±0.01% of full scale range following a 20V step.

[11] The current loop characteristics include the effects of the driving D/A converter.

[12] To ±0.02% of full scale current following a full scale step.

[13] Space provided for HC-18/U crystal cut for a frequency of up to 50MHz. User can select to divide crystal frequency by 10^3 or 10^4 on-board the RTI-1200.

[14] Power requirements shown are for an RTI-1200 with no DAC or current loop options.

[15] The DC/DC power converter is an option that converts +5VDC power to ±15V. It is shown in the ordering guide as DC/DC.

[16] +12V and -5V power is required only if optional PROM is used. This power is supplied by the SBC bus.

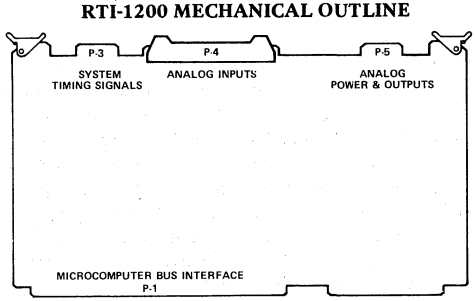
Specificatons subject to change without notice.

RTI-1200 ORDERING GUIDE

MODEL NUMBER	MUX EXP	DACS
RTI-1200-001		
-004		X
-011	X	
-014	X	X
ACCESSORIES		
0A08	4-20mA V/I Module	
0A09	DC/DC Converter	

X DENOTES OPTIONS INCLUDED WITH THE CORRESPONDING MODEL NUMBER. THE OPTIONS ARE DESCRIBED IN NOTES 1, 9, AND 15.

RTI-1200 MECHANICAL OUTLINE



MATING CONNECTORS FOR RTI-1200

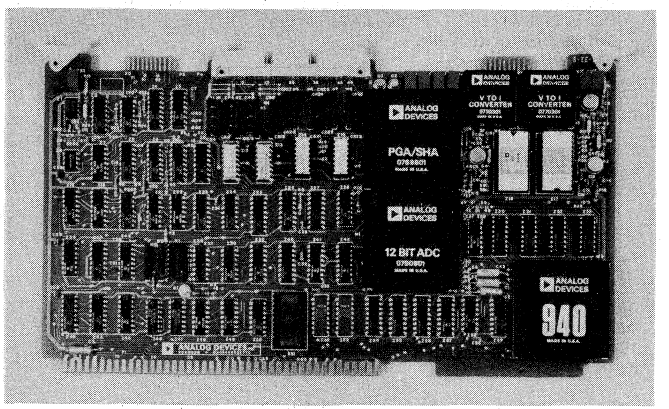
PART NO.	MATES TO	DESCRIPTION
AC1551	P3 or P5	Flat Cable Connector 20 Pin, 0.1" Center
AC1552	P4	Flat Cable Connector 50 Pin, 0.1" Center
AC1553	P4	Flat Cable Connector 50 Pin, 0.1" Center with 2' Color Coded Assembly Attached

ANALOG DEVICES

MULTIBUS™ Intel Compatible Analog Output Subsystem

MODEL RTI-1201

FEATURES
- Low Cost
- Complete Output Subsystem
- SBC-80, SYSTEM-80, MDS, BLC-80 Compatible
- Memory Mapped I/O Interface
- Wire Wrap Feature Selection
- Four Software Controlled Logic Driver Outputs
- Four Channels of 12-Bit Analog Output
- DAC Reset Function
- Optional 4-20mA Current Loop Outputs
- Precision +10V Reference
- Optional Single +5V Power
- Memory Overlay – RAM and ROM Inhibit
- Multiple Card Select Function
- On-Board PROM Socket



GENERAL DESCRIPTION

The RTI-1201 is a complete 8 channel output subsystem comprised of 4 digital and 4 analog channels. This subsystem is electrically and mechanically compatible with the Intel SBC-80 series of single board computers. It is also compatible with the Analog Devices RTI-1200 Analog I/O Interface board, the Intel System-80 microcomputer series, the MDS-800 microcomputer development system and the National Semiconductor BLC-80/10 board level computer.

The RTI-1201 combines on a single printed circuit board many features and capabilities which reduce both the hardware and software effort required to interface a microcomputer to the real world. The RTI-1201 was designed to be extremely versatile, efficient and easy to use in the end user's application. All connections to the microcomputer are made by simply plugging the RTI-1201 into the digital bus connector in the user's card cage. The analog interface is made through a high quality pin connector mounted at the opposite board edge from the digital bus connection. Digital outputs are made at a card edge connector.

DIGITAL OUTPUTS

The RTI-1201 contains four digital output channels. These digital outputs are comprised of high-current logic drivers which can be used for simple "on/off" control of various system functions. These open collector driver outputs are software controlled and have a 30V, 300mA capability.

ANALOG OUTPUTS

The RTI-1201 is configured with four 12-bit D/A converters which are software driven via double buffered registers. They can be used for such functions as driving an analog recorder or generating analog control signals. By using the +10V on-board reference, each of the D/A converters can be individually set by the user to any of five output ranges. The D/A input code for each channel can also be individually set for natural binary, offset binary, or two's complement. The desired configuration is user selectable at convenient wire wrap posts.

REFERENCE

The RTI-1201 inherently guarantees superb tracking capability of all analog output channels since they all share a single on-board reference. This reference is also buffered and brought out for user convenience. The user may also choose to disconnect the internal reference and use the provision for an external reference.

REMOTE SENSING

Sense inputs of the D/A converter are present at the output connector for applications where the load is to be located a considerable distance from the RTI-1201. Without this feature, IR drops in the output line could rapidly degrade overall accuracy. The board is shipped with jumpers connecting the D/A converter sense inputs to local sense points.

DAC DATA REGISTERS

The D/A converters are software driven via double buffered registers. The buffers allow two data bytes to be loaded simultaneously into the D/A converter so that the output changes directly from one 12-bit value to another. The RTI-1201 also has a provision for writing the 8 MSBs in a single byte word to each D/A converter. This allows fast, highly accurate, eight-bit operation.

MULTIBUS is a trademark of Intel Corporation.

SPECIFICATIONS (typical at +25°C and with nominal voltages, unless otherwise noted)

RTI-1201 ANALOG/DIGITAL OUTPUT BOARD

ANALOG OUTPUTS	
Number Available	4 DACs
Accuracy[2]	
Resolution	12 Bits
Overall Error	±1/2LSB (0.0125% FSR)
Voltage Output Characteristics	
Ranges[3]	0 to 5V, 0 to 10V, ±2.5V, ±5V, ±10V
Output Current	5mA min @ ±10V
Settling Time (to 0.02% FS for 10V Step)	5μs
Offset T.C.	±10μV/°C
Gain T.C.	±10ppm/°C
Current Loop Characteristics[1, 4]	
Number	0 to 4
Range	4-20mA Nonisolated
Compliance Voltage[5]	10V @ 20mA with 18V to 30V Supply
Loop Supply Voltage Range	+15V to +30V
Settling Time (to ±0.01% for Full Scale Step)	50μs max
Offset T.C.	±0.4μA/°C
Gain T.C.	±15ppm/°C
Load Resistance Range	0 to 500 ohms
Digital Input Coding[3]	BIN, OBN, 2SC
DAC Load Sense	Provision is made for Local (on-board) or External Load Sensing for each DAC.
Reset[3]	All DACs can be Reset to 0V Output with a Single Write Instruction or upon System Reset. All logic drivers can be turned "off" upon system reset.
On-Board Reference[6]	
Voltage Output	+10.00V ±0.02% @ 2mA
T.C.	±10ppm/°C
External Reference Input[6]	
Range	1V to +10V
Input Impedance	20kΩ ±15%

LOGIC DRIVER OUTPUTS

Number	4
Characteristics	Open Collector, 30V max, 300m A max Continuous Sink Current per Output

MICROCOMPUTER INTERFACE

Compatibility	Completely Compatible with Intel SBC-80/10, SBC-80/20, and MDS Bus System; RTI-1200; BLC-80/10
Type of Interface	Interfaces as a Block of Memory Locations, Using Address, Data and Control Busses.
Position in Memory[7]	User Selectable Among any of 16 Possible Locations.
Card Select Feature[7]	16 Cards per 1K Memory Position
On-Board PROM Socket	Socket for Intel 2708 or Equivalent 1024 Byte x 8-Bit PROM, of which 1008 Bytes are Usable. +12V and -5V are supplied from the Digital Bus.
Memory Overlay (Inhibit)[3]	RAM or ROM

POWER REQUIREMENTS[8]

Without DC/DC Options	
RTI-1201-040	+15V ±3% @ 45mA -15V ±3% @ 95mA +5V ±5% @ 800mA
Per V/I (0A08)	+15V ±3% @ 5mA -15V ±3% @ 1mA
With DC/DC (0A09) Option[9]	
RTI-1201-040, 0A09 and 4, 0A08's	+5V ±5% @ 1700mA max

TEMPERATURE RANGE

Operations	0 to +70°C
Storage	-55°C to +85°C

MECHANICAL

Size	6.75" x 12.00" with 0.6" min Board Spacing (171.5 x 304.8 x 15.2mm)
Connectors	See Ordering Guide

NOTES

[1] See ordering guide for information.

[2] Overall error is specified with gain and offset trimmed and is defined as the deviation from a straight line passing through the end points of the range. It is expressed in terms of bits and in terms of the deviation as a percent of the full scale range, (i.e., 2.5mV is 0.0125% FSR of a -10V to +10V range).

[3] User selectable with wire-wrap jumpers.

[4] The current loop specifications include the effects of the driving D/A converter.

[5] Up to 11V compliance is possible @ 20mA with a +18V minimum loop supply.

[6] The reference is trimmed to within 0.02% accuracy at no load. Long term drift is less than 1/2LSB/1000 Hours operation. DAC accuracy is reduced with lower reference levels. Overall error is 0.1% with a 1V external reference input.

[7] The memory map shows in detail where the data and control functions appear in memory.

[8] Power requirements shown are for RTI-1201-040 with 4 DACs and no Current Loop options. Power requirements for each additional pair of V/I converters are also shown.

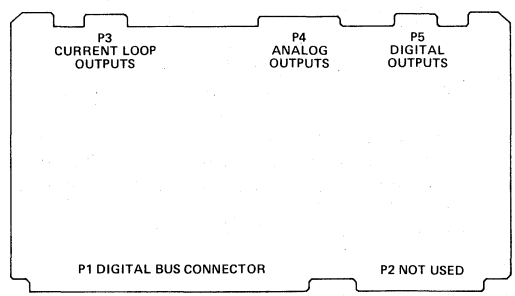
[9] The DC/DC converter option provides ±15V for the analog circuits from the SBC system's +5V bus.

Specifications subject to change without notice.

RTI-1201 ORDERING GUIDE

MODEL NUMBER	DESCRIPTION
RTI-1201-040	**Output Subsystem With 4 DAC's**
ACCESSORIES	
0A08	**4-20mA V/I Converter (order 0, 2 or 4)**
0A09	**DC/DC Converter (+5V to ±15V)**

MECHANICAL OUTLINE



MATING CONNECTIONS

	Mates to	Description
AC1551	P3 or P5 (Card Edge Connector)	Solder Tail Connector 20 pin, 0.1" centers w/o connecting cable
AC1555	P4 (Analog Pin Connector)	Flat Cable Connector 20 pin, 0.1" centers with 2' color coded cable attached
AC1556	P3 or P5 (Card Edge Connector)	Flat Cable Connector 20 pin, 0.1" centers with 3' color coded cable attached

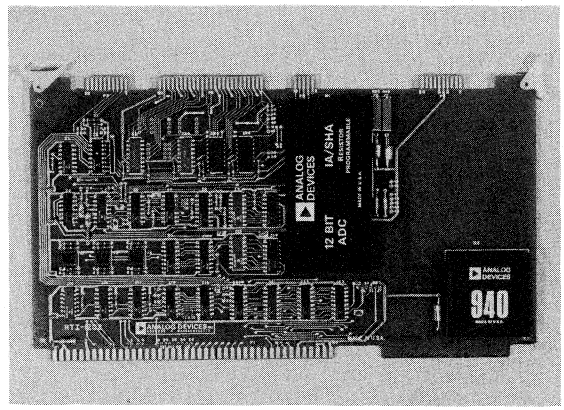
MULTIBUS™ Intel Compatible Analog Input Subsystems

MODEL RTI-1202

FEATURES

Complete Analog Input Subsystems for OEM Applications
SBC-80, System-80, MDS, BLC-80 Compatible
Memory Mapped I/O Interface
Wire-Wrap Feature Selection
Data Acquisition:
- **Up to 32 Input Channels On-Board**
- **Auto Scan Operation Mode**
- **Input Fault Protection**
- **Instrumentation Amplifier**
- **Sample and Hold Amplifier**
- **4-20mA Current Loop Inputs**
- **12-Bit ADC (RTI-1202-R)**

Interrupt Operation Mode
Memory Overlay — RAM and ROM Inhibit
Optional Single +5V Power



GENERAL DESCRIPTION

The RTI-1202-R represents a complete cost-effective solution to *OEM* applications. This analog input system is electrically and mechanically compatible with the Intel SBC-80 series of single board microcomputers. In addition, the RTI-1202 is compatible with the Intel MDS microcomputer development system, the National Semiconductor BLC-80 microcomputer board and many other MULTIBUS™ compatible microcomputers.

The RTI-1202 offers on a single printed circuit board many features that significantly simplify interfacing microcomputers to real world analog signals. These analog input subsystems are versatile, easy to use and cost effective. All connections to the microcomputer are made by simply plugging the subsystem into the digital bus connector in the user's card cage. The analog signals are connected to the system via a printed circuit board connector.

The RTI-1202 analog input subsystem offers up to 32 channels of protected multiplexer input, a selectable gain instrumentation amplifier, a sample and hold amplifier, and a 12-bit A/D converter.

INPUTS

The basic RTI-1202-R offers 16 single-ended, 16 pseudo-differential, or 8 differential input channels (jumper selectable). Each input channel is fully protected to 20 volts beyond the supply voltages ($\pm V_{CC}$ ±20V). The number of input channels can be expanded on board to 32 channels and off board to 256 channels.

The multiplexer outputs are connected to the inputs of a resistor programmable instrumentation amplifier. A single metal film or wire-wound resistor can be used to set the amplifier gain to any value between 1 and 1000. The instrumentation amplifier provides low level signal acquisition with a system CMRR (Common Mode Rejection Ratio) consistent with 12-bit resolution.

A/D CONVERSION

The RTI-1202 comes with a high resolution 12-bit ADC (25μs). Data is made available to the microcomputer in a two byte format (8 LSB and 4MSB). For synchronization with external events, a TTL level sync signal can be hardwired to the P-3 edge connector to create an external convert command. A wire-wrap jumper offers the user a choice between autoscan operation and random channel addressing. In the autoscan mode each convert command automatically increments the multiplexer register to the next channel. After a channel is addressed, a built-in convert command delay provides ample time for the input signal to fully settle, before the A/D conversion.

In the memory mapped mode of operation, the user may opt to have the processor continue operation during each conversion, or halt the processor completely during the A/D conversion. The halt mode allows the operator to avoid jumping to an interrupt service routine to read the converted data. By simply addressing the selected channel as a location in memory, the data is automatically transferred to the processor at the completion of the A/D conversion. In the interrupt mode, the optional end of conversion signal sets the EOC bit in the status word, activating any one of eight jumper selectable interrupts. Upon recognition of the interrupt, the microcomputer branches to a service routine to read the converted data. At the end of the service routine the microcomputer continues with the mainline program operation. In addition to end of conversion interrupt and CPU hold, the user can simply loop to check the EOC status bit or wait a sufficient amount of time for the A/D conversion to take place. All four methods are available on this subsystem for maximum user flexibility. The converted data is available in either natural binary, offset binary, or two's complement code.

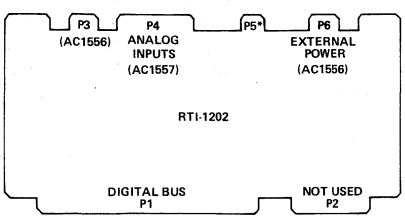
MULTIBUS is a trademark of Intel Corporation.

SPECIFICATIONS (typical at +25°C with nominal supply voltages unless otherwise noted)

MODEL	RTI-1202-R
INPUT	
Number of Analog Inputs	
Standard	16 Single Ended, 16 Pseudo-Differential, or 8 Differential[1]
With Multiplexer Expander Option	32 SE, 32 PD or 16 Diff.[1]
Total Channel Addressing Capability	
Using On Board Logic	256 Total
Multiplexer Switching Characteristics	Break-Before-Make. All Channels Off When No Power Applied
Input Overvoltage Protection	±(V_{CC} +20V)
Input Full Scale Range at Connector[2]	10mV FS to ±10V FS
Current Loop Inputs	16 Locations For User Installed Conversion Resistors
INSTRUMENTATION AMPLIFIER	
Gain Range	1V/V to 1000V/V
Gain Equation	$G = \left(1 + \frac{20k\Omega}{R_G}\right)$
CMV Range	±10V min
CMRR (dc to 100Hz)	74dB min
Input Impedance	$>10^8\,\Omega$
Input Bias Current	±50nA max
0 to +70°C	±70nA
Input Offset Current	±5nA max
0 to +70°C	±7nA
Offset Error	Adjustable to Zero
Gain Error	Adjustable to Zero
Offset T.C.	$\pm\left(1 + \frac{35}{G}\right)\mu V/^{\circ}C$ (RTI)
Gain T.C.	±25ppm of rdg./°C (RTI)
Settling Time[3]	15μs max to 0.01%
SAMPLE/HOLD AMPLIFIER	
Aperture Delay	90ns
Aperture Width	20ns
Aperture Uncertainty	5ns
CONVERSION CHARACTERISTICS	
Resolution	12 Bits
Conversion Time	25μs max
Throughput Rate[4]	40,000 Channels/sec
Nonlinearity Error	±1/2LSB typ, ±1LSB max
Nonlinearity T.C.	±3ppm/°C
Noise Error	±1/4LSB max (G=1) ±1LSB max (G=100)
Overall Error	±1LSB max (G = 1) ±2LSB max (G = 200)
Output Codes[1]	Bin, OBN, 2SC
THE FOLLOWING SPECIFICATIONS APPLY TO ALL BOARDS	
POWER REQUIREMENTS	
Without dc-dc Converter	650mA
+5V, ±5%	
+15V, ±3%	40mA
-15V, ±3%	40mA
With dc-dc Converter	
+5V ±5%	1100mA
MICROCOMPUTER INTERFACE	
Digital Bus Connections	SBC-80 "Multibus" Compatible (1TTL Load max)
Type of Interface	Memory Mapped Using Data, Address and Control Buses
Position in Memory	Selectable by the Use of 3 on-board sockets
Memory Overlay (Inhibit)	RAM or ROM
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	-55°C to +85°C
MECHANICAL	
Size	6.25" (171.5mm) x 12.00" (304.8mm)
Board-Board Spacing	0.7" (15mm)
max Weight	14 ounces (400 grams)

NOTES:
[1] Selectable with wire-wrap jumpers.
[2] The input range at the connector is the A/D converter full scale input range divided by the gain of the instrumentation amplifier.
[3] Settling time is for a 20V step or any channel change at G = 1. Settling time will increase to 55μs at G = 1000.
[4] The effective throughput rate is determined by the user's software data handling capability. The maximum throughput rate listed is exclusive of the CPU interface operations which may or may not be completed during the subsystem's conversion time. In the CPU hold mode, the user's software and interface time must be added to the conversion time to determine the maximum effective throughput rate.
Specifications subject to change without notice.

MECHANICAL OUTLINE



*CABLE NOT AVAILABLE

ORDERING GUIDE

MODEL NUMBER	DESCRIPTION
RTI-1202-R	Input Board with 12-Bit ADC and Resistor Programmable Gain IA
ACCESSORIES	
0A09	DC-DC Converter (5V to ±15V)
0A10	Multiplexer Expansion Kit (2 ea. HI-508A)
CONNECTORS	
AC1556	20 Pin, Card Edge, with 3' Cable
AC1557	50 Pin, Card Edge, with 3' Cable

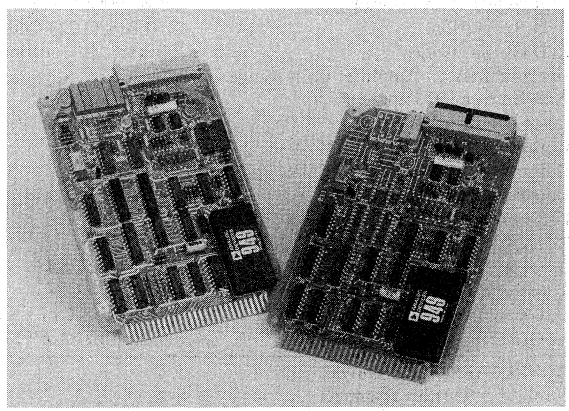
Low Cost, STD Bus Compatible Analog I/O Subsystems

RTI-1225/1226

FEATURES
RTI-1225 ANALOG INPUT/OUTPUT CARD
16 Single-Ended/8 Differential Input Channels
2 Output Channels
10-Bit A/D and 8-Bit D/A Resolution

RTI-1226 ANALOG INPUT CARD
16 Single-Ended/8 Differential Input Channels
10-Bit A/D Resolution

GENERAL
Low Cost
Single +5V Power Requirement
Memory Mapped I/O
Compatible with All STD CPU Cards



SERIES DESCRIPTION

Analog Devices' RTI-1225 series products handle analog inputs and outputs for STD Bus microcomputer systems. These subsystems provide a cost effective solution to interfacing with the analog world by minimizing the development time and providing low function cost.

The RTI-1225 combines both analog input and output functions on a single card, thus reducing components count. This design provides data acquisition of analog signals from 8 differential or 16 single-ended, jumper-selectable voltage inputs and 2 independent voltage outputs. Also included is a differential amplifier, a sample and hold circuit and a 10-bit A/D converter (AD571). Throughputs of 25,000 channels per second is achievable. The analog output section consists of two 8-bit D/A converters. Each channel has a user selectable output range of 0 to +10V, ±5V and ±10V.

The RTI-1226 Analog Input Card provides the same analog functions as the RTI-1225, but does not include the two channels of 8-bit analog output. An ideal choice when only analog inputs are required, this card can be configured for 0 to +10V, ±5V and ±10V input ranges.

The RTI-1225 series cards come complete with their own dc/dc converters, allowing the cards to operate directly from the microcomputer's +5V supply. Configured as a block of contiguous memory locations (memory mapped interface), these products simplify the task of interfacing STD Bus microcomputers to the real world.

For higher performance 12-bit resolution, please reference our RTI-1260 series products.

		INPUT		OUTPUT	
Card Type	Model No.	Channel Capacity	A/D Resolution	Channel Capacity	D/A Resolution
Analog Input/ Output	RTI-1225	16SE/8D	10 Bits	2	8 Bits
Analog Input	RTI-1226	16SE/8D	10 Bits	←——N/A——→	

RTI-1225/1226 Function Chart

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SPECIFICATIONS (typical @ +25°C with nominal supply voltage unless otherwise noted)

INPUT	
Number of Input Channels	16 Single-Ended or 8 Differential (Jumper Selectable)
Input Overvoltage Protection[1]	±35V (Dielectrically Isolated)
Input Impedance	$>10^8\ \Omega$
Input Current	±50nA
Input Voltage Ranges[2]	0V to +10V, ±5V, ±10V
Input/Output Connector	3M #3493, 34 pin
A/D Resolution	10 Bits (1024 Counts)
A/D Output Codes[2]	Binary, Offset Binary, Two's Complement
Instrumentation Amplifier Gain Range	1V/V
A/D Conversion Time	25μs
System Throughput	25,000 channels/sec
Common Mode Voltage (CMV)	±10V min
Common Mode Rejection (CMR)	60dB
Linearity	±1/2LSB
Differential Nonlinearity	±1/2LSB
Total System Error	
(Adjustable to Zero)	±0.1% of FSR
Temperature Coefficient	
Gain	±50ppm/°C of FSR (Full Scale Range)
Offset	±25ppm/°C of FSR
OUTPUT (RTI-1225 Only)	
Number of Output Channels	2
D/A Resolution	8 Bits (256 Counts)
D/A Input Codes[2]	Binary, Offset Binary, Two's Complement
Output Voltage Ranges[2]	0V to +10V, ±5V, ±10V @ 5mA
Output Settling Time	25μs (to ±1/2LSB)
Nonlinearity	±1/2LSB
Differential Nonlinearity	±1/2LSB
Total Error (Adjustable To Zero)	±0.4%
Temperature Coefficient	
Gain	±50ppm/°C of FSR
Offset	±30μV/°C
INTERFACE PARAMETERS	
Compatibility	Meets all electrical and mechanical STD bus specifications
Implementation	Memory mapped I/O, compatible with all CPU types
Address Selection	5 contiguous bytes in a 16 byte block jumper selectable in any one of 256 locations in 64k of memory space
POWER REQUIREMENT	+5V ±5% @ 750mA (on-board dc/dc converter generates an isolated ±15V to power the data acquisition components)
TEMPERATURE	
Operation	0 to +70°C
Storage	-55°C to +85°C
RELATIVE HUMIDITY	Meets or exceeds MIL-STD 202 Method 103

[1] Specification with power applied, ±20V with power off.
[2] User selectable with wire-wrap jumpers.
Specifications subject to change without notice.

ORDERING GUIDE

ADI Model No.	Description	Used On
Cards		
RTI-1225	Analog Input/Output Card	–
RTI-1226	Analog Input Card	–
Mating Connectors		
AC1562	34 pin flat cable connector with 3′ color coded cable	
	Analog Input/Output	RTI-1225
	Analog Input	RTI-1226
User's Manual*		
AC1564	User's Manual for RTI-1225/1226	–

*A user's manual is furnished with each shipment. Additional copies are available under this part number.

Micromodule Motorola Compatible Analog I/O Subsystems

MODELS RTI-1230, 1231, 1232

FEATURES

- **Complete Analog I/O Systems for OEM Applications**
- **Motorola Micromodule and EXORcisor Compatible**
- **Memory Mapped I/O Interface**
- **Convenient Address and Features Selection**
- **12-Bit ADC**
- **Direct Operation from ±12V, +5V Bus Power**
- **Analog Input Subsystem RTI-1230**
  - **Up to 32 Input Channels**
  - **Each Input Channel Protected to V_{CC} +20 Volts**
  - **Software or Resistor Programmable Gain**
  - **Software Controlled EOC Interrupt**
  - **Auto Scan Capability**
  - **0-20mA Current Loop Input**
- **Analog Combination I/O Subsystem RTI-1231**
  - **Same Analog Input Features Plus:**
    - **Two 12-Bit D/A Converters**
    - **4 Quadrant Multiplication**
    - **On-Board or External Reference Capability**
- **Analog Output Subsystem RTI-1232**
  - **Four Independent 12-Bit Analog Outputs**
  - **Four Software Controlled, High Current Logic Driver Outputs**
  - **Optional 4-20mA Current Loop Converter Outputs**
  - **DAC and Logic Driver Reset**
  - **Remote Load Sensing**

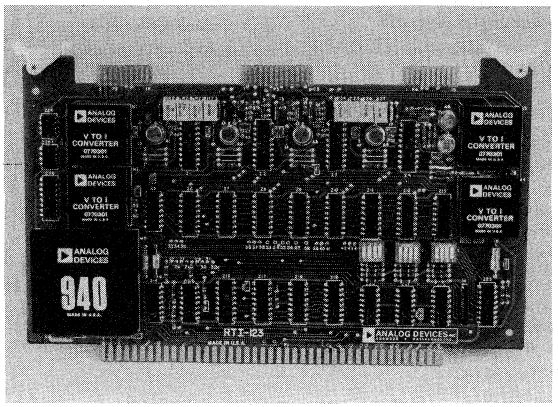
SERIES DESCRIPTION

The RTI-1230 series are complete 12-bit analog I/O subsystems which are electrically and mechanically compatible with the Motorola EXORcisor Development System and Micromodule single board microcomputer. The series is comprised of an input only board (RTI-1230), an output only board (RTI-1232), and a combination I/O board (RTI-1231); each of which interfaces to the microcomputer as a block of 16 address locations (memory mapped interface). All data bus, control bus and address bus connections to the microcomputer are made by simply plugging the board into the computer card cage. The analog signals connect at the opposite board edge from the digital bus connector.

Many additional features and options reduce both the hardware and the software effort required to interface analog signals to the microcomputer, freeing the designer to spend more time and effort on his particular application.

RTI-1230 ANALOG INPUT SUBSYSTEM

The basic function of the RTI-1230 input subsystem is to digitize analog signals and transfer the converted digital data to the microcomputer. The design includes protected input multiplexers, either a resistor-programmable-gain or a software programmable-gain instrumentation amplifier, a sample and hold amplifier, a 12-bit analog to digital (A/D) converter (RTI-1230-R and RTI-1230-S) and the associated digital interface logic.



RTI-1231 COMBINATION ANALOG I/O SUBSYSTEM

The RTI-1231 provides the same analog input functions as the RTI-1230 *plus* two channels of high resolution, 12-bit analog voltage output. The 12-bit digital to analog converters are capable of full 4 quadrant multiplication. Four output voltage ranges can be jumper selected independently for each output channel, by using the on-board references.

RTI-1232 ANALOG OUTPUT SUBSYSTEM

The RTI-1232 output subsystem provides 4 channels of 12-bit analog output and 4 high current, digital logic driver outputs. The four digital outputs are software controlled, open collector drivers capable of sinking 300mA and sustaining voltages up to +30V. They can be used to provide "ON/OFF" system functions for driving relays, solenoids, and valve control.

The DAC's used are 4 quadrant multiplying 12-bit DAC's. Each DAC input code and output range are jumper selectable.

The analog output channels can also be ordered with optional 4-20mA current loop outputs ideal for use in process and industrial control applications. These high compliance voltage to current (V/I) converter modules (P/N 0A08) meet all the requirements of ISA-S50.1 compatibility of signal for Type 3, Class L, nonisolated 4-20mA current loop transmitters.

SPECIFICATIONS (typical @ +25°C and +5V, ±15V unless otherwise noted)

ANALOG INPUT		
Model Numbers - Input Boards:	RTI-1230-R	RTI-1230-S
Combo I/O Boards:	RTI-1231-R	RTI-1231-S
Input Channels: Basic Board	16 SE, 16 PD, 8 Diff.	*
with On-Board Expansion	32 SE, 32 PD, 16 Diff.	*
with Off-Board Expansion	256 Total	*
Input Range at Card Edge	10mV F.S. to ±10V F.S.	0.625V F.S. to ±10V F.S.
Current Loop Inputs	Resistor Selectable	*
Input Protection	±(V_{CC} +20V)	*
Switching Characteristics	Break-Before-Make	*
Instrumentation Amplifier Gain	Resistor Programmable	Software Programmable
Gain Range	1V/V to 1000V/V	1, 2, 4, 8V/V
CMV Range	±10V min	*
CMRR (dc to 500Hz)	78dB min	*
Input Settling Time (G = 1)	15μs max	10μs max
Input Impedance	$>10^8\Omega$	*
Input Bias Current	±50nA	±5nA max
0 to +70°C	±70nA max	±50nA max
ADC Resolution	12 Bits	12 Bits
Conversion Time	25μs max	*
Throughput Rate	40K Channels/sec	*
ADC Input Ranges	±5V, ±5.12V, ±10V, ±10.24V ±2.5V, +5V, +10V, +10.24V	*
ADC Output Codes	BIN, OBN, 2SC	*
Nonlinearity Error	±1/2LSB typ (±1LSB max)	*
Offset Error	Adj. to Zero	*
Offset TC (RTI)	$\left(1+\frac{50}{G}\right)$ μV/°C	±50μV/°C
Gain Error	Adj. to Zero	*
Gain TC (RTI)	±25ppm of RDG./°C	*
Noise Error (G = 1)	±1/4LSB max	*
Overall Error (G = 1)	±1LSB max	*
Overall Error	±1LSB at G = 100	±1.5LSB at G = 8

ANALOG OUTPUT		
Model Numbers -		
Combo I/O Boards:	RTI-1231-R, S	
Output Boards:		RTI-1232
Output Channels	2	4
DAC Resolution	12 Bit	*
Nonlinearity Error	±0.05% FSR	*
Settling Time for a 20V Step	10μs max	*
Output Ranges	±5V, ±10V, +5V, +10V	*
Output Current	5mA @ 10V	*
Offset Error	Adj. to Zero	*
Offset TC	±25μV/°C	*
Gain Error	Adj. to Zero	*
Gain TC	±25ppm/°C	*
External Reference Range	-10V to +10V	*
Input Impedance	10kΩ Each DAC	*
DAC Input Codes	BIN, OBN, 2SC	*
DAC Updating	Double Buffered	*
Load Sensing	Each DAC	*

CURRENT LOOP OUTPUTS (RTI-1232)	(Option P/N 0A08)
Type	ISA-S50.1, Type 3, Class L
Number	One per DAC
Output Current Range	4-20mA (Nonisolated)
Supply Voltage Range	+15V to +30V
Load Resistance Range	0Ω to 475Ω
Offset TC	±0.4μA/°C
Gain TC	±30ppm/°C
Nonlinearity	±1/2LSB
Settling Time	50μs max to 0.05%

DIGITAL OUTPUTS (RTI-1232)	
Type	Open Collector Peripheral Driver
Number	4(Independently Controlled)
Current Range	300mA max Sink Current at 0.1V
Supply Voltage Range	30V max at the Collectors

MECHANICAL	
Size	9.75" x 6.00" x 0.6" (247.6mm x 156.2mm x 15.2mm)
Weight	14 oz (500gm)

TEMPERATURE RANGE	
Operating 0 to +70°C	0 to +70°C
Storage	-25°C to +85°C

*Same specifications as for RTI-1231-R.
Specifications subject to change without notice.

POWER REQUIREMENTS

Without dc-dc Option	Input Boards	Output Boards	Combo Boards	0A08(2)
±15V/±3%	30mA	50mA	50mA	10mA
-15V/±3%	30mA	40mA	45mA	2mA
+5V/±5%	700mA	350mA	900mA	0mA
With dc-dc Option				
+5V/±5%	1100mA	950mA	–	-

ORDERING GUIDE

MODEL NUMBER	DESCRIPTION
RTI-1230-R	**Input Board with 12 Bit A/D and Resistor Programmable Gain Amplifier**
RTI-1230-S	**Input Board with Software PGA**
RTI-1231-R	**I/O Board with Resistor Programmable Gain Amplifier**
RTI-1231-S	**I/O Board with Software PGA**
RTI-1232	**Output Board with 4 DAC's**
ACCESSORIES	
0A08	**4–20mA V/I Module**
0A09	**DC-DC Converter**
0A10	**Multiplexer Expansion Kit**
CONNECTORS	
AC1556	**20 Pin, Card Edge***
AC1557	**50 Pin, Card Edge***
AC1559	**26 Pin, Card Edge***

***ALL CONNECTORS HAVE 3' OF COLOR CODED CABLE ATTACHED**

TM-990/100M Texas Instruments Compatible Analog I/O Subsystems

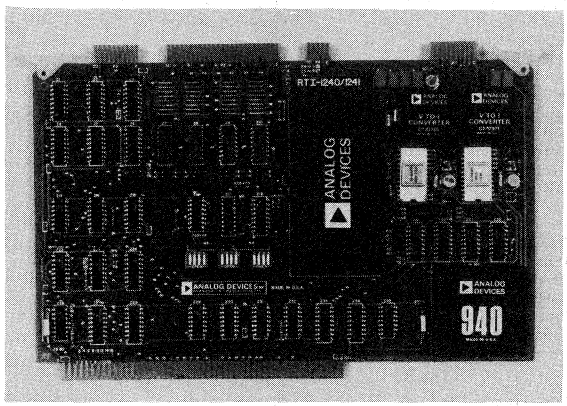
MODELS RTI-1240, 1241, 1242, 1243

FEATURES
- **Complete Analog I/O Subsystems**
- **T.I. 16-Bit TM-990/100M Compatibility**
- **Memory Mapped I/O Interface**
- **12-Bit Resolution and Accuracy**
- **Optional Single +5V Power**
- **Wire Wrap Feature Selection**

INPUT SUBSYSTEMS
- **256 Channel Expansion Capability**
- **Input Overvoltage Protection**
- **Software or Resistor Programmable Gain**
- **Interrupt Operation Capability**
- **Optional Analog Output Channels**
- **Multiplexer Auto Increment**

OUTPUT SUBSYSTEMS
- **8 High Current Logic Driver Outputs**
- **4 or 8 Analog Output Channels**

Detailed User's Guide



SERIES DESCRIPTION

The RTI-1240 Series are complete, 12-bit resolution, analog I/O subsystems which are electrically and mechanically compatible with the Texas Instruments 16-bit TM-990/100M single board microcomputer. The series is comprised of an input board, two output boards, and a combination I/O board; each of which interfaces to the microcomputer as a block of 8 or 16 address locations (memory mapped interface). All data bus, control bus and address bus connections to the microcomputer are made by simply plugging the board into the computer card cage. The analog signals connect at the opposite board edge from the digital bus connector.

Many additional capabilities, features and options are included to reduce both the hardware and the software effort required in interfacing analog signals to the microcomputer. The designer is then free to spend more time and effort on the particular application instead of on designing basic building block functions.

RTI-1240 ANALOG INPUT SUBSYSTEM

The basic function of the RTI-1240 is to acquire signals and present them to the microcomputer in digital form. The design is comprised of a protected input multiplexer, either a resistor or a software programmable gain instrumentation amplifier, a sample and hold amplifier, a 12-bit A/D converter and the associated digital interface logic.

INPUT MULTIPLEXER

The RTI-1240 is available with up to 32 single-ended/16 differential protected input channels on-board, and has the capability of off-board expansion to 256 channels using on-board control logic. The multiplexer (MUX) channel can be randomly selected at the MUX word in the memory map. The MUX can also be incremented to the next channel upon receipt of a convert command. This auto increment feature is enabled by a software command to the setup word which allows scanning and random channel addressing to be mixed under software control.

INSTRUMENTATION AMPLIFIER/SAMPLE AND HOLD AMPLIFIER

The RTI-1240 is available with two types of instrumentation amplifiers (IA) which provide 12-bit compatible CMRR and CMV specifications. The software-programmable-gain (1-2-4-8) IA provides dynamic range expansion through subranging as well as the flexibility of using different gain settings for each input channel to accommodate different signal levels. The resistor-programmable-gain IA may be used for input ranges from 10mV F.S. to ±10V F.S. There is very little loss of speed and no degradation of linearity at high gains.

The sample and hold amplifier (SHA) allows sampling of high slew rate signals and is automatically switched to the hold mode upon receipt of a convert command. The RTI-1240 also has a built-in provision which delays the convert command to allow for input section settling following a gain change or channel change. For very high gain applications, the convert command delay can be increased either through software or by addition of a single resistor.

SPECIFICATIONS (typical @ +25°C and nominal supply voltage)

ANALOG INPUT	COMBINATION I/O BOARDS		INPUT ONLY BOARDS	
Model Numbers	RTI-1241-R	RTI-1241-S	RTI-1240-R	RTI-1240-S
Input Channels				
Basic Board	16 SE, 16 PD, 8 Diff.[1]	*	*	*
Expansion: On-Board	32 SE, 32 PD, 16 Diff.[1]	*	*	*
Off-Board	256 Total	*	*	*
Input Range at Card Edge[2]	10mVFS to ±10VFS	0.625 to ±10VFS	*	**
Current Loop Inputs[3]	0 to 50mA, 0 to 20mA, etc.	*	*	*
Input Protection	$\pm(V_{CC}+20V)$	*	*	*
Switching	Break-Before-Make	*	*	*
Input Impedance	$>10^8\Omega$	*	*	*
Input Bias Current	±50nA max	±5nA max	*	**
0 to +70°C	±70nA	±50nA	*	**
Instrumentation Amplifier	Resistor Programmable Gain	Software Programmable Gain	*	**
Gain Range	1 to 1000 V/V $\left[G = 1 + \frac{20k}{R}\right]$	1, 2, 4, 8 V/V	*	**
CMV	±10V min	*	*	*
CMRR (dc–500Hz)	76dB min	*	*	*
Input Settling Time[4]	15µs max (G = 1)	10µs max (G = 1 to 8)	*	**
ADC Input Ranges[1]	±5V, ±5.12V, ±10V, ±10.24V, +10V, +10.24V	*	*	*
Resolution	12 Bits	*	*	*
Conversion Time	25µs max	*	*	*
Throughput Rate[5]	40,000 Channels/sec	*	*	*
Output Codes[1]	Binary, Offset Binary, Two's Complement	*	*	*
Nonlinearity Error	±1/2LSB typ (±1LSB max)	*	*	*
Offset Error[6]	Adj. to Zero	*	*	**
Gain Error[6]	Adj. to Zero	*	*	*
Offset TC	$\pm(1 + \frac{50}{G})\mu V/°C$ (RTI)	±30µV/°C (RTI)	*	**
Gain TC	±20ppm of rdg/°C (RTI)	±25ppm of rdg/°C (RTI)	*	**
Noise Error[7]	±1/4LSB max	*	*	*
Overall Error @ G = 1[8]	±1LSB max	*	*	*
SHA Aperture Delay	90ns	*	*	*
SHA Aperture Width	20ns	*	*	*
SHA Aperture Uncertainty	5ns	*	*	*

ANALOG OUTPUT	OUTPUT ONLY BOARDS			
Model Number	RTI-1241-R	RTI-1241-S	RTI-1242	RTI-1243
Output Channels	2	2	4	8
Resolution	12 Bits	*	*	*
Output Ranges[1] (with on board Ref)	+5V, +10V, ±2.5V, ±5V, ±10V	*	*	*
Output Current	±5mA min @ ±10V	*	*	*
Nonlinearity Error @ +10V Ref	±0.01% max	*	*	*
Offset Error	Adj. to Zero	*	*	*
Gain Error	Adj. to Zero	*	*	*
Offset TC	±15µV/°C	*	*	*
Gain TC	±15ppm/°C	*	*	*
Settling Time[8] (for 20V step to ±0.01%)	10µs	*	*	*
Reference Range External[9]	1V to +10V	*	*	*
Input Codes	Binary, Two's Complement, or Offset Binary	*	*	*
OTHER OUTPUTS	2 Optional Current Loops	*	8 Logic Drivers	***
Type	ISA-S50.1, Type 3, Class L	*	Open Collector	***
Output Current Range[10]	4-20mA	*	300mA sink @ 0.7V	***
Supply Voltage Range	+15V to +30V	*	+30V max	***
Input Voltage Range	0V to +10V	*		
Offset Error	Adj. to Zero	*		
Gain Error	Adj. to Zero	*		
Offset TC	±0.4µA/°C	*		
Gain TC	±30ppm/°C	*		
Nonlinearity Error	±0.01% max	*		
Settling Time	50µs max to 0.02%	*		

POWER REQUIREMENTS					
Model Number	RTI-1240	RTI-1241	RTI-1242	RTI-1243	V/I
Without Optional dc-dc					
+15V ±3%	40mA	50mA	45mA	50mA	10mA
–15V ±3%	40mA	80mA	80mA	150mA	2mA
+5V ±5%	1100mA	1100mA	900mA	1000mA	0mA
With dc-dc Option					
+5V ±5%	1.4A	1.5A	1.3A	1.6A	mA

MECHANICAL (All Models)	
Size	7.5" x 11.0" (190.5mm x 279.4mm)
Card Outline	Conforms to Texas Instruments Drawing SK922321
Card Spacing	0.6" min (15.2mm)
Operating Temperature	0 to 70°C
Storage Temperature	–25°C to +85°C

*Same as for RTI-1241-R
**Same as for RTI-1241-S
***Same as for RTI-1242
Specifications subject to change without notice.

NOTES
[1] User selectable by wire wrap jumpers.
[2] The full scale input signal range is the A/D converter range divided by the gain of the instrumentation amplifier.
[3] The user may install one resistor per channel (SE or Diff) to convert the input current to the proper voltage range. Any input current span can therefore be accommodated.
[4] Input settling time applies to either a multiplexer channel change or a software controlled gain change. The settling time increases to 50µs @ G = 1000.
[5] The effective throughput rate is determined by the user's software data handling capability. The max throughput rate listed is exclusive of the CPU interface operations which may or may not be completed during the subsystem's conversion time. In CPU hold mode, the user's software and interface time obviously must be added to the conversion time to determine the maximum effective throughput rate.
[6] For any one programmable gain setting. Maximum offset shift of ±1LSB or gain shift of ±0.02% when using a programmable gain setting other than the one used during calibration.
[7] Noise error increases to ±1/2LSB max @ G = 8 for the SPG models and to ±1LSB @ G = 100 for the RPG models.
[8] Overall error increased to ±2LSB max @ G = 8 for the SPG models and ±2LSB max @ G = 1000 for the RPG models.
[9] Overall error increases to 0.1% @ 1V external reference.
[10] The current loop load resistance range is 0Ω to 450Ω with a +15V supply. A load resistance of 500Ω may be used with a +18V supply.

DEC LSI-11 LSI-11/2 and LSI-11/23 Compatible Analog I/O Subsystems

MODELS RTI-1250, 1251, 1252

FEATURES

Complete Analog I/O Subsystems
Digital Equip. Corp. 16-Bit LSI-11/2 and 11/23 Compatibility
Memory Mapped I/O Interface
12-Bit Resolution and Accuracy
Single +5V Power Requirement
4-20mA Current Loop I/O Capability
Convenient Wire Wrap Feature Selection

RTI-1250 Analog Input Subsystem
- **16 Input Channels — Expandable On-Board to 32 Channels**
- **Input Overvoltage Protection to ±35 Volts**
- **Resistor or Software Programmable Gain Amplifier**
- **Software Control of Interrupt, Channel Scanning and External Trigger**

RTI-1251 Analog I/O Subsystem
- **16 Input Channels and 2 12-Bit Analog Output Channels**
- **Four Quadrant Multiplying DAC's**
- **On-Board Reference**

RTI-1252 Analog Output Subsystem
- **2- or 4-, 12-Bit Analog Output Channels**
- **Field Expandable from 2 to 4 DAC Outputs**
- **4 High Current Digital Logic Drivers**
- **Optional 4-20mA Current Loop Outputs**
- **Selectable DAC and Logic Driver Reset**

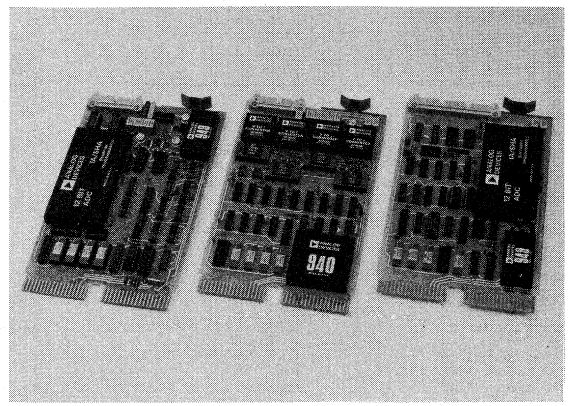
SERIES DESCRIPTION

The RTI-1250 Series products are complete, 12-bit resolution, analog I/O subsystems which are electrically and mechanically compatible with the Digital Equipment Corp. LSI-11, LSI-11/2, and LSI-11/23 single board microcomputers. The series is comprised of an input only board, an output only board, and a combination I/O board; each of which interfaces to the microcomputer as a block of 4 address locations (memory mapped interface). All bus connections to the microcomputer are made by simply plugging the board into the computer card cage. The analog signals connect at the opposite board edge from the digital bus connector.

Many additional capabilities, features and options are included to reduce both the hardware and software effort required to interface analog signals to the microcomputer.

RTI-1250 ANALOG INPUT SUBSYSTEM

The basic function of the RTI-1250 is to convert analog signals into a digital format and to present this digital data to the microcomputer. The design includes a protected input multiplexer for switching up to 32 single-ended inputs, either a software or resistor programmable gain instrumentation amplifier, a sample and hold amplifier, a 12-bit A/D converter and the associated digital interface logic.



INPUT MULTIPLEXER

The RTI-1250 is available with up to 32 single-ended/16 differential protected input channels on board. The multiplexer (MUX) channel can be randomly selected by writing to the MUX ADDRESS BYTE in the memory map. Also, in the AUTO MUX INC mode the MUX can be automatically incremented to the next channel following the receipt of a convert command. This auto increment feature is enabled by a software command which allows sequential scanning and random channel addressing to be mixed under software control.

INSTRUMENTATION AMPLIFIER/SAMPLE AND HOLD AMPLIFIER

The RTI-1250 is available with two types of instrumentation amplifiers (IA) which provide 12-bit compatible CMRR and CMV specifications. The software-programmable-gain (1-2-4-8) IA provides dynamic range expansion through subranging as well as the flexibility of using different gains for each input channel to accommodate different signal levels. The resistor-programmable gain IA may be used for input ranges from 10mV F.S. to ±10V F.S.

The sample and hold amplifier (SHA) allows sampling of high slew rate signals and is automatically switched to the hold mode upon receipt of a convert command. The RTI-1250 also has a built-in provision which delays the convert command to allow the input section to fully settle following a gain change or channel change. For very high gain applications, the convert command delay can be increased either through software or by addition of a single resistor.

SPECIFICATIONS (typical @ +25°C and nominal supply voltages unless otherwise noted)

	INPUT ONLY BOARDS		COMBINATION I/O BOARDS
ANALOG INPUT			
Model Numbers	RTI-1250-R	RTI-1250-S	RTI-1251
Input Channels			
Basic Board	16 SE, 16 PD, 8 Diff.[1]	*	*
Expansion On-Board	32 SE, 32 PD, 16 Diff.[1]	*	None
FS Input Range[2]	±10mVFS to ±10VFS	±0.625VFS to ±10VFS	±10mVFS to ±10VFS
Current Loop Inputs[3]	0 to 50mA, 0-20mA, etc.	*	*
Input Protection	±(V_{CC} +20V)	*	*
Mux Switching	Break-Before-Make	*	*
Input Impedance	>10^8 Ω	*	*
Input Bias Current	±50nA max	±5nA max	±50nA max
0 to +70°C	±70nA	±50nA	±70nA
Instrumentation Amplifier	Resistor Programmable Gain	Software Programmable Gain	Resistor Programmable Gain
Gain Range	1 to 1000V/V	1, 2, 4, 8V/V	1 to 1000V/V
CMV Range	±10V min	*	*
CMRR (dc - 500Hz)	76dB min	*	*
Input Settling Time[4]	20μs max (G = 1)	15μs max (G = 1 to 8)	20μs max (G = 1)
ADC Input Ranges	±2.5V, ±5V, ±10V, 0 to 10V, 0 to 5V	*	±5V, ±10V, 0V to +10V
Resolution	12 Bits	*	*
Conversion Time	25μs max	*	*
Throughput Rate[5]	30,000 Channel/sec.	*	*
Output Codes[1]	Binary, Offset Binary, Two's Complement	*	*
Nonlinearity Error	±1/2LSB typ (±1LSB max)	*	*
Offset Error[6]	Adj. to Zero	*	*
Gain Error[6]	Adj. to Zero	*	*
Offset TC	$\pm\left(1+\frac{50}{G}\right)\mu V/^{\circ}C$ (RTI)	±30μV/°C (RTI)	$\pm\left(1+\frac{50}{G}\right)\mu V/^{\circ}C$ (RTI)
Gain TC	±20ppm of rdg./°C (RTI)	±25ppm of rdg./°C (RTI)	±20ppm of rdg./°C (RTI)
Noise Error[7]	±1/4LSB max	*	*
Overall Error @ G = 1[8]	±1LSB max	*	*
SHA Aperture Delay	90ns	*	*
SHA Aperture Width	20ns	*	*
SHA Aperture Uncertainty	5ns	*	*
ANALOG OUTPUT			
Model Number	RTI-1251	RTI-1252-2	
Output Channels	2	2 expandable to 4	
Resolution	12 Bits	**	
Output Ranges[1] (with on board Ref)	+5V, +10V, ±5V, ±10V	+5V, +10V, ±2.5V, ±5V, ±10V	
Output Current	±5mA min. @ ±10V	**	
Nonlinearity Error	±0.01% max	±0.01%	
Offset Error	Adj. to Zero	**	
Gain Error	Adj. to Zero	**	
Offset TC[10]	±25μV/°C	±25μV/°C	
Gain TC[10]	±25ppm/°C	±15ppm/°C	
Settling Time[8] (for 20V step to ±0.01%)	10μs max	**	
Input Codes	Binary, Two's Complement, or Offset Binary	**	
Reference[11]	-10.00V or -5.00V	+6.3V ±2%	
OTHER OUTPUTS (RTI-1252 ONLY)	V/I Current Loop Converter (Option 0A08)	4 Logic Drivers	
Type	ISA-S50.1, Type 3, Class L	Open Collector	
Output Current Range[9]	4-20mA	300mA sink @ 0.7V	
Supply Voltage Range	+15V to +30V	+30V max	
Input Voltage Range	0V to +10V		
Offset Error	Adj. to Zero		
Gain Error	Adj. to Zero		
Offset TC[12]	±0.4μA/°C		
Gain TC[12]	±30ppm/°C		
Nonlinearity Error[12] (V/I Only)	±0.01% max		
Settling Time[12]	50μs max to 0.02%		

POWER REQUIREMENTS

Model Number	RTI-1250	RTI-1251	RTI-1252	V/I (2)
+5V ±5%	1.4A	1.5A	1.4A	1.7A

MICROCOMPUTER INTERFACE

Complies with D.E.C. bus loading and electrical specifications

TEMPERATURE RANGE

Operation	0 to +70°C (0 - 95% RH non-condensing)
Storage	-55° C to +85°C

MECHANICAL

Size	5" X 8.5" (per D.E.C. Drawing)
Weight	10 ounces
Connectors	See Ordering Guide

*Same as for RTI-1250-R
**Same as for RTI-1251-R

Specifications subject to change without notice.

ORDERING GUIDE

MODEL NUMBER	DESCRIPTION
RTI-1250-R	Input Board with Resistor Programmable Gain Amplifier
RTI-1250-S	Input Board with Software Programmable Gain Amplifier
RTI-1251	I/O Board with Resistor Programmable Gain Amplifier and Two Multiplying DAC's
RTI-1252-2	Output Board with Two Trimmed DAC's
RTI-1252-4	Output Board with Four Trimmed DAC's
ACCESSORIES	
0A08	4-20mA V/I Module
0A10	Multiplexer Expansion Kit (2 ea. HI-0508A-5)
0A12	12-Bit DAC for RTI-1252-2
CONNECTORS	
AC1553	50 Pin, Flat Cable Connector*
AC1554	26 Pin, Flat Cable Connector*
AC1560	14 Pin, Dip Plug Connector*

*All Connectors Have 3' of Color Coded Cable Attached

NOTES:
[1] User selectable by wire-wrap jumpers.
[2] The full scale input signal range is the A/D converter range divided by the gain of the instrumentation amplifier.
[3] The user may install one resistor per channel (4 max with RTI-1251, 8 max with RTI-1250) to convert the input current to the proper voltage range. Any input current span can therefore be accommodated.
[4] This time can overlap A/D conversion period. The settling time increases to 50μs @ G = 1000.
[5] The effective throughput rate is determined by the user's software data handling capability. The max throughput rate listed is exclusive of the CPU interface operations which may or may not be completed during the subsystem's conversion time. The user's software and interface time must be added to the conversion time to determine the maximum effective throughput rate.
[6] For any one programmable gain setting, maximum offset shift of ±1LSB or gain shift of ±0.02% when using a programmable gain setting other than the one used during calibration.
[7] Noise error increased to ±1/2LSB max @ G = 8 for the SPG models and to ±1LSB @ G = 100 for the RPG models.
[8] Overall error increases to ±2LSB max @ G = 8 for the SPG models and 2LSB max @ G = 500 for the RPG models.
[9] The current loop load resistance range is 0Ω to 450Ω with a +15V supply. A load resistance of 500Ω may be used with >+18V supply.
[10] Temperature coefficients are specified for the ±10V full scale range.
[11] The on-board references are also available at the card edge. Users must limit any current load to less than 2mA. External reference inputs have an input impedance of greater than 5kΩ.
[12] Specified for V/I module only (P/N 0A08).

High Performance STD Bus Compatible Analog I/O Subsystems

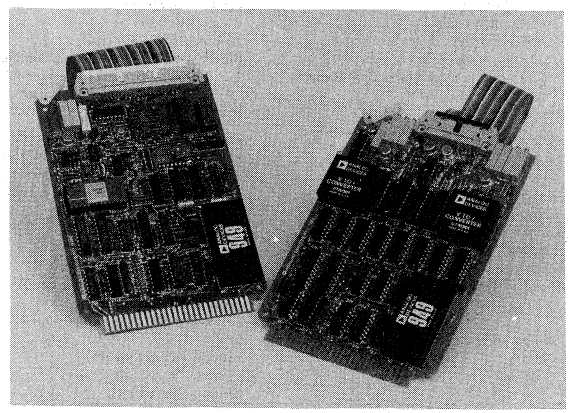
RTI-1260/1262

FEATURES

RTI-1260 ANALOG INPUT CARD
- 32 Single-Ended/16 Differential Channels
- User Configurable Gains of 1 to 1000
- 12-Bit Resolution

RTI-1262 ANALOG OUTPUT CARD
- 4 Analog Output Channels
- 12-Bit Resolution
- Optional 4-20mA Current Loop Outputs

GENERAL
- Low Cost
- Single +5V Power Requirement
- Memory Mapped I/O
- Compatible with All STD CPU Cards



SERIES DESCRIPTION

Analog Devices RTI-1260 series products handle analog inputs and outputs for STD Bus microcomputer systems. These subsystems provide a cost effective solution to interfacing with the analog world by minimizing the development time, providing high performance specifications and predictable results.

The RTI-1260 Analog Input Card provides data acquisition of analog signals from 32 single-ended or 16 differential voltage inputs. User configured gains of 1 to 1000 allow effective input ranges from 10 millivolts to 10 volts. The ability to sample millivolt level signals allows the RTI-1260 to be used for reading strain gages and thermocouples. The 12 bits of resolution is provided using our own A/D converter (AD574). Throughputs of 25,000 channels per second are achievable at a gain of 1.

The RTI-1262 Analog Output Card provides four independent output channels of analog voltage. In addition, two channels can be configured for 4-20mA outputs by adding two voltage to current converters. This product is ideal for process control applications.

The RTI-1260 series boards come complete with their own dc/dc converter, allowing the boards to operate directly from the microcomputer +5V supply. Configured as a block of contiguous memory locations (memory mapped interface), the products simplify the task of interfacing STD Bus microcomputers to the real world.

For low cost, 10-bit resolution, please reference our RTI-1225 series products.

		INPUT				OUTPUT		
		Channel Capacity			A/D		D/A	4-20mA
Card Type	Model No.	STD	OPT	Gain Range	Resolution	Channel Capacity	Resolution	(OPT)
Analog Input	RTI-1260	16SE/8D	32SE/16D	1-1000	12 Bits	← N/A →		
Analog Output	RTI-1262	← N/A →				4	12 Bits	2

RTI-1260/1262 Function Chart

ORDERING GUIDE

ADI Model No.	Description	Used On
Cards		
RTI-1260	Analog Input Card	–
RTI-1262	Analog Output Card	–
Accessories		
OA08	V/I converter provides 4-20mA output from D/A. One required per channel.	RTI-1262 (2 max)
OA10	Multiplexer Expansion Kit expands channel capacity from 16SE/8D to 32SE/16D. One required per board.	RTI-1260
Mating Connectors		
AC1553	50 pin flat cable connector with 3′ color coded cable.	Analog Input
AC1554	26 pin flat cable connector with 3′ color coded cable	Analog Output
User's Manual*		
AC1563	User's Manual for RTI-1260/1262	

*A user manual is furnished with each shipment. Additional copies are available under this part number.

SPECIFICATIONS (typical @ +25°C with nominal supply voltage unless otherwise noted)

RTI-1260 ANALOG INPUT CARD

Number of Input Channels	16 Single-Ended or 8 Differential (Jumper Selectable) Expandable to 32 Single-Ended or 16 Differential using two plug-in multiplexers (ADI Part #OA10)
Input Overvoltage Protection[1]	±35V (Dielectrically Isolated)
Input Impedance	$>10^8\Omega$
Input Current	±50nA
Analog Connector	3M #3433, 50 pin
A/D Input Ranges[2]	0 to +10V, ±10V
A/D Resolution	12 Bits (4096 Counts)
A/D Output Codes[2]	Binary, Offset Binary, Two's Complement
Instrumentation Amplifier Gain Ranges	1 to 1000V/V (Resistor Programmable Gain)
Gain Equation	$G = 1 + \frac{20k\Omega}{R_G}$
A/D Conversion Time	25μs
System Throughput[3]	25,000 Channels/sec (G < 150) 20,000 Channels/sec (150 < G > 300) 13,000 Channels/sec (G = 1000)
Common Mode Voltage (CMV)	±10V min
Common Mode Rejection (CMR)	78dB
Linearity	±1/2LSB
Differential Nonlinearity	±1LSB
Total System Errors (Adjustable to Zero)	±0.01% of FSR (G = 1 to 10) ±0.05% of FSR (G = 100) ±0.1% of FSR (G = 1000)
Temperature Coefficient	
Gain	±30ppm/°C of FSR (G = 1)
Offset	±10ppm/°C of FSR (G = 1) ±100ppm/°C of FSR (G = 1000)
INTERFACE PARAMETERS	
Compatibility	Meets all electrical and mechanical STD Bus specifications
Implementation	Memory mapped I/O, compatible with all CPU types
Address Selection	3 contiguous bytes in a 16 byte block. (Jumper selectable in any one of 256 locations in 64K of memory space.)
POWER REQUIREMENTS	+5V ±5% @ 450mA (on-board dc/dc converter generates an isolated ±15V to power the data acquisition components.)
TEMPERATURE	
Operating	0 to +70°C
Storage	−55°C to +85°C
RELATIVE HUMIDITY	Meets or exceeds MIL-STD 202 Method 103

[1] Specified with power applied, ±20V with power off.
[2] User selectable with wire-wrap jumpers.
[3] Does not include CPU latency time.
Specifications subject to change without notice.

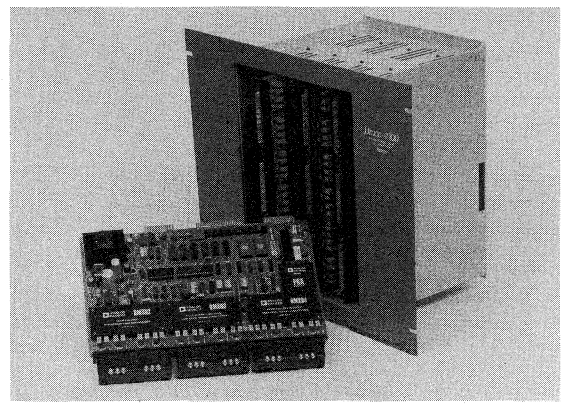
RTI-1262 ANALOG OUTPUT CARD

Number of Output Channels	4
D/A Resolution	12 Bits (4096 Count)
D/A Input Codes[1]	Binary, Offset Binary
Output Voltage Range[1]	0V to +5V, 0V to +10V, ±5V, ±10V @ 5mA
Output Current Range[2]	4-20mA using 2 V/I converters
(Optional—2 Channels Only)	(ADI Part #OA08)
Analog Connector	3M #3429, 26 pin
Nonlinearity	±1/2LSB
Differential Nonlinearity	±1/2LSB
Output Settling Time	25μs (to ±1/2LSB)
Gain Error (Adjustable to Zero)	±0.01% of FSR (Full Scale Range)
Offset Error (Adjustable to Zero)	±0.02% of FSR
Temperature Coefficient	
Gain	±15ppm/°C of FSR
Offset	±25μV/°C
INTERFACE PARAMETERS	
Compatibility	Meets all electrical and mechanical STD BUS specifications
Implementation	Memory mapped I/O compatible with all CPU types
Address Selection	8 contiguous bytes in a 16 byte block (Jumper selectable in any one of 256 locations in 64K of memory space)
POWER REQUIREMENTS	+5V ±5% @ 550mA (on-board dc/dc converter generates an isolated ±15V to power the data acquisition components)
TEMPERATURE	
Operating	0 to +70°C
Storage	−55°C to +85°C
RELATIVE HUMIDITY	Meets or exceeds MIL-STD 202 Method 103

[1] User selectable with wire-wrap jumpers.
[2] Solder in option, +16V to +30V loop power required.
Specifications subject to change without notice.

μMAC-4000
Measurement-and-Control Subsystems

FEATURES
Analog Inputs
Thermocouples, RTDs, Strain Gages, AD590s
High and Low Level Voltages, Current Loops
±1000V Isolated and Nonisolated
Analog Outputs
Voltage and Current
±1000V Isolated and Nonisolated
Digital Inputs/Outputs
Contact Closures
ac and dc Signals (High and Low Level)
Microcomputer Based
Linearization, Unit Conversion, Limit Checking
Powerful Command Set
Serial Communications
20mA or RS-232C
Integral Power Supply
ac or +24V dc



GENERAL DESCRIPTION

The μMAC-4000 Measurement and Control System is a complete, low cost solution designed to simplify process to computer interface in a wide range of industrial automation applications.

The μMAC-4000 offers an unprecedented set of hardware and software capabilities that can be easily tailored to virtually any automation application. Modular design permits expansion within the system and the flexibility to accept a variety of analog and digital input and output functions.

The μMAC-4000 is optimized for high performance measurement and control. Analog inputs handling capability offers reliable operation in harsh, electrically noisy, industrial environments. The high performance is assured by high quality signal conditioning featuring input protection, ±1000V channel-to-channel and input-to-output isolation, high common mode rejection, filtering, low drift amplification and 13-bit A/D conversion. A unique plug-in module approach allows the selection of standard signal conditioning modules for direct connection to a wide range of sensors. The μMAC-4000 scales, linearizes and converts the input data to engineering units.

Both analog and digital control capability is provided by the μMAC-4000 system. Analog outputs feature 12-bit resolution, voltage and 4-20mA/0-20mA current outputs with ±1000V isolation, as well as increment/decrement and bumpless transfer for precise control in either manual or computer mode. Digital I/O offers direct interface to contact closures, TTL levels or high level ac and dc voltages.

The μMAC-4000 system is designed to operate with any host computer which has a 20mA or RS-232C serial port. The μMAC-4000 can be either used as a local front end or located up to 10,000 feet from the host. A powerful command set is included in the μMAC's firmware which allows control via the serial interface bus. Once the command is executed, the results are transmitted back to the host in an ASCII format–at speeds up to 9600 baud.

The μMAC-4000 system requires either ac line power or +24V dc. Circuitry is provided to detect intermittent ac power losses and switch automatically to an external battery backup mode.

A wide variety of packaging options are available to match user requirements. These options include single board enclosures, card cage/rack mounting or NEMA enclosures.

APPLICATIONS

The μMAC-4000 is a versatile, self-contained measurement and control system designed for a broad range of industrial and laboratory applications. It is extremely useful in both control room and remote locations where monitoring and control of temperature, pressure, flow, analog and digital signals are required.

DESIGN FEATURES AND USER BENEFITS

Ease of Use: Direct sensor interface via screw terminal connectors, output in engineering units, powerful command set, make the μMAC-4000 extremely easy to use.

Integral Signal Conditioning: High quality signal conditioning provides input protection and isolation, cold junction compensation for thermocouples, RTD excitation, and sensor linearization and scaling, eliminating the need for expensive external signal conditioning.

High Noise Rejection: The μMAC-4000 preserves high system accuracy in electrically noisy environments, providing excellent common mode and normal mode noise rejections and RFI/EMI immunity.

Control Capability: Analog and digital outputs are provided to control motor speeds, dictate valve positions and drive actuators.

Features such as isolation, bumpless transfer and DAC readback are included in the design.

Expandability: Expansion capability to 384 analog input channels, 256 analog output channels, 1088 digital inputs and 1088 digital outputs on one 20mA serial line using the μMAC-4000 with expander boards.

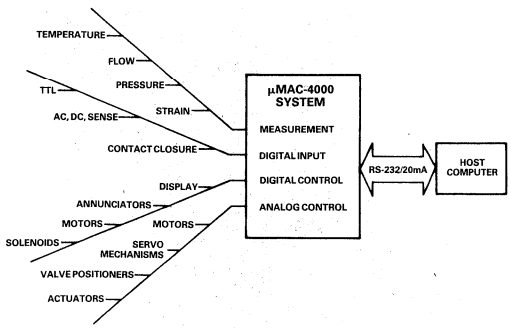
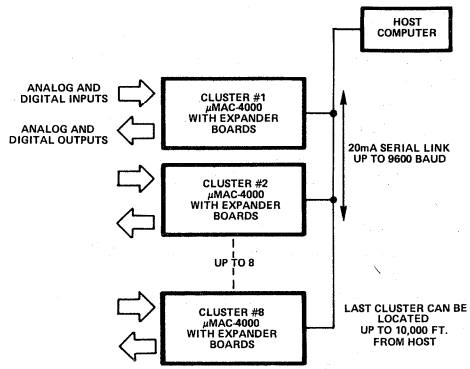
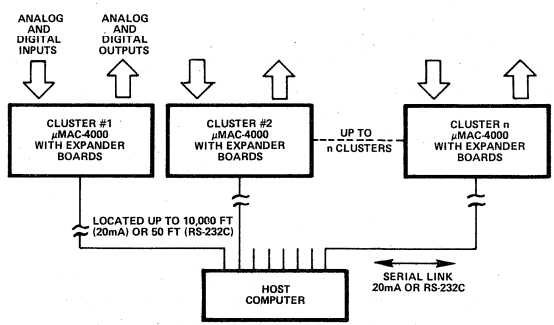


Figure 1. Measurement and Control Concept



Party Line Connection (Multidrop)



Radial Line Connection

Figure 2. µMAC System Configuration

The µMAC-4000 system consists of a family of cards providing the measurement and control functions through interfaces to analog and digital inputs and outputs and the host computer.

µMAC-4000 SERIES

The µMAC-4000 series consists of: the µMAC-4000 Master Board, the µMAC-4010 Analog Input Expander, the µMAC-4030 Analog Output Expander, the µMAC-4040 Digital I/O Expander, and the µMAC-4020 High Level Digital I/O Subsystem. Designed to provide maximum flexibility, it allows you to select only the functions which are required.

SYSTEM CONFIGURATION

A typical configuration can consist of a single µMAC-4000 Master Board which accepts 4, 8, or 12 analog inputs and includes 8 digital inputs and 8 digital outputs. A multiple board configuration (cluster) consists of one µMAC-4000 Master Board and up to six Expander Boards. A µMAC-4000 Master Board must reside in each cluster since it contains the communications and intelligence.

	Number of Channels	
	Single µMAC-4000 Master Board	**Maximum per Cluster**
Analog Input	4,8, or 12	48
Analog Output	0	32
Digital Input	8	136
Digital Output	8	136

Table 1. I/O Capability

A network using up to 8 clusters in a multidrop configuration allows your computer to monitor and control 640 analog and 2176 digital points or varying combination of both types.

COMMUNICATIONS

The µMAC-4000 system is designed to operate with any host computer or terminal which has a 20mA or RS-232C port. A full duplex UART is used to receive and transmit data of selectable baud rates from 110 to 9600 and distances up to 10,000 feet (3048 M). The µMAC's serial link allows use of either the party line (multidrop) or radial (point-to-point) system configuration as shown in Figure 2. The party line connections consist of two twisted pairs of wires and provides substantial cost reductions in wiring and cabling. The RS-232C port includes the control lines (RTS, DTR and CTS) which allow connection to a modem for long distance communication.

POWER

Each µMAC-4000 series board can be powered from either ac line or +24V dc power or both. On-board circuitry detects intermittent ac power losses and automatically switches to an external battery backup mode.

PACKAGING

To facilitate easy installation, single board enclosures, card cages and 19″ rack mounts are available. These 9 1/2″ × 13″ boards can also be installed in sealed industrial cabinets (NEMA enclosures) if the environmental conditions require this type of packaging. (Contact factory for installation guidelines.)

μMAC-4000 MASTER BOARD

FEATURES

4, 8 or 12 Analog Input Channels
Mix and Match Capability
Integral Signal Conditioning: ±1000V CMV, 160dB CMR
13-Bit A/D Converter
8 Digital Inputs/8 Digital Outputs

GENERAL DESCRIPTION

A basic building block in the μMAC-4000 system, the μMAC-4000 contains the unique combination of sensor signal conditioning, analog multiplexing, analog to digital conversion, digital I/O and serial communication all on a single circuit board. A plug-in module approach allows selection of standard signal conditioning modules for direct connection to a wide range of analóg inputs (see Table 2).

μMAC-4010 ANALOG INPUT EXPANSION

The μMAC-4010 Analog Input Expander Board offers low cost channel expansion capability by operating as a slave to the μMAC-4000 Master Board. The same input modules are used to provide mix and match capability along with 4, 8 or 12 analog input channels per board.

Input	Resolution	Accuracy
Thermocouples Type J, K, T, S	0.1°C	±1.3°C
RTDs 100Ω Platinum	0.05°C	±0.3°C
Solid State Temperature Sensors AD590 or AC2626	0.1°C	±0.2°C
Strain Gage Transducers ±30mV, ±100mV Spans	0.025% of Span	±0.01% of Span
Low Level dc Voltages ±25mV, ±50mV, ±100mV	6μV	±0.005% of FS
High Level dc Voltages ±1V, ±5V, ±10V	250μV	±0.1% of FS
DC Currents 0 to ±1mA, 0 to ±20mA, 4-20mA	0.031% of Span	±0.025% of Span

Table 2. μMAC-4000, μMAC-4010 Input Type, Resolution and System Accuracy

SPECIFICATIONS (μMAC-4000, μMAC-4010)

ANALOG INPUTS	
Channel Capacity up to 12 channels (differential)	per board
Common Mode Voltage	±1000V
Common Mode Rejection	160dB
Normal Mode Rejection	86dB
A/D Converter	13-Bit Dual Slope (12 Bits plus Sign)
Conversion Rate	15 or 30 Conversions per second
DIGITAL INPUTS	
Number	8 channels per board
Isolation	±300V pk
Compatiblity	TTL signals or contact closures
DIGITAL OUTPUTS	
Number	8 channels per board
Compatibility	TTL signals

μMAC-4030 8-CHANNEL, ANALOG OUTPUT EXPANDER BOARD

FEATURES

12-Bit Resolution
Voltage or Current Output (±1000V Isolation)
Bumpless Transfer
Increment/Decrement for Back-Up Control
Programmable Slew Rate

GENERAL DESCRIPTION

The μMAC-4030 is an eight channel analog output expander which provides the μMAC-4000 system with digital to analog capability. It contains eight independent 12-bit D/A converters with optional 4-20mA/0-20mA isolated current loop outputs for proportional controllers, valves, actuators, or strip chart recorders. The analog outputs are programmed in engineering units using the μMAC-4000 command set and include features such as increment/decrement for back-up control and programmable slew rates.

This expander board is designed for applications requiring analog output control or display purposes such as indicators, recorders, valve positioners, servo mechanisms and motors.

SPECIFICATIONS (μMAC-4030)

Output Voltage Range	Resolution	Accuracy
0 to +5V	1.22mV	±0.1%
0 to +10V	2.44mV	±0.1%
±5V	2.44mV	±0.1%
±10V	4.88mV	±0.1%
Output Current Range	**Resolution**	**Accuracy**
0 to 20mA	5.3μA (0.026%)	±0.1%
4 to 20mA	5.3μA (0.033%)	±0.1%
Output Protection	130V rms	
Isolation (Input to Output)	±1000V rms	

μMAC-4040 64-CHANNEL, DIGITAL I/O EXPANDER BOARD

FEATURES

32 Digital Inputs
32 Digital Outputs
±300V Peak Optical Isolation on Digital Inputs

GENERAL DESCRIPTION

The μMAC-4040 is a 64-channel, Digital I/O Expander which provides reliable, solid state digital I/O expansion to μMAC-4000. Each board can accommodate 32 digital inputs and 32 digital outputs.

SPECIFICATIONS (μMAC-4040)

Digital Inputs		Digital Outputs	
Number	32 Channels	Number	32 Channels
Isolation	±300 V pk	Compatibility	TTL Signals
Compatibility	TTL Signals or Contact Closures		

18

μMAC-4020 16-CHANNEL, SOLID STATE DIGITAL I/O SUBSYSTEM

FEATURES

Interface to High Level Signals (ac or dc)
2500V ac Optical Isolation
Industrial Type Barrier Strip Connections

GENERAL DESCRIPTION

The μMAC-4020 is a 16-channel, digital I/O subsystem which provides a reliable solid state opto-isolated interface between the μMAC-4000, μMAC-4010 or μMAC-4040 and process I/O. This subsystem increases the μMAC-4000's capability to monitor ac or dc voltages and controls ac and dc loads.

	Type	Voltage Range
AC	Input Voltage	90V–140V 180V–280V
	Output Voltage	12V–140V 24V–280V
DC	Input Voltage	10V–32V
	Output Voltage	Up to 60V

Table 3. Digital I/O Module Selection (μMAC-4020)

SYSTEM CONTROL

Command Set

It is extremely easy for any host computer or terminal to communicate with the μMAC-4000 using a simple, yet powerful command set resident in the μMAC-4000 firmware. The host can delegate measurement and control operations to the μMAC by sending a command on the serial interface line. The μMAC accepts protocol commands for gathering analog and digital data, setting analog outputs and digital bits, activating channels and setting analog input limits. Examples of these commands are listed below.

Command	Function
CHANNEL n	Transmit channel n data.
SCAN n,m	Transmit channel n through channel m data.
SET p,b	Set digital output bit b of port p.
LIMIT n,LL,HL	Sets "HI" and "LOW" limits of channel n.
SDAC n,v	Set channel n to analog value v.

Protocols

Two serial protocols can be used with the μMAC-4000. The "T" protocol is designed for use with CRT and TTY terminals where familiarization, debugging, system calibration and manual control is required. Simple "English-like" commands are used with this protocol. The "C" protocol is designed for use with computers and controllers where communication efficiency, reliability and adaptability to a wide variety of hosts is required.

"T" Protocol Command

SCAN 0,2

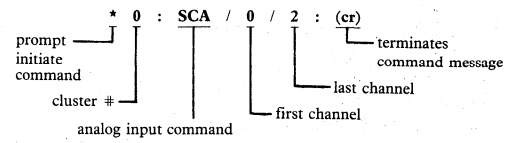
This command requests the μMAC to transmit the latest data for channel 0 through 2.

"T" Protocol Reply

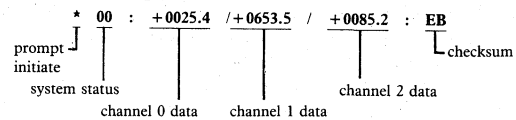
CH0 = +0025.4 CH1 = +0653.5 CH2 = +0085.2

If thermocouples were connected to these channels, the data is in terms of °C or °F.

"C" Protocol Command



"C" Protocol Reply



This reply message contains a μMAC-4000 status and data from the three input channels selected. The μMAC-4000 has scaled, linearized and converted the input data to engineering units.

HOST COMPATIBILITY

The μMAC's simplified ASCII-based protocol can be easily accommodated by a wide range of host computers. As long as RS-232C or 20mA communication ports are available, the μMAC-4000 system can be used as a local front end or remote measurement and control peripheral. The μMAC command set and protocol are easy-to-use, whether you're programming in a high level, assembly or machine language. Typical examples of host computers are listed below:

Microcomputers from–	Intel, DEC, National, Motorola, Mostek, TI, Pro-Log, etc.
Minicomputers from–	DEC, Data General, HP Modcomp, IBM, ADI, etc.
Personal/Professional Computers from–	HP, Apple, IBM, Cromemco, Radio Shack, etc.

DEVELOPED SOFTWARE PACKAGES

RSX-11 Based Systems
HP-85
APPLE II

FEATURES

Reduce Software Development Time
High Level Subroutines
Assume all Communication Responsibility (Checksum Generation and Checking, Timeouts, Status Checking)
Commented Source Code to Allow Modifications
Include Application Programs

GENERAL DESCRIPTION

To minimize software development efforts, Analog Devices offers several software packages designed specifically for popular mini and microcomputers. These software packages convert all μMAC-4000 commands to high level callable subroutines and unburden the user from having to write communication software.

LICENSING AGREEMENT

Analog Devices offers a liberal licensing agreement giving unlimited use of software support packages in development of programs for the μMAC-4000. Analog Devices' only restriction limits the distribution of source codes to a third party.

MACSYM Measurement & Control Systems

MACSYM 2 – MINICOMPUTER CONTROL SYSTEM



MACSYM 2 is a fully integrated Measurement And Control SYsteM developed specifically to acquire, reduce, store, present, and output real-time information in laboratory, process control, and discrete manufacturing applications. From architecture and packaging, to software and documentation, the system is human engineered to minimize the time and experience required to configure, hook-up, program, and operate in your environment.

The complete MACSYM 2 system with integral signal conditioning is packaged in a compact desktop unit – rack mount optional. The basic system includes a high speed 16-bit processor, keyboard, display, tape cartridge storage, and data acquisition subsystem. Our large library of Analog/Digital Input/Output (ADIO*) cards let you configure a system to your exact requirements.

Anyone can configure a MACSYM 2 for a particular application. Just plug the appropriate ADIO cards into any of the 16 card slots provided in MACSYM 2's chassis. Then, connect your external signals directly to the cards, or to screw type terminal boards. System operation is equally simple. There is no need for prior software experience or a separate development system. Write your own application programs immediately in MACBASIC, a multitasking real-time BASIC optimized specifically for measurement and control.

The Central Processor Unit is a 16-bit, general purpose, digital minicomputer, built on Schottky TTL and integrated injection logic, bit-slice technology for optimum speed and low power consumption. The processor's instruction set is near-ideal for measurement and control applications. Special features include byte manipulation instructions and floating point mathematics.

MACSYM 2's fully buffered RAM memory is expandable to 128K bytes. Memory backup power is provided in the event of a power failure.

The ADIO Controller serves as the MACSYM 2's data acquisition subsystem. It interfaces the ADIO cards and the CPU. It shares its central analog to digital conversion system with all ADIO cards to reduce overall system size, complexity, and cost.

This unique dual bus architecture provides a conventional computer bus for communication between the CPU, memory and high speed peripherals, and an ADIO Bus for interfacing the ADIO cards to the ADIO Controller. The ADIO Bus is isolated from the noisy, high speed processor bus for high quality analog measurements.

The MACSYM 2 serves as its own stand-alone terminal. It features a full ASCII keyboard and a CRT display. Display format (16 lines of 32 characters, or 16 lines of 64 characters) is a keyboard selectable option.

System options include:
- Intelligent CRT Terminal
- Remote CRT Monitor
- Printers
- Single and Dual 8″ Floppy Disk Drives
- 9-Track Tape Unit
- Graphics Terminal
- Plotter
- Expansion Chassis
- Nema 12 Cabinet
- IEEE-488, RS-232, 20mA Current Loop Interfaces

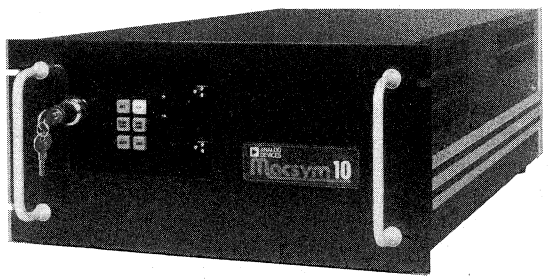
SPECIFICATIONS

Central Processor Unit	
Architecture	16-Bit CPU with hardware floating point
Memory	Up to 128K bytes RAM
System Control Card	
Real-Time Clock	24 Hr. with 10ms resolution
Power Monitor	
Console Serial Interface	RS-232 or 20mA current loop, 110–9600 Baud
ADIO Controller	
Resolution	12 Bit
Conversion Time	25μs
Input Range	± 10V
Software Programmable Gain	1, 2, 4, 8 (more gain available on ADIO cards)
Sample and Hold	90ns max aperture time

*A complete selection of ADIO Cards appears on page II-19-4.

Display	
Integral CRT	5″ (12.7cm) diagonal
Format	16 lines of 32 or 64 characters
Remote CRT	(Optional) one RS-170 75Ω connector provided
Keyboard	Full ASCII keyboard (Upper Case)
Cartridge Drive Unit	
Cartridge	3M DC 100A data cartridge
Capacity	60k bytes
System Console	
I/O Card Slots	16 cards per chassis
Overall Size (with Keyboard)	9.5″H × 17.5″W × 32.5″D (24.13cm × 44.5cm × 82.55cm)
Weight	85 lbs (38.25kg) with 16 ADIO cards
Operating Temperature	41°F – 104°F (5°C – 41°C)
Relative Humidity	Up to 90% noncondensing
Input Power	115V ac, 230V ac ± 10%, 50/60Hz 575 Watts max

MACSYM 10 – COMPUTER CONTROL FOR INDUSTRY



MACSYM 10 is a stand-alone real-time computer control system developed specifically for industrial applications requiring signal conditioning, data collection, computation and control. Ruggedized packaging and PROM base system and user software ensure reliability in a factory floor environment.

You can incorporate complicated control equations into your application using the MACSYM 10. It combines a 16-bit minicomputer with hardware floating point and a multitasking operating system. Write your application programs in MACBASIC, a multitasking real-time BASIC expanded and optimized specifically for measurement and control. The MACSYM 10 can also run previously developed MACSYM 2 software.

The MACSYM 10 uses the same dual bus structure, CPU, and ADIO controller as the MACSYM 2. This architecture minimizes overall system size, complexity and cost while ensuring high quality analog measurements.

Configuring the MACSYM 10 for specific applications is easy. Select the measurement and control functions you need from our extensive family of Analog/Digital Input/Output (ADIO*) cards, plug them into the MACSYM 10, connect your sensors and actuators to convenient screw terminals, and the system is ready to go.

All system software can be stored in PROM. There is space for up to 40K bytes of user PROMs (type 2732). Software is loaded from PROM into RAM and executed out of RAM. Battery backup protection is provided for the RAM memory.

The MACSYM 10 is industrial rugged, capable of operating in temperatures up to 122°F (50°C). Since all software can be stored in PROM, there is no need to worry about the bearing failures or head crashes associated with tape and disk drives. A key lockable door prevents unauthorized access to the system control switches.

The MACSYM 10, combined with a floppy disk drive, CRT terminal, and PROM programmer serves as its own development system. When the application program is complete, it is burned into PROM and loaded into the MACSYM 10. The peripherals can then be removed and the MACSYM 10 placed on the plant floor and put on-line.

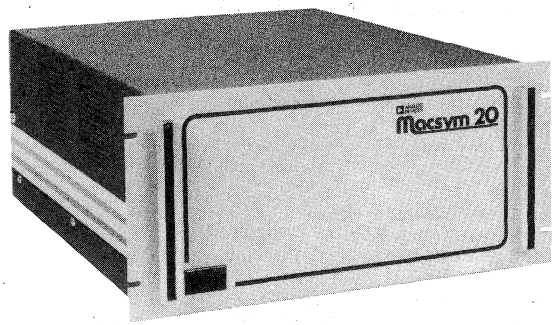
System options include:
- Intelligent CRT Terminal
- Printers
- Single and Dual 8″ Floppy Disk Drives
- Expansion Chassis
- RS-232, 20mA Current Loop Interfaces
- PROM Programmer
- EPROM Eraser
- Nema 12 Cabinet

SPECIFICATIONS

Central Processor Unit	
Architecture	16-Bit CPU with hardware floating point
Memory	Up to 128K bytes RAM
System Control Card	
Real-Time Clock	24 Hr. with 10ms resolution
Power Monitor	
Console Serial Interface	RS-232 or 20mA current loop, 110-9600 Baud
PROM Card	
The PROM card contains the entire operating system and has space for 40k bytes of user 2732 PROMs.	
ADIO Controller	
Resolution	12 Bit
Conversion Time	25μs
Input Range	± 10V
Software Programmable Gain	1, 2, 4, 8 (more gain available on ADIO cards)
Sample and Hold	90ns max aperture time
System Unit	
I/O Card Slots	16 cards per chassis
Overall Size	8.72″H × 19.0″W × 24.25″D (22.1cm × 48.2cm × 61.6cm)
Weight	85 lbs (38.25kg) with 16 ADIO cards
Operating Temperature	41°F – 122°F (5°C – 50°C)
Relative Humidity	Up to 95% noncondensing
Input Power	115V ac, 230V ac ± 10%, 50/60Hz 575 Watts max

*A complete selection of ADIO cards appears on page II-19-4.

MACSYM 20 – INTELLIGENT FRONT-END



The MACSYM 20 is a low cost intelligent front-end which adds multichannel measurement and control capability to your existing computer systems. It can accept up to 16 Analog/Digital Input/Output (ADIO*) cards in any combination. Interfacing to real world signals can be made via screw termination panels.

Because MACSYM 20 incorporates a powerful microcomputer architecture, control of all signal timing, scanning and buffering is handled independently of the host computer. This independent control is supported by MACSYM 20's Z80A CPU and 48K byte internal RAM capacity for program storage and input data buffering.

The MACSYM 20 is programmed using a powerful command set, which permits users to define application tasks using English-like command statements communicated in ASCII. These commands can be PROM resident or downloaded from the host computer. The system software significantly reduces the communications load between the host computer and the MACSYM 20. Once the MACSYM 20 is programmed, it can function on its own should the host computer go down.

Standard communications features include RS-232, RS-422, and 20mA current loop. This flexibility enables the MACSYM 20 to be used in local or remote environments. A 122°F (50°C) temperature specification lets you put the MACSYM 20 on the plant floor, right next to the process under control. Since all data acquisition, signal conditioning, and control outputs are carried out locally, signal wire runs are minimized while overall system accuracy is improved.

MACSYM 20 is ideally suited for OEM applications. Its modular design allows unbundling down to and including the card level.

The low cost and flexibility of the MACSYM 20 make it an attractive replacment for data loggers and microcomputer board level systems.

System options include:
- Up to 48K Byte RAM Memory
- Dual RS-170 Video Outputs
- PROM Programmer
- EPROM Eraser
- Intelligent CRT Terminal
- Remote CRT Monitor
- Nema 12 Cabinet

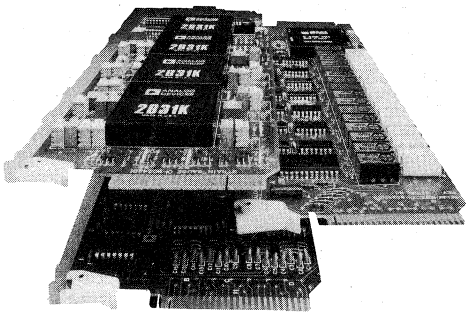
SPECIFICATIONS

Central Processor Unit	
Architecture	Z80A microprocessor
Clock Speed	2.5MHz
Memory	Up to 48K bytes RAM, 16K bytes PROM
System Control Card	
Real-Time Clock	24 Hr. with 10ms resolution
Power Monitor	
Serial Interface	Port A: RS-232C, RS-422 or isolated 20mA Port B: RS-232C or non-isolated 20mA Both ports 110 to 9600 Baud

ADIO Controller	
Resolution	12 Bit
Conversion Time	25μs
Input Range	±10V
Software Programmable Gain	1, 2, 4, 8 (more gain available on ADIO cards)
Sample and Hold	90ns max aperture time
System Unit	
I/O Card Slots	16 cards per chassis
Overall Size	8.75″H × 19″W × 20.75″D (22.2cm × 48.2cm × 55.25cm)
Weight	34 lbs (14.4kg)
Operating Temperature	32°F – 122°F (0° – 50°C)
Relative Humidity	Up to 95% noncondensing

*A complete selection of ADIO cards appears on page II-19-4.

ADIO CARDS – FOR MACSYM 2, 10 & 20



The processing capability of the MACSYM family of computer systems (MACSYM 2, 10, 20) is interfaced to real-world signals through our extensive library of Analog/Digital Input/Output (ADIO) function cards. These ADIO cards provide all of the signal conditioning necessary for connecting directly to thermocouples, strain gages, flow meters, relays, tachometers, valves, alarms, controllers, etc. You merely select the cards you need, connect your sensors and actuators to them using convenient screw terminals, and your system is ready to go. Changing applications is as simple as changing cards.

AIM03 Wide Range Solid State Analog Input

Number of Channels	16 Differential or 32 Single Ended
Resolution	12 Bits
Input Range	± 5mV to ± 10V (Voltage)
	0–20mA (Current)
Speed	Up to 4000 Samples/Sec

AIM05 Strain Gage Input

Number of Channels	4
Bridge Configuration	1, 2 or 4 Arm Bridge Mix or Match
Strain Gage Excitation Voltage	+ 10V or + 5V Switch Selectable

AIM06 RTD Input

Number of Channels	4
RTD Configuration	3 or 4 Wire Mix or Match

AIM09 Isolated Analog Input

Number of Channels	16 Differential
Resolution	12 Bits
Input Voltage Range	± 5mV to ± 10V

TIC03/TIC04 Isolated/Nonisolated Thermocouple Input

Number of Channels	4
Thermocouple Types	J, K, T, E, R & S
Isolation TIC03	1000V at 60Hz

TIC05 AD590 Temperature Transducer Input

Number of Channels	16
Transducers	AD590
Temperature Range	− 55°C to + 150°C
Resolution	0.1°C

STB02/STB03 Isothermal Thermocouple Panel
For use with AIM03 (STB03) or AIM09 (STB02)

Number of Thermocouple Inputs	14 or 28
Thermocouple Type	J, K, T, E, R & S or Any Other

AOC01 High Resolution Analog Output

Number of Channels	4
Output Range Unipolar	0–10V dc at 10mA max
Bipolar	− 10V dc to + 10V dc at 10mA max
Resolution	12 Bits
Settling Time	15µs max

AOC02 High Resolution Current Output

Number of Channels	4
Output Range	4–20mA at 10.5V max or 0–20mA at 10.5V max
Resolution	12 Bits

AOC04/05/06 Analog Output

Number of Channels	4
Output Range	AOC04: 0–10V dc at 10mA max
	AOC05: − 10V dc to + 10V dc at 10mA max
	AOC06: 4–20mA @ 9.5V dc max
Resolution	10 Bits

DIN01 Isolated AC Input

Number of Channels	16
Logic Levels "ON"	>2.53V ac rms at 2mA max
"OFF"	≤1.0V ac rms at 0.3mA max
Isolation Voltage	± 500V dc min

DIN02 Isolated DC Input

Number of Channels	16
Logic Levels "ON"	>3.8V dc rms at 2mA max
"OFF"	≤0.8V dc rms at 0.1mA max
Isolation Voltage	± 500V dc min

DIO01 Solid State Isolated Digital I/O Interface

Number of Channels	16 dc or ac, Input or Output
Isolation	2500V ac max
Inputs	Up to 32V dc and 280V ac
Outputs	Up to 200V dc at 1A and 280V ac at 3A

POC01 Pulse Output/Stepper Motor Output

Number of Channels	2
Output Pulse	Continuous or 0 to 65,535 Counts

DOT01 Digital DC Output

Number of Channels	16
Output Current	100mA max
Output Voltage	30V max
Isolation	± 500V dc

INT01/INT02 Isolated/Nonisolated Interrupt Priority Encoder

Number of Channels	8
Isolation (INT01)	500V dc min

FIN01/02 Frequency Input

Number of Channels	8 (FIN01), 16 (FIN02)
Input Signal Range	1.6Hz to 500kHz

EVC01 Event Counter

Number of Channels	2
Range	16 Bits (65,535)
Isolation	500V dc

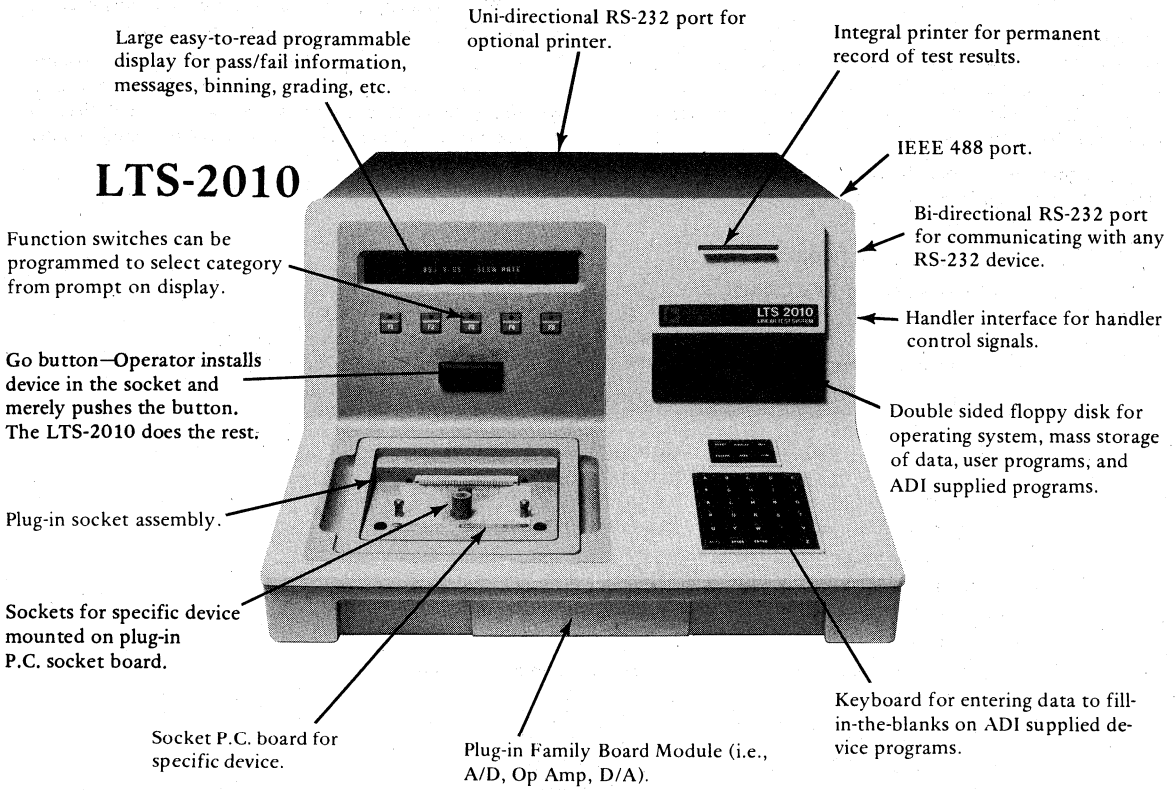
CLK01 Pacer Clock

Used for High Speed Data Acquisition	
Time Interval	20µs to 42905 sec

CLK03 Battery Backed Calendar Clock

Battery Life	20 Days
Clock Accuracy	1 Min/Month

TEST OP AMPS, DACs & ADCs WITH 16-BIT ACCURACY



THE LTS SYSTEM CONCEPT

The LTS systems are easy-to-use, flexible component test systems that allow you to test any component to the manufacturer's own specifications, ADCs, DACs, op amps, regulators, comparators and other linear devices. The system also offers such features as datalogging, statistical analysis, yield analysis and two RS-232 interfaces, IEEE interface and a handler interface.

The computing power of the LTS-systems lies in their 16-bit central processing unit. The microprocessor incorporates a minicomputer instruction set which includes hardware multiply and divide as well as 15 prioritized interrupts for the system keypad, function switches, floppy disk drive, and the IEEE 488 interface.

A real time, 3MHz, four-phase crystal stabilized system clock generates system timing, allowing the implementation of a real time clock. The system memory includes 60K bytes of dynamic RAM, of which 32K bytes are available for program generation by the user.

The LTS-systems not only provide for several data output formats—data log, yield analysis or statistical analysis—they also provide a choice of data display. If desired, the data may be presented via the single line LED display, the integral 20-column thermal printer, through either of the RS-232 ports or the IEEE port. (All data outputs are standard features on both the LTS-2000 and the LTS-2010.)

LTS-2000

The LTS-2000 is far more than a simple tester; it is an optimal low cost solution for incoming inspection. It can be used for basic GO/NO-GO testing, for component selection, for qualification testing, or as a diagnostic tool for component evaluation.

The LTS-2000 can be set up in minutes by using either a program from the device library, or the complete test menu of "Fill-in-the-Blanks" software. Prompts for each step of the "Fill-in-the-Blanks" test programs are conveniently displayed directly over the associated function switches. Standard test programs can be easily altered to suit your needs. Select your test, and arrange them in the order you prefer. The full edit

capability enables you to change test parameters quickly and simply.

LTS-2010

The LTS-2010 is the first benchtop tester that's programmable in BASIC, as well as "Fill-in-the-Blanks" programming, and its 16-bit CPU and 64K bytes of memory offer a new level of programmable sophistication.

Far more than just a comprehensive production tester, it can handle complex engineering analysis, and even incoming inspection. It is the first system that can provide all the capabilities of today's large, centralized test systems at a cost that is approximately one-third the "big system" price.

The LTS-2010 not only provides the flexibility of distributed or decentralized testing, it allows for cost-effective multiple system purchases. And it increases overall test reliability, since the threat of a single big system failure is eliminated in a distributed testing environment.

LTS SPECIFICATIONS

MEASUREMENT ACCURACY

High Accuracy	±(0.0015% of Reading +0.025% of Range +100μV)
Direct	±(0.025% of Reading +0.025% of Range +100μV)
Null and Difference	±(0.025% of Reading +0.025% of [Diff Range + Null Range] +100μV)
Input Voltage Range	±10V (64 Different Ranges)

REFERENCE DAC

Range	Resolution	Software Corrected Accuracy
0 to 10V	2.5mV	RDVO ± 150μV
-5V to 5V	2.5mV	RDVO ± 150μV
-10V to 10V	5mV	RDVO ± 300μV

SYSTEM REFERENCE

Short Term	10V Adjustable in hardware or software
Long Term	10V ±50ppm/1000 hrs, noncumulative

SOURCES

Source	Voltage Range	Resolution	Software Corrected Accuracy
SA	0 to 20V	±0.1V	SAVO ± 0.05V
SB	0 to 20V	±0.1V	SBVO ± 0.05V
SC	0 to -20V	±0.1V	SCVO ± 0.05V
SD	0 to -20V	±0.1V	SDVO ± 0.05V
TH	0 to 10V	±0.05V	THVO ± 0.025V
SR	-10V to 10V	±0.001V	SRVO ± 0.0005V

Source	Current Range	Accuracy of Measurement
SA	-10mA to 150mA	±(2.5% of Reading + 10μA/V + 15μA)
SB	-10mA to 150mA	±(2.5% of Reading + 10μA/V + 15μA)
SC	10mA to -150mA	±(2.5% of Reading + 10μA/V + 15μA)
SD	10mA to -150mA	±(2.5% of Reading + 10μA/V + 15μA)
TH	-10mA to +10mA	±(0.5% of Reading + 10μA)
SR	-10mA to +10mA	±(0.5% of Reading + 10μA)

OPERATING TEMPERATURE

At Rated Accuracy after 1 hr warm-up
0 to 40°C
32°F to 104°F

OPERATING VOLTAGE

105V ac to 125V ac @ 50Hz to 60Hz
210V ac to 250V ac @ 50Hz to 60Hz

Modular AC/DC Power Supplies

Analog Devices ac/dc Power Supplies are designed to provide OEM's and circuit designers with a broad line of high reliability, regulated and short circuit protected power supplies at low overall cost. These modules are available with 5 volt to 15 volt outputs (single, dual and triple) and current ratings from 25mA to 2 amps. Most Analog Devices' Power Supplies are available from stock in both large and small quantities. Substantial discounts apply on quantity orders.

ADVANTAGES

Packaged circuit modules have found wide acceptance. Engineers have discovered the convenience and economy of plug-in building blocks . . . op amps, logic cards, miniature A/D and D/A converters are now available in wide varieties. Now a complete line of modular power supplies is available from Analog Devices. These encapsulated units are shipped ready to use, at prices below the internal manufacturing cost of most OEM users.

TRIPLE OUTPUT SUPPLIES – NEW

Analog Devices offers four new triple output ac/dc designs which are particularly useful in A/D, D/A and signal conditioning applications. Using a triple output supply is often less expensive than purchasing two separate supplies and also saves on space.

Models 972 and 926 provide ±15V @ ±150mA and +5V @ 300mA. Models 974 and 927 provide ±15V @ ±150mA and +5V @ 1000mA. Models 972 and 974 are printed-circuit mountable while models 926 and 927 are chassis-mountable.

5 VOLT 3 AMP SUPPLY – NEW

Models 976 and 928 supplies combine the primary advantages of switching linear regulated supplies in a single, compact package. This +5V 3 amp supply is available in PC-mountable (928) and chassis-mountable models (976).

AC/DC POWER SUPPLIES FEATURES

- Current limited short circuit protection
- PC mounted and chassis mount designs
- Single, dual and triple output designs
- Current outputs of 25mA to 500mA for dual output supplies, 250mA to 3A for single output supplies
- Free-air convection cooling—no external heat sink required

GENERAL SPECIFICATIONS FOR ALL MODELS

Input Voltage: 105V ac to 125V ac, 50 to 400Hz
Temperature Coefficient: 0.02%/°C
Input Isolation: 50 megohms
Breakdown Voltage: 500V rms, minimum
Operating Temperature: -25°C to +71°C
Operating at elevated temperatures may require derating. Consult factory.
Storage Temperature: -25°C to +85°C
Short Circuit Protection: All of the ac/dc Power Supplies employ current limiting. They can withstand substantial overload including direct shorts. Prolonged operation should be avoided since excessive temperature rises will occur.

Modular DC/DC Converters

Analog Devices' compact dc-dc converters satisfy a wide variety of floating power requirements in analog (Computational Circuits, Op Amps, Instrumentation Amps) and digital (a-d/d-a) applications. Available in five power levels of 1 watt, 1.8 watt, 4.5 watt, 6 watt and 12 watt, these designs offer accurate (±0.05% max error), regulated outputs with very low noise. Most models are high efficiency (typically over 60% at full load) that feature complete 6-sided continuous shielding for EMI/RFI protection.

DUAL OUTPUT MODELS

Logic to analog power conversion is available with several models delivering floating power (±12V and ±15V) from logic power sources (+5V). This permits analog networks to be separated from digital systems in order to avoid intersystem grounding problems. Model 945 derives regulated ±15V outputs from any combination of inputs between 23 and 31 volts. The 945 can be powered from dual 12 volt, dual 15 volt, +24 volt or +28 volt power supplies.

DC/DC CONVERTERS FEATURES

- Inaudible (>20kHz) converter switching frequency
- Continuous, six-sided EMI/RFI shielding except on 1 watt and 1.8 watt models
- Free air convection cooling—no external heat sink or specification derating is required over operating temperature range
- Output short circuit protection (either output to common) for at least 8 hrs. at T_A = +71°C
- Automatic restart after short condition removed
- Automatic starting with reverse current injected into outputs

GENERAL SPECIFICATIONS FOR 4.5W, 6W, 12W MODELS

Line Regulation—full range: ±0.05% max (±0.02% max, 960 series)
Load Regulation—no load to full load: ±0.05% max (±0.02% max, 960 series)
Output Noise and Ripple: 1mV rms max
Breakdown Voltage: 500V dc minimum
Input Filter Type: π
Operating Temperature Range: -25°C to +71°C
Storage Temperature Range: -40°C to +100°C

GENERAL SPECIFICATIONS FOR 1W AND 1.8W MODELS

Line Regulation—full range: ±0.3% (±1% max, 949)
Load Regulation—no load to full load: 30% (±0.5% max, 949)
Output Noise and Ripple: 20mV p-p (with 15μF tantalum capacitor across each output), (1mV rms max, 949)
Breakdown Voltage: 300V dc (500V dc min, 949)
Input Filter Type: π (models 958, 960, 962, 964)
Operating Temperature Range: -25°C to +71°C
Storage Temperature Range: -40°C to +100°C

MODULAR AC/DC POWER SUPPLIES

SPECIFICATIONS (typical @ +25°C and 115V ac 60Hz unless otherwise noted)

	Type	Model	Output Voltage Volts	Output Current mA	Line Reg. Max %	Load Reg. Max %	Output Voltage Error Max	Ripple & Noise mV rms Max	Dimensions Inches
PC Board Mounted	Dual Output	915	±15	±25	0.2	0.2	±1%	1	3.5×2.5×0.875
		904	±15	±50	0.02	0.02	±200mV −0mV	0.5	3.5×2.5×0.875
		902	±15	±100	0.02	0.02	+300mV −0mV	0.5	3.5×2.5×1.25
		902-2	±15	±100	0.02	0.02	+300mV −0mV	0.5	3.5×2.5×0.875
		920	±15	±200	0.02	0.02	+300mV −0mV	0.5	3.5×2.5×1.25
		925	±15	±350	0.02	0.02	±1%	0.5	3.5×2.5×1.62
		921	±12	±240	0.02	0.02	+300mV −0mV	0.5	3.5×2.5×1.25
	Single Output	906	5	250	0.02	0.04	±1	1	3.5×2.5×0.875
		903	5	500	0.02	0.04	±1	1	3.5×2.5×1.25
		905	5	1000	0.02	0.05	±1	1	3.5×2.5×1.25
		922	5	2000	0.02	0.05	±1	1	3.5×2.5×1.62
		•928	5	3000	0.05	0.10	±2	5 (typ)	3.5×2.5×1.25
	Triple Output	923	±15	±100	0.02	0.02	±1	0.5	3.5×2.5×1.25
			+5	500	0.02	0.05	±1	0.5	
		•926	±15	±150	0.02	0.02	±2	0.5 (typ)	3.5×2.5×1.62
			+5	300	0.02	0.10	±2	1.0 (typ)	
		•927	±15	±150	0.02	0.02	±2	0.5 (typ)	3.5×2.5×1.62
			+5	1000	0.02	0.10	±2	1.0 (typ)	
		2B35J	±15	±65	0.08	0.1	(−0, +300mV)	0.5	3.5×2.5×1.25
			+1 to +15*	125	0.08	0.1		0.25	
		2B35K	±15	±65	0.01	0.02	(−0, +300mV)	0.5	3.5×2.5×1.25
			+1 to +15*	125	0.01	0.02		0.25	
Chassis Mounted	Dual Output	952	±15	±100	0.05	0.05	±2	1	4.4×2.7×1.44
		970	±15	±200	0.05	0.05	±2	1	4.4×2.7×1.44
		973	±15	±350	0.05	0.05	±2	1	4.4×2.7×2.00
		975	±15	±500	0.05	0.05	±2	1	4.4×2.7×2.00
	Single Output	955	5	1000	0.05	0.15	±2	2	4.4×2.7×1.44
		•976	5	3000	0.05	0.10	±2	5 (typ)	4.75×2.7×2.00
	Triple Output	•972	±15	±150	0.02	0.02	±2	0.5 (typ)	4.75×2.7×1.45
			+5	300	0.02	0.10	±2	1.0 (typ)	
		•974	±15	±150	0.02	0.02	±2	0.5 (typ)	4.75×2.7×1.45
			+5	1000	0.02	0.10	±2	1.0 (typ)	

*Resistor Programmable

•New product since *1980 Data-Acquisition Components and Subsystems Catalog*

MODULAR DC/DC CONVERTERS

SPECIFICATIONS (typical @ +25°C over the full range of input voltages unless otherwise noted)

Model	Output Voltage Volts	Output Current mA	Input Voltage Volts	Input Voltage Range Volts	Input Current Full Load	Output Voltage Error Max	Temperature Coefficient /°C Max	Efficiency Full Load Min	Dimensions Inches
943	5	1000	5	4.65/5.5	1.52A	±1%	±0.02%	62%	2.0×2.0×0.375
•957*	5	100	5	4.5/5.5	200mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
•958	5	100	5	4.5/5.5	200mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
941	±12	±150	5	4.65/5.5	1.17A	±0.5%	±0.01%	58%	2.0×2.0×0.375
•959*	±12	±40	5	4.5/5.5	384mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
•960	±12	±40	5	4.5/5.5	384mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
•961*	±15	±33	5	4.5/5.5	396mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
•962	±15	±33	5	4.5/5.5	396mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
•963*	±15	±33	12V	10.8/13.2	165mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
•964	±15	±33	12V	10.8/13.2	165mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
•965	±15	±190	5V	4.65/5.5	1.7A	±1%	±0.005% (typ)	62% (typ)	2.0×2.0×0.38
•966	±15	±190	12V	11.2/13.2	710mA	±1%	±0.005% (typ)	62% (typ)	2.0×2.0×0.38
•967	±15	±190	24V	22.3/26.4	350mA	±1%	±0.005% (typ)	62% (typ)	2.0×2.0×0.38
•968	±15	±190	28V	26/30.8	300mA	±1%	±0.005% (typ)	62% (typ)	2.0×2.0×0.38
949	±15	±60**	5	4.65/5.5	0.6A	±2%	±0.03%	58%	2.0×1.0×0.375
940	±15	±150	5	4.65/5.5	1.35A	±0.5%	±0.01%	62%	2.0×2.0×0.375
953	±15	±150	12	11/13	0.6A	±0.5%	±0.01%	62%	2.0×2.0×0.375
945	±15	±150	28	23/31	250mA	±0.5%	±0.01%	61%	2.0×2.0×0.375
951	±15	±410	5	4.65/5.5	3.7A	±0.5%	±0.01%	62%	3.5×2.5×0.88

*Unfiltered Models

**Single-ended or unbalanced operation is permissible such that total output current load does not exceed a total of 120mA.

•New product since *1980 Data-Acquisition Components and Subsystems Catalog*

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Selection Guides for Product Categories Not Included in This Volume

INSTRUMENTATION AMPLIFIERS

The abbreviated specifications listed here permit a choice on the basis of the key parameters of instrumentation amplifiers, depending on which parameters are critical for the application. Complete and detailed specifications can be found in the data-sheet section.

Descriptive information on instrumentation and isolation amplifiers and a guide to specifications are provided beginning on page 5-4 in Vol. I. Devices that perform instrumentation-amplifier functions can also be found in section 15 (Data Acquisition Subsystems).

All specifications are typical at rated supply voltage and load, and $T_A = 25°C$, unless otherwise noted.

SELECTION GUIDE – INSTRUMENTATION AMPLIFIERS

	Monolithic IC AD521J(K)(L)(S)[1]	Hybrid IC AD522A(B)(S)[1]	Monolithic AD524J(K)(L)(S)	Hybrid IC AD612A(B)(C)	Hybrid IC AD614A(B)
GAIN					
Range V/V	0.1 to 1000	1 to 1000	1 to 1000	1 to 1024	1 to 1024
Nonlinearity (G = 100) – % max	0.2(0.2)(0.1)(0.2)	0.01(0.005)(0.005)	0.02(0.01)(0.005)(0.02)	0.001	0.001
RATED OUTPUT – V dc/mA	±10/±10	±10/±5	±10/±5	±10/±5	±10/±5
DYNAMIC RESPONSE					
Small Signal (-3dB)					
G = 1000	40kHz	300Hz	25kHz	10kHz	20kHz
Full Power Frequency	100kHz	1.5kHz	–	–	–
Slew Rate – V/μs	10	0.1	5	1	1
OFFSET VOLTAGE					
Input Offset Voltage	3(1.5)(1)(1.5)μV max	±400(200)(200)μV max	250(100)(25)(100)μV	±200μV	±200μV
vs. Temperature	15(15)(2)(5)μV/°C	±6(2)(6)μV/°C	3(1.5)(0.5)(1.5)μV/°C	±5(2)(1)μV/°C	±5(2)μV/°C
Output Offset Voltage	400(1200)(100)(200)μV max		1mV(500μV)(250μV)(500μV)		
vs. Temperature	400(150)(75)(150)μV/°C		50(20)(10)(20)μV/°C		
INPUT BIAS CURRENT – nA max	±80(40)(40)(40)	±25(15)(25)	50(70)(10)(50)μA	+100	+100
INPUT IMPEDANCE					
Common Mode – Ω	6×10^{10}	10^9	10^9	10^9	10^9
COMMON MODE REJECTION RATIO min @ 1kΩ Source Unbalance, CMV = ±10V					
G = 1 – dB	70(74)(74)(74)[2]	75(80)(85) dc to 30Hz	70(75)(80)(70)	74	74
G = 10 – dB	90(94)(94)(94)[2]	90(95)(90) dc to 10Hz	90(95)(100)(90)	80	80
G = 1000 – dB	100(110)(110)(110)[2]	100(110)(100) dc to 1Hz	115(125)(130)(190)	94	94
Volume I Page	5-9	5-15	5-19	5-23	5-23

[1] Processing to MIL-STD-883B available.
[2] DC to 60Hz.

VOLTAGE REFERENCES

		AD589	AD580	AD1403	AD581	AD584	AD2700	AD2710
Output Voltage Range	1.235V	•				•		
	2.5V		•	•		•		
	5.0V					•		
	7.5V					•		
	+10.00V				•	•	•	•
	-10.00V						•	
	±10.00V						•	•
Output Voltage Tolerance	⩽±0.4%		•	•				
	⩽±0.05%				•	•		
	⩽±0.025%						•	
	⩽±0.012%							•
Temperature Stability	⩽25ppm/°C	•		•				
	⩽10ppm/°C		•					
	⩽5ppm/°C				•	•	•	
	⩽1ppm/°C							•
Temperature Range	0 to +70°C	•	•	•	•	•	•	•
	-55°C to +125°C	•	•		•	•	•	
Package Style	Hermetic Package	•	•		•	•	•	•
	Plastic Package			•				
Dice Available		•	•		•	•		
Volume I Page		8-21	8-5	8-25	8-9	8-15	8-29	8-33

CMOS SWITCHES AND MULTIPLEXERS

The devices catalogued in this section are grouped into two classes: Switches and Multiplexers. Descriptions, specifications, and application information can be found in the data sheets; definitions of the terminology can be found on page 16-4 in Vol. I.

CMOS IC SWITCHES

Type	Characteristics	Vol I Page
AD7510DI	Dielectrically isolated Quad SPST; Address High closes switch	16-13
AD7511DI	Dielectrically isolated Quad SPST; Address Low closes switch	16-13
ADG201	Dielectrically isolated Quad SPST, replace DG201	16-33
ADG200	Dielectrically isolated Dual SPST, replace DG200	16-29
AD7512DI	Dielectrically isolated Quad SPDT	16-13
•AD7590DI	Dielectrically Isolated Quad SPST; Data Latches	16-21
•AD7591DI	Dielectrically Isolated Quad SPST; Data Latches	16-21
•AD7592DI	Dielectrically Isolated Dual SPST; Data Latches	16-21

CMOS IC MULTIPLEXERS

Type	Characteristics	Vol I Page
AD7501	8-channel multiplexer, High enables	16-5
AD7503	8-channel multiplexer, Low enables	16-5
AD7502	4-channel differential multiplexer	16-5
AD7506	16-channel multiplexer	16-9
AD7507	8-channel differential multiplexer	16-9

•New product since the *1980 Data-Acquisition Components and Subsystems Catalog.*

Product Families Not in this Databook (But Still Available)

The information published in this Databook is intended to assist the user in choosing components for the design of *new* equipment, using the most cost-effective products available from Analog Devices. The popular product types listed below may have been designed into your circuits in the past, but they are no longer likely to be the most economic choice for your new designs. Nevertheless, we recognize that it is often a wise choice to refrain from redesigning proven equipment, and we are continuing to make these products available for use in existing designs or in designs for which they are uniquely suitable. Data sheets on these products are available upon request.

AD108/208/308
AD108A/208A/308A
AD111/211/311
AD351
AD502
AD511
AD512
AD514
AD520
AD523
AD528
AD530
AD531
AD559
AD801
AD2003
AD2008
AD2020
AD2022
AD2023
AD3900 Series
AD7513
AD7519
AD7570
AD7583
ADC-QM
ADC-QU
ADC-8S
ADC-10Z
ADC-12QZ
ADC-14I/17I
ADC-16Q
ADC1100
ADC1102
ADC1103
ADC1105
ADC1109
ADC1111
ADC1133
B100
BDM1615/1616/1617
DAC-M
DAC-QG
DAC-QM
DAC-QS
DAC-QZ
DAC-10DF
DAC-10Z
DAC1009
DAC1118
DAC1125
DAC1132
DAC1137
DAS1150
DAS1151
DGM1040
MDA-F
MDA-10Z
RTI-1220
RTI-1221
SCDX1623
SCM1677
SDC1604
SHA-1A
SHA-2A
SHA-3
SHA-4
SHA-5
SHA-1114
SHA-1134
SMC1007
SMX1004
SMX2607
SRX1005
SRX2605
STX1003
STX2603
40
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956

Substitution Guide for Product Families No Longer Available

The products listed in the left-hand column are no longer available from Analog Devices. In many cases, comparable functions and performance may be obtained with newer models, but–as a rule–they are not directly interchangeable. The closest recommended Analog Devices equivalent, physically and electrically, is listed in the right-hand column. If no equivalent is listed, or for further information, get in touch with Analog Devices.

Model	Closest Recommended Equivalent
AD501	AD511
AD505	AD509
AD508	AD517
AD513	AD503
AD516	AD506
AD550	None
AD551	None
AD553	None
AD555	AD7519
AD810-813	None
AD814-816	None
AD818	None
AD820-822	None
AD830-833	None
AD835-839	None
AD840-842	None
AD7516	AD7510DI
ADC1121	AD7550
ADM501	ADM501/506
ADP501	ADP511
DAC-10H	DAC-10Z
DAC1112	DAC12QS
DAC1122	AD7541
IDC1703	IRDC1730/1731
MDA-LB	None
MDA-LD	None
MDA-UB	None
MDA-UD	None
MDA-8H	MDA-10Z
MDA-10H	MDA-10Z
MDA-11MF	AD7521
SERDEX	μMAC-4000
SHA-6	SHA1144
SSCT1621	None
TSDC1608-1611	TSL1612
2N3954	None
2N5900	None
41	AD515
47	48
101 (module)	45
102	48
106	118
107	118
108	52
110	48
111	AD308
114	119
115	43
120	50
142	48
143	52
149	50
153	AD517
161	165
163	165
170	171
220	234
231	233
274J	284J
279	286J
280	281
282J	292A
283J	292A
301 (module)	52
302	310 (module)
350	None
427	424
602J10	AD612
602J100	AD612
602K100	AD612
603	AD612
901	904
907	921
908	921
909	921
931	None
932	None
933	None
935	None
948	947
971	921

Analog Devices provides a wide array of FREE technical publications. These include data sheets for all products, catalogs, Application Notes and Guides, and two serial publications: *Analog Productlog*, a digest of new-product information, and *Analog Dialogue*, our technical journal, with in-depth discussions of products, technologies, and applications.

In addition to the free publications, three technical handbooks, a set of *Analog-Digital Conversion Notes*, and *Synchro and Resolver Conversion*, published at the end of 1980, are available at reasonable cost.

A brief description of this literature appears below. If you would like copies, or if you want to receive *Analog Productlog* and *Analog Dialogue*, please get in touch with Analog Devices or your nearby sales office.

CATALOGS

DATA ACQUISITION PRODUCTS DATABOOK (this book)
Two volumes of data sheets for all Analog Devices ICs, hybrids, modules, and subsystems recommended for new designs.

1981-1982 SHORT-FORM GUIDE to Electronic Products for Precision Measurement & Control
A 48-page catalog of all ADI Products.

APPLICATION NOTES AND GUIDES

ISOLATION AND INSTRUMENTATION AMPLIFIER DESIGNERS GUIDE
This guide explains, in detail, the differences between isolation and instrumentation amplifiers, and the applications for which each type is optimized (24 pages).

MULTIPLIER (Analog) APPLICATION GUIDE
Over 30 workable applications for the ubiquitous multiplier. Circuits, specifications and theory (50 pages).

APPLICATION GUIDE TO CMOS MULTIPLYING D TO A CONVERTERS
This 44-page guide includes detailed information on the internal design and successful application of CMOS MDACs. Typical circuits discussed include measurement, function generation, programmable filters, and audio control.

IC VOLTAGE TO FREQUENCY CONVERTER APPLICATION NOTES
Twenty-four pages of V to F converter applications.

A USER'S GUIDE TO IC INSTRUMENTATION AMPLIFIERS
Application note tells how they work, explains their specifications and provides an example of error budget computation (12 pages).

AN IC AMPLIFIER USER'S GUIDE TO DECOUPLING, GROUNDING, AND MAKING THINGS GO RIGHT FOR A CHANGE (8 pages)
A down-to-earth application note on the often ignored topic of ground management in combined analog and digital systems.



UNDERSTANDING HIGH SPEED (Video) A/D CONVERTER SPECIFICATIONS
A sixteen-page profusely illustrated application note.

DESIGNER'S GUIDE TO HIGH-RESOLUTION PRODUCTS
20-page brochure describes how to use 14-, 16-, and 18-bit Data Converters and where to apply them.

MACSYM SYSTEM NOTES:
Multitasking, RS-232 Interface, and P-I-D Control Loops

BOOKS

SYNCHRO & RESOLVER CONVERSION (1980)
Edited by Geoffrey Boyes
Everything you need to know about interfacing synchros, resolvers, and Inductosyns™ to digital and analog circuitry. $11.50

TRANSDUCER INTERFACING HANDBOOK (1980)
A Guide to Analog Signal Conditioning
Edited by D.H. Sheingold
A book for the electronic engineer who must interface temperature, pressure, force, level or flow transducers to electronics, these 260 pages tell how transducers work–as circuit elements–and how to connect them to electronic circuits for effective processing of their signals. Hardcover $14.50

MICROPROCESSOR SYSTEMS HANDBOOK (1977)
by Dr. D. Philip Burton and Dr. A. L. Dexter
Two hundred pages of concise explanation of microprocessor hardware and software, and how to interface to A/D and D/A converters. Hardcover $9.50

ANALOG-DIGITAL CONVERSION NOTES (1977)
Edited by D.H. Sheingold
A 250-page guide to A/D and D/A converters and their applications, illustrated by more than 275 diagrams and tables. $5.95

NONLINEAR CIRCUITS HANDBOOK (1974)
Edited by D. H. Sheingold
A 540-page guide to multiplying and dividing, squaring and rooting, rms-to-dc conversion, and multifunction modules with 325 illustrations. Principles, circuitry, performance, specifications, testing, and application of these devices. $5.95

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